Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

TEN BITS DIFFERENTIAL TRANSCEIVER (Version B)

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1. GENERAL INFORMATION

The goal of these specifications is to define a TEN bits transceiver for the SVX II Silicon Strip Detector Upgrade Project. There are several uses intended for these transceivers:

a) to transmit data from the Port Card [1] to the Fiber Interface Board (FIB) [2]
b) to transmit commands from the FIB to the Port Card
c) to transmit bi-directional data and commands between the Port Card and SVX-II chips (a configuration suitable for D0)
d) to drive clocks and control signals from the Port Card to the SVX-III chips [3]

Figure 1 (a) shows the configuration of this chip, while Figure 1 (b) shows the just one transceiver gate. Each differential transceiver gate is formed by two units:

a) one is a transmitter, with differential inputs I and I* and differential outputs D and D*. The outputs can be tri-state by the control line EN_XMT*.
b) the other is a differential receiver, with inputs D and D* and output O. The output of the receiver can be tri-state by the control line EN_RCV.

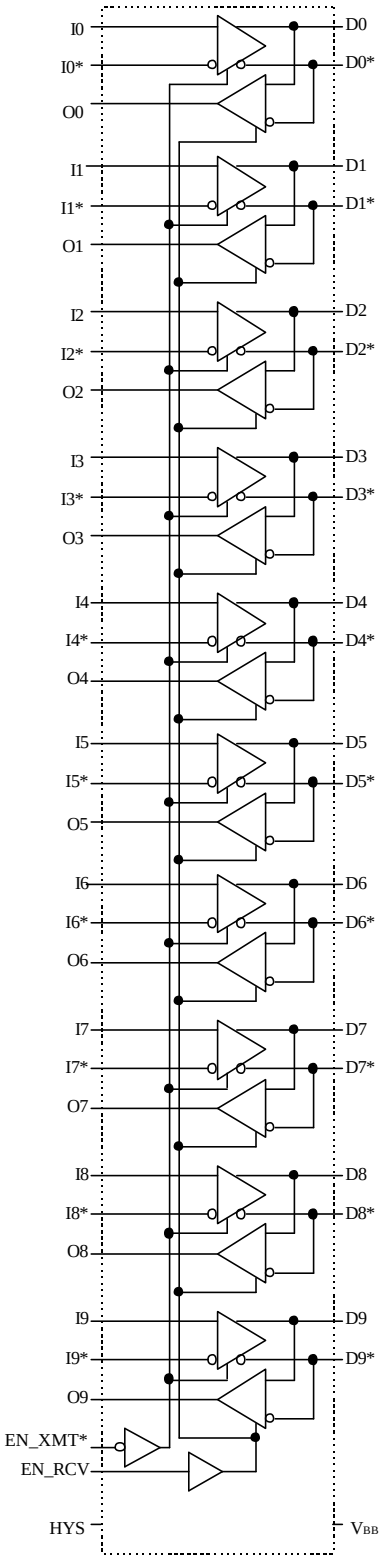
Along these specifications, when we refer to "transmitter", we are referring to the transmitter unit of the transceiver, and when we refer to "receiver", we are referring to the receiver unit of the transceiver. For completeness, these present specifications **MUST** be supplemented by the Low Current Differential Signals (LCDS) specifications [4], which defines the characteristics of the differential signals in the D and D* lines of the transmitter and receiver. Therefore, in this present specifications, we will not refer to the characteristics of the D and D* lines. Finally, all transmitter and receiver gates should adhere to the specifications.

The transceiver is composed by ten transceiver gates controllable by the EN_XMT* and EN_RCV lines[1]. Table 1 shows the true table of the enable control lines. When using the transmitter, EN_RCV should be low to disable the receiver, and when using the receiver, EN_XMT* should be connected to high to disable the transmitter. In this way, the chip will consume less current: disabling the transmitter or receiver reduces the power consumption of that specific unit. Also, avoids contention when using the receiver.

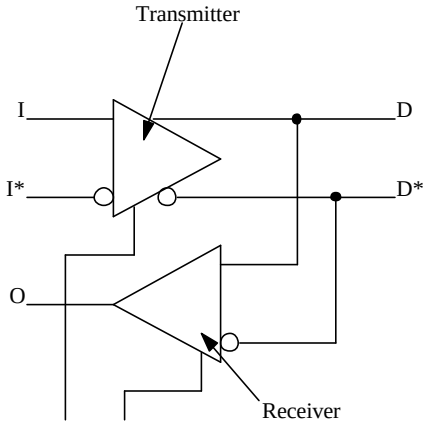
Transmitter Enable (EN_XMT*)	Receiver Enable (EN_RCV)	Operation
high	low	transmitter output (D and D*) tri-state
low	low	transmitter output (D and D*) active
high	low	receiver output (O) tri-stated
high	high	receiver output (O) active

Table 1. True table for the enable control lines

[1] MOSIS submission of the transceiver requires a logical level one in the input EN_XMT to enable the transmitter. The Honeywell version will have a logical level zero in the input EN_XMT to enable the transmitter, as described in the specifications. See Section 5.



(a) Transceiver chip



(b) Transceiver gate

Figure 1. Transceiver

The signal HYS (receiver hysteresis level) are common to all receivers and set the hysteresis level of the D and D* lines (see the Low Current Differential Signal specifications for the details of I_{REF} and H control lines). V_{BB} is a reference voltage used to transform the differential inputs in single ended inputs[2].

The transceiver chip requires specific bias currents for the driver and for the receiver. Furthermore, one of the operation modes of the transmitter requires jumpers to ground to set the differential output current. These details are not shown in Figure 1, but they are described in details in Section 4. The document Ten Bit Differential Transceiver Testing describes testing and results done with the MOSIS submission of the transceiver chip [5].

Figure 2 shows the model for the differential outputs of the transmitter. There are two different ways to drive the outputs: using the current sources and/or using the programmable resistors.

The transistors T shown in Figure 2 operate like switches, sourcing or sinking current from the outputs OA and OB. The control of the transistors (signals A+ and A- in Figure 2) must be such that the transistors behave in the following way: when the transmitter input (not shown in Figure 2) is set to ONE, transistors T_{A1} and T_{B2} are closed, while T_{A2} and T_{B1} are open; when the input of the transmitter is set to ZERO, we have the opposite, transistors T_{A2} and T_{B1} are closed, and T_{A1} and T_{B2} are open.

[2] On the MOSIS submission, V_{BB} has to be provided by an external voltage divider. The Honeywell submission will have this divider inside.

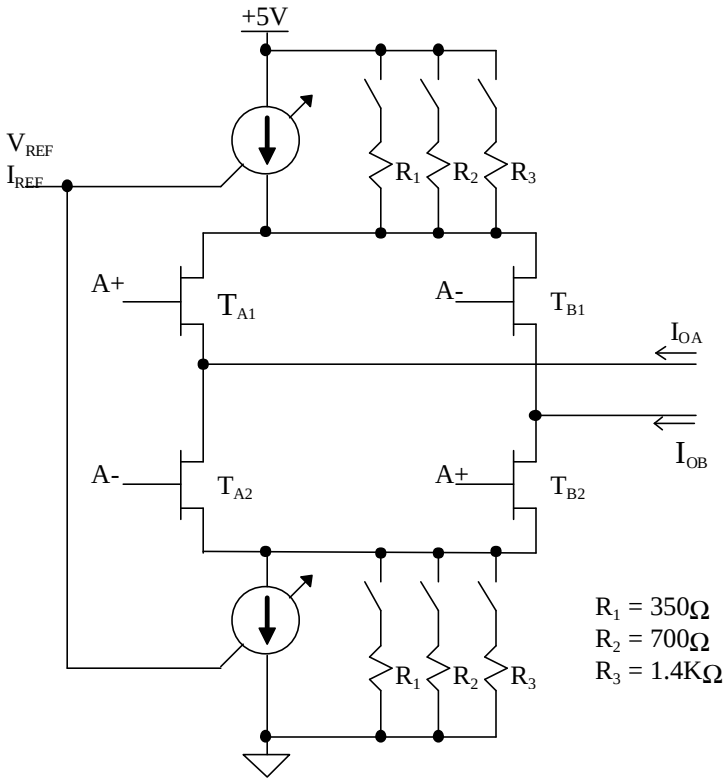


Figure 2. Transmitter Model

Next, we will augmented the LCDS specifications to complete describe this transceiver.

2. ELECTRICAL SPECIFICATION

Table 2 to Table 5 contain the electrical DC and AC specifications of the transmitter and receiver, while Table 6 contains the absolute maximum rating. Refer to Figure 1 for the labeling used. Note that we will not be referring to the specification of the lines D and D*, which can be found in the Reference [4]. The enable inputs (EN_XMT* and EN_RCV) and the receiver hysteresis level HYS are TTL inputs. For the specifications of the receiver hysteresis levels see Reference [4]. V_{BB} is specified in Table 3.

V_{CC}=5V ± 5%, T_{DIE}=35°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Units
V_{ICM}	Minimum input common mode voltage range	V_{CC}= 5 V, $\|V_I - V_{I*}\| \le 0.2V$	0.5	4.0	V
$\|V_I - V_{I*}\|$	Differential input voltage[3]		0.1	5	V
$\|V_{ITH}\|$	Differential input threshold			60	mV
V_{IHYST}	Differential input hysteresis		15	20	mV
$R_{IDIF(DC)}$	DC differential input impedance		50		KΩ
$R_{ICM(DC)}$	DC common mode input impedance		50		KΩ
V_{EDH}	Enable high level input voltage	V_{CC} = 5.25 V	2		V
V_{EDL}	Enable low level input voltage	V_{CC} = 4.75 V		0.8	V
I_{EDH}	Enable high level input current	V_{CC} = 5.25 V		40	µA
I_{EDL}	Enable low level input current	V_{CC} = 4.75 V		-1.6	mA

Table 2. Transmitter DC specifications

V_{CC} =5V ± 5%, T_{DIE}=35°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output voltage low	V_{CC} = 5.25 V I_{OL} = 10 mA	0.2	0.4	V
V_{OH}	Output voltage high	V_{CC} = 4.75 V I_{OH} = - 10 mA	2.4	4.0	V
V_{BB}	Bias voltage	R_{LOAD} = 100 KΩ	1.1	1.9	V
$V_{H[0:1]}$, $I_{H[0:1]}$	Hysteresis input characteristics: the same as the transmitter enable.				
V_{ER}, I_{ER}	Enable input characteristics: the same as the transmitter enable.				

Table 3. Receiver DC specifications

[3] Refer to Section 2.1 to a precise definition of differential input voltage, threshold and hysteresis

V_{CC}=5V ± 5%, T_{DIE}=35°C , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Units
$R_{IDIF(AC)}$	AC differential input impedance	Freq. = 53 MHz	50		KΩ
$R_{ICM(AC)}$	AC common mode input impedance	Freq. = 53 MHz	50		KΩ
t_{DP}	Propagation delay (low to high, and high to low)	25 Ω < Z_{LOAD} < 120 Ω[4]	4	6	ns
t_{DJ}	Propagation jitter	Any differential pair[5] 25 Ω < Z_{LOAD} < 120 Ω, T_{DIE} = 35°C		0.5	ns

Table 4. Transmitter AC characteristics

[4] Propagation delay time of the transmitter is measured at 50% of the voltage transition of input and output.
[5] Jitter of the output of the transmitter is measured at the 50% of the voltage transition.

V_{CC}=5V, T_{DIE}=35°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Units
DC_{ODIST}	Output duty cycle distortion	Input freq. = 35 MHz, 50% duty cycle; C_L= 20pF, R_{LOAD} = 500Ω	47.5	52.5	%
t_{OF}	Fall time	C_L= 20pF, R_{LOAD} = 500Ω[6]	1	3	ns
t_{OR}	Rise time	C_L= 20pF, R_{LOAD} = 500Ω[7]	1	3	ns
t_{OSKEW}	Channel to channel skew	C_L= 20pF, R_{LOAD} = 500Ω[8]		0.5	ns
t_{OP}	Propagation delay (low to high, and high to low)	C_L= 20pF, R_{LOAD} = 500Ω[9]		6	ns
t_{OJ}	Propagation jitter	C_L= 20pF, R_{LOAD} = 500Ω[10], 15°C≤ T_{DIE}≤ 40°C		0.5	ns

Table 5. Receiver AC characteristics

Parameter	Limit
Output voltage	-0.5 to V_{CC}+0.5 V
Input voltage	-0.5 to V_{CC}+0.5 V
Temperature	60°C
DC power supply	-0.5 to 7 V

Table 6. Absolute maximum ratings

2.1 Definition of the Transceiver Specifications

In this Section we will describe in details what we understand by differential input voltage, threshold and hysteresis. Figure 3 shows these concepts.

The differential input voltage ($|V_I - V_{I*}|$) is the module of the difference between the voltages in the inputs I and I*. In our specifications it can vary from 100 mV to 5V.

[6] Fall time is the time the output takes to fall from 2.4 V to 0.4 V.
[7] Rise time is the time the output takes to rise from 0.4 to 2.4 V.
[8] Skew of the output of the receiver is measured at 1.3V.
[9] Propagation delay of the receiver is measured at 50% of the current transition of the input and 1.3V of the output.
[10] Propagation jitter of the output of the receiver is measured at 1.3V.

The differential input threshold ($|V_{ITH}|$) is a region of the differential voltage of the inputs where the output is not known. So, in our specifications, if $|V_I - V_{I*}|$ is smaller than $|V_{ITH}| = 60$ mV, we don't know the state of the outputs of the transmitters (D and D*).

Finally, we have specified differential hysteresis in order to reject noise in the input when the differential input voltage of the transmitter $|V_I - V_{I*}|$ is switching. The hysteresis is a differential voltage locate inside the threshold region. So, when the inputs of the transmitter are switching, a differential noise added to the I and I* lines smaller than 90 mV (as our specifications require) is guarantee not to change the state of the outputs of the transmitter.

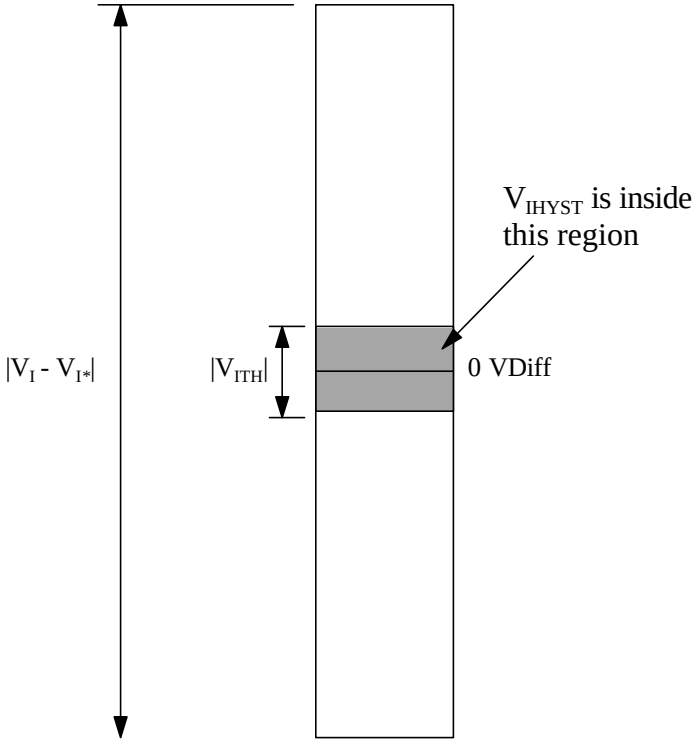


Figure 3. Definition of differential input voltage, threshold and hysteresis

3. MECHANICAL REQUIREMENTS

The transceiver will be used in bare dye and in some package form (possibly some miniaturized SOIC).

4. PAD ASSIGNMENT AND DIE DIMENSIONS

The die size, starting and ending on the outer corner of the outer pads is 2502 x 2503 um, with 150 um pad pitch. Figure 4 shows the pad assignment and location.

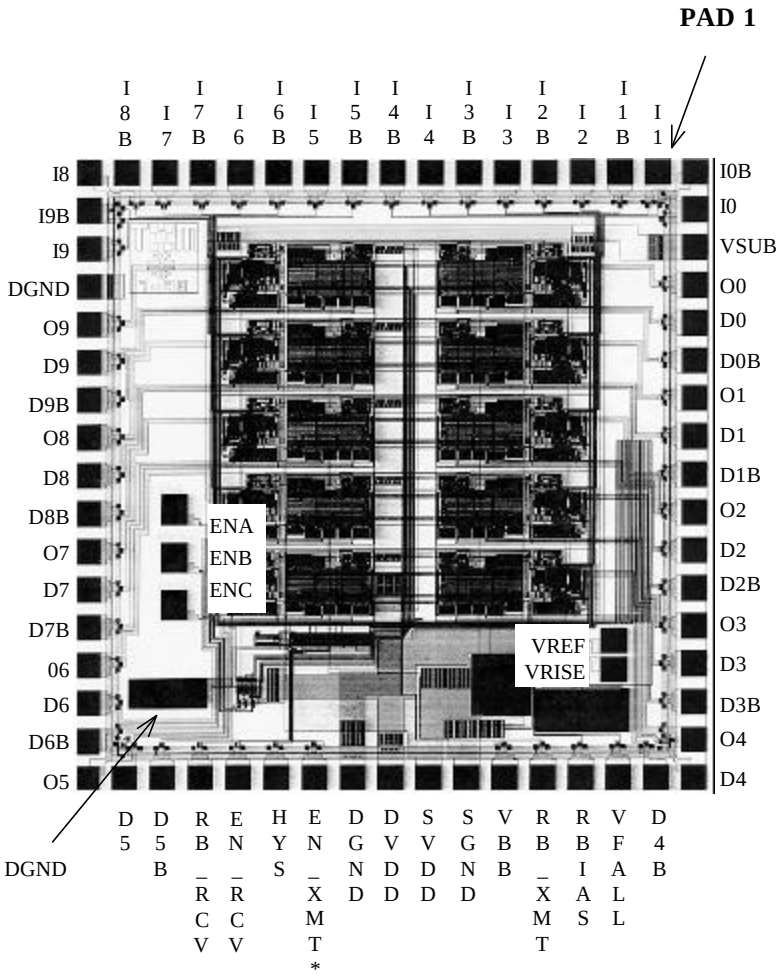


Figure 4. Transceiver Chip Pad Assignment (Version B)[11]

Below, the description of the Transceiver chip, version B padout:

1. I1: Bit 1 input to the transmitter
2. I1B: Complement Bit 1 input to the transmitter
3. I2: Bit 2 input to the transmitter
4. I2B: Complement Bit 2 input to the transmitter
5. I3: Bit 3 input to the transmitter
6. I3B: Complement Bit 3 input to the transmitter
7. I4: Bit 4 input to the transmitter

[11] Figure 4 shows the pad-out for the Honeywell submission. The only change in the MOSIS submission is that ENA, B, & C are lined up vertically directly above RB_RCV. The order of the three pads is also reversed with ENC on top (farthest from RB_RCV), followed by ENB & A. In addition, DGND, for ENA, B, & C, is positioned parallel to the three pads, directly above D5B.

8. I4B: Complement Bit 4 input to the transmitter
9. I5B: Complement Bit 5 input to the transmitter
10. I5: Bit 5 input to the transmitter
11. I6B: Complement Bit 6 input to the transmitter
12. I6: Bit 6 input to the transmitter
13. I7B: Complement Bit 7 input to the transmitter
14. I7: Bit 7 input to the transmitter
15. I8B: Complement Bit 8 input to the transmitter
16. I8: Bit 8 input to the transmitter
17. I9B: Complement Bit 9 input to the transmitter
18. I9: Bit 9 input to the transmitter
19. DGND: Digital ground
20. O9: Bit 9 receiver output
21. D9: Bit 9 output of the transmitter
22. D9B: Complement Bit 9 output of the transmitter
23. O8: Bit 8 receiver output
24. D8: Bit 8 output of the transmitter
25. D8B: Complement Bit 8 output of the transmitter
26. O7: Bit 7 receiver output
27. D7: Bit 7 output of the transmitter
28. D7B: Complement Bit 7 output of the transmitter
29. O6: Bit 6 receiver output
30. D6: Bit 6 output of the transmitter
31. D6B:Complement Bit 6 output of the transmitter
32. O5: Bit 5 receiver output
33. D5: Bit 5 output of the transmitter
34. D5B: Complement Bit 5 output of the transmitter
35. RB_RCV: Bias for receivers, nominal 12KΩ resistor (can be variable) connected to DVDD
36. EN_RCV: When connected to DVDD enables for the receiver
37. HYS: When connected to DVDD enables the hysteresis

38. EN_XMT*: When connected to DGND enables for the transmitter[12]
39. DGND: Digital ground
40. DVDD: +5V digital power supply
41. SVDD: +5V output driver power supply, connect to digital power supply
42. SGND: Output driver ground, connect to digital ground
43. VBB: Output reference voltage of 1.5V[13]
44. RB_XMT: Bias resistor for the transmitter, nominal 50K (can be variable up to 120K) connected to DVDD.
45. RBIAS: Provides the bias current for the current sources associated with the differential output of the transmitter. The current mirror connected with RBIAS has an amplification factor around 50 times, so 0.1 mA passing over the RBIAS resistor provides around 5 mA output current. The resistor should be connected between RBIAS and DGND. A 33 KΩ resistor provides about 5 mA of output current. A resistor of 15 KΩ achieves approximately 10 mA. When the output current sources are being used, ENA, ENB and ENC should be left disconnected (See LCDS specifications [4]).
46. VFALL: Generated internally to set the current at the output of the transmitter circuit. It should be used in conjunction with VRISE. In general, left unconnected.
47. D4B: Complement Bit 4 output of the transmitter
48. D4: Bit 4 output of the transmitter
49. O4: Bit 4 receiver output
50. D3B: Complement Bit 3 output of the transmitter
51. D3: Bit 3 output of the transmitter
52. O3: Bit 3 receiver output
53. D2B: Complement Bit 2 output of the transmitter
54. D2: Bit 2 output of the transmitter
55. O2: Bit 2 receiver output
56. D1B: Complement Bit 1 output of the transmitter
57. D1: Bit 1 output of the transmitter
58. O1: Bit 1 receiver output
59. D0B: Complement Bit 0 output of the transmitter

[12] MOSIS submission of the transceiver requires a logical level one in the input EN_XMT to enable the transmitter. The Honeywell version will have a logical level zero in the input EN_XMT to enable the transmitter, as described in the specifications. See Section 5.

[13] On the MOSIS submission, V_{BB} has to be provided by an external voltage divider. The Honeywell submission will have this divider inside.

60. D0: Bit 0 output of the transmitter

61. O0: Bit 0 receiver output

62. VSUB: Connect to DGND.

63. I0: Bit 0 input to the transmitter

64. I0B: Complement of Bit 0 input to the transmitter

There are 6 pads which are placed inside the chip and are listed below:

a) VREF: Input, voltage reference for the transmitter common mode voltage. The 2.5V reference for 2.5V transmitter common mode voltage is generated internally.

b) VRISE: Input. Generated internally to set the current at the output of the transmitter circuit. It should be used in conjunction with VFALL. In general, left unconnected.

c) ENC, ENB, ENA: Programmable resistors to adjust the differential output current of the transmitter. When the resistors are used, the output current sources should be disabled (connect RBIAS to DVDD). These pads have internal pull-up that disable the resistors. These enables select two resistors that form a voltage divider with the termination resistor. (See LCDS specifications [4]). Table 7 describes the relation between output resistor and enable.

d) DGND: Digital ground.

Control Pad	**Resistor (W)**
ENA	350
ENB	700
ENC	1400

Table 7. Relation Between Output Resistor and Enables

5. MOSIS PROTOTYPE OF VERSION B

We have tested the MOSIS prototype of version B of the transceiver chip. We identified the following items that were corrected in the Honeywell submission:

a) Version B, MOSIS prototype does not have the internal voltage divider for V_{BB}, which has to be supplied externally to this pad of the chip. V_{BB} is used inside the chip.

b) Also, to enable the transmitter, one has to provide logical level “1” to the EN_XMT pad. This changed to EN_XMT* in the Honeywell version.

c) The polarity of the differential inputs of the receiver (D and D*) are inverted in relation to the output.

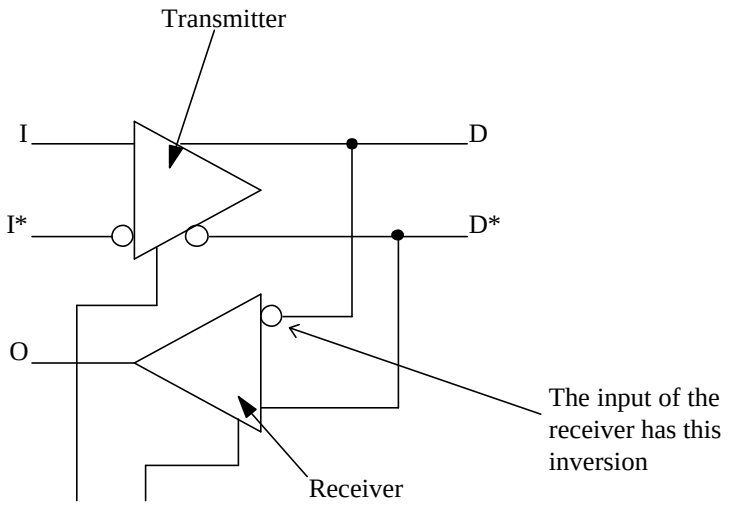


Figure 5. Transceiver Gate of Version B, MOSIS Submission

5.1 Power Supply Current

We have measured the power supply currents of both the driver and receiver. These measurements were taken with the MOSIS submission. It was accomplished by placing an ammeter between the power pins of the transceiver chip and the power of the LCDS daughter cards (XMIT LCDS Transmitter Board & RECV LCDS Receiver Board). The setup was bypassed using 10 and 0.1 μF capacitors to decouple the ammeter. See Figure 6 for this implementation.

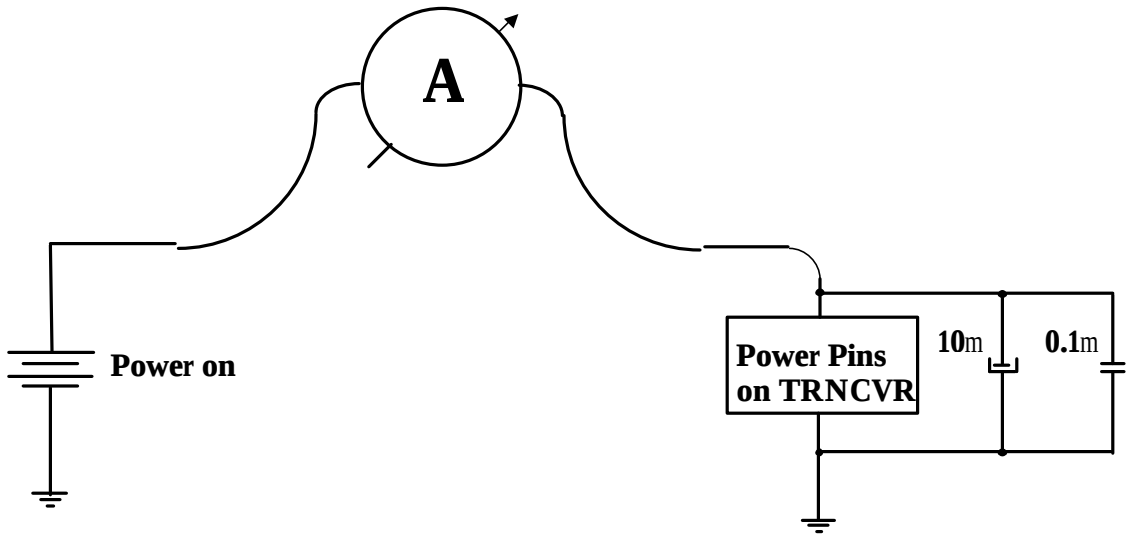


Figure 6. Setup to Measure Power Supply Current

We have taken measurements at 24 and 53 MHz, and with minimum and maximum output current (3.1 and 15.5 mA, respectively). There are also four states in which measurements were taken.

- Power on, but no data being transferred
- normal operation- data transferred using the **alt** pattern
- sending a DC of zeros (giving the command: *send 34 00000000*, at the BERT terminal)
- sending a DC of ones (giving the command: *send 34 ffffffff*)

The results are reported in Table 8 and Table 9.

Frequency (MHz)	Output Current	No data transfer (mA)	Normal Operation (mA)	Sending '0's (mA)	Sending '1's (mA)
24	min	40	48	38	40
53	min	41	52	39	41
24	max	158	157	155	159
53	max	160	182	157	160

Table 8. Transmitter Power Supply Currents

Frequency (MHz)	Output Current	No data transfer (mA)	Normal Operation (mA)	Sending '0's (mA)	Sending '1's (mA)
24	min	22	52	23	62
53	min	22	47	22	61
24	max	21	52	21	60
53	max	23	61	23	62

Table 9. Receiver Power Supply Currents

It is noted that during the testing of the power supply current while sending '1's, the current, at times, would be read as much more than what Tables 7 & 8 indicate. For example, when the frequency was 24 MHz and the output was set to minimal current, the table indicates the power supply current when transmitting '1's to be 40 mA. However, some measurements taken after executing *send 34 ffffffff*, gave values of 80 mA. After further investigation on the cause of the discrepancy, it was the reveled that the 100S325 ECL to TTL translator chips were not always driving hard '1's to the transceiver chip after executing the command. When the transceiver chip receives these unrecognized states, it draws more current. This problem was not seen when transmitting alternating 0's and 1's (normal operation).

From the results, we can see that for the receiver the power supply current relatively does not change with variation of frequency and driver output current.

6. PREVIOUS VERSION (VERSION A) OF TRANSCEIVER CHIP

Two previous versions of the transceiver chip were submitted, one for the MOSIS process and another for the Honeywell process. We will call this version as version A. The two submissions of version A have the same padout, the same functionality and operate in the same

way. Therefore, we will consider them as just one submission. An important difference between version A and B has to do with the transmitter portion. Version A doesn't have the option to select resistors (see Figure 2) to control the output current of the differential transmitter. Also, the current sources of version B have more current capacity them version A.

The padout of version A is similar to version B, as shown in Figure 4. The difference between both is mainly in the bias and control voltages. Also, version A does not have internal pads. Pin 1 starts in the same pad as indicated in Figure 4, and they increase counterclockwise. Below, the description of the Transceiver chip, version A padout:

1. I1: Bit 1 input to the transmitter
2. I1B: Complement Bit 1 input to the transmitter
3. I2: Bit 2 input to the transmitter
4. I2B: Complement Bit 2 input to the transmitter
5. I3: Bit 3 input to the transmitter
6. I3B: Complement Bit 3 input to the transmitter
7. I4: Bit 4 input to the transmitter
8. I4B: Complement Bit 4 input to the transmitter
9. I5B: Complement Bit 5 input to the transmitter
10. I5: Bit 5 input to the transmitter
11. I6B: Complement Bit 6 input to the transmitter
12. I6: Bit 6 input to the transmitter
13. I7B: Complement Bit 7 input to the transmitter
14. I7: Bit 7 input to the transmitter
15. I8B: Complement Bit 8 input to the transmitter
16. I8: Bit 8 input to the transmitter
17. I9B: Complement Bit 9 input to the transmitter
18. I9: Bit 9 input to the transmitter
19. DGND: Digital ground
20. O9: Bit 9 receiver output
21. D9: Bit 9 output of the transmitter
22. D9B: Complement Bit 9 output of the transmitter
23. O8: Bit 8 receiver output
24. D8: Bit 8 output of the transmitter
25. D8B: Complement Bit 8 output of the transmitter
26. O7: Bit 7 receiver output

27. D7: Bit 7 output of the transmitter
28. D7B: Complement Bit 7 output of the transmitter
29. O6: Bit 6 receiver output
30. D6: Bit 6 output of the transmitter
31. D6B:Complement Bit 6 output of the transmitter
32. O5: Bit 5 receiver output
33. D5: Bit 5 output of the transmitter
34. D5B: Complement Bit 5 output of the transmitter
35. DVDD: +5V digital power supply
36. VCN: Variable voltage that range from 0V to +5V. Should be bypassed. Tests have shown that VCN has very little influence on the single ended output, and can be disabled by connecting it to GND.
37. VCP: Variable voltage that range from 0V to +5V. Should be bypassed. Tests have shown that VCP has very little influence on the single ended output, and can be disabled by connecting it to DVDD.
38. RB_RCV: Bias for receivers, nominal 12KΩ resistor (can be variable) connected to DVDD
39. EN_RCV: When connected to DVDD enables for the receiver
40. HYS: When connected to DVDD enables the hysteresis
41. EN_XMT*: When connected to DGND enables for the transmitter
42. VBB: External voltage reference input of 1.5V. It is a high impedance input.
43. RB_XMT: Bias resistor for the transmitter, nominal 50K (can be variable up to 120K) connected to DVDD.
44. REF_P: Together with REF_N, provides the reference for the differential output current of the transmitter. A resistor should be connected between REF_P and REF_N. A resistor value of 200Ω provides an output current of approximately 6 mA, and a resistor of 12K provides an output current of approximately 2 mA.
45. REF_N: see REF_P
46. VSUB: V Substrate: Connect to DGND
47. D4B: Complement Bit 4 output of the transmitter
48. D4: Bit 4 output of the transmitter
49. O4: Bit 4 receiver output
50. D3B: Complement Bit 3 output of the transmitter
51. D3: Bit 3 output of the transmitter
52. O3: Bit 3 receiver output
53. D2B: Complement Bit 2 output of the transmitter

54. D2: Bit 2 output of the transmitter
55. O2: Bit 2 receiver output
56. D1B: Complement Bit 1 output of the transmitter
57. D1: Bit 1 output of the transmitter
58. O1: Bit 1 receiver output
59. D0B: Complement Bit 0 output of the transmitter
60. D0: Bit 0 output of the transmitter
61. O0: Bit 0 receiver output
62. DVDD: +5V digital power supply
63. I0: Bit 0 input to the transmitter
64. I0B: Complement of Bit 0 input to the transmitter

7. SUGGESTED CONNECTIONS

We will now suggest ways to connect the Transceiver chip to supporting components, for all versions of the chip: version B, Honeywell and MOSIS submissions and version A, Honeywell and MOSIS submissions. Of course, there are different ways to connect the chip to meet different requirements. For example, version B Honeywell submission provides the output voltage V_{BB} ~ 1.5V . This voltage can be used to transform the differential inputs in single ended TTL inputs, if it is connected to the negative input (I*n*B or D*n*B) of the differential inputs. The proper knowledge of the chip will enable the user to take full advantage of all its facilities.

7.1 Version B

We will now suggest ways to connect the Transceiver chip, version B to supporting components.

7.1.1 Version B, Honeywell Submission, Transceiver as a Receiver

Figure 7 shows the suggested connection. Observe that the hysteresis (HYS) can be enabled or disable depending if it is connected to +5V or GND.

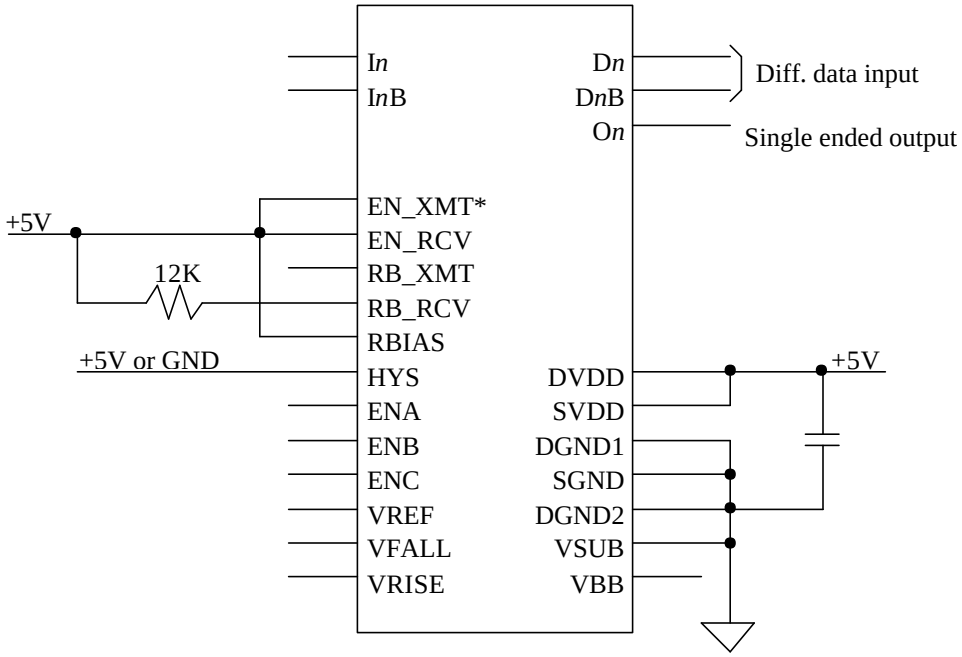
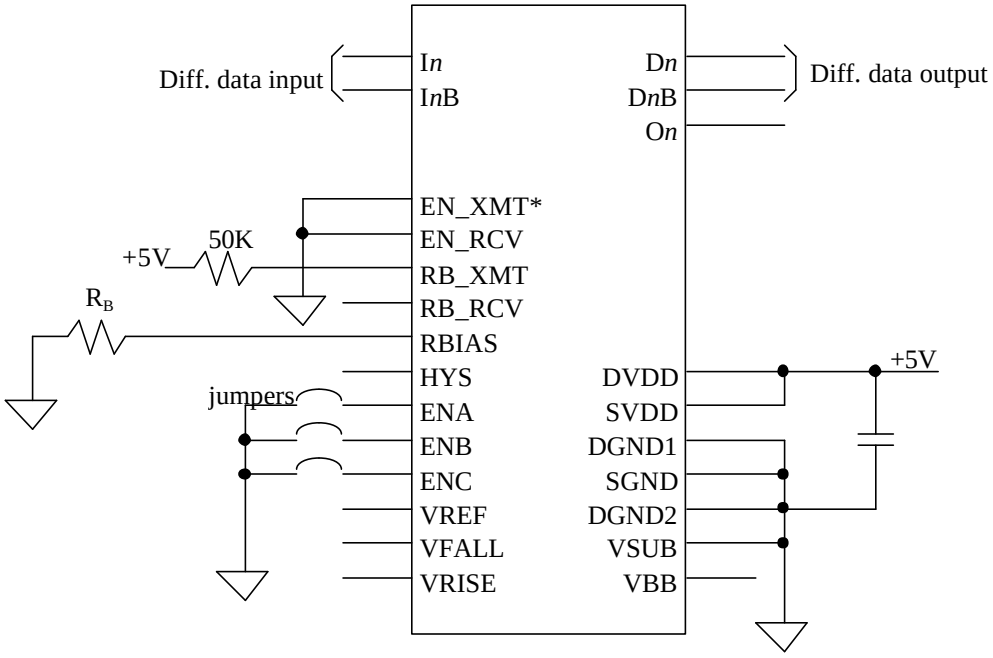


Figure 7. Version B, Honeywell Submission, Transceiver as a Receiver

7.1.2 Version B, Honeywell Submission, Transceiver as a Transmitter

Figure 8 shows the Transceiver chip operating as a transmitter. As Figure 2 shows, there are two ways to control the output current of the differential outputs: through output resistors or output current sources. Both operating modes were fully tested in the MOSIS submission and both worked very well. However, if one is using the transceiver chip in conjunction with the SVX3 chip, we suggest the use of the resistor mode. The reason is that the SVX3 chip also has a similar differential output, and it will be configured for the resistor mode. So, to keep a similar operation for both chips, the resistor mode should be used. Also, one should use one operating mode or the other, but in general should not use both at the same time. If the jumpers are being used, R_B should be removed and RBIAS connected to +5V (see Section 4). This disables the current sources. If one is using the current mode, do not assemble the jumpers, and use R_B connected to GND. The output current of the current sources is controlled by R_B (see Section 4). The common mode voltage of the differential outputs in this case is set by V_{REF}, but since it is set internally to the chip to +2.5V, and in general it should be left floating.



Note: One should use R_B or the jumpers, but not both at the same time. Read text and padout definition.

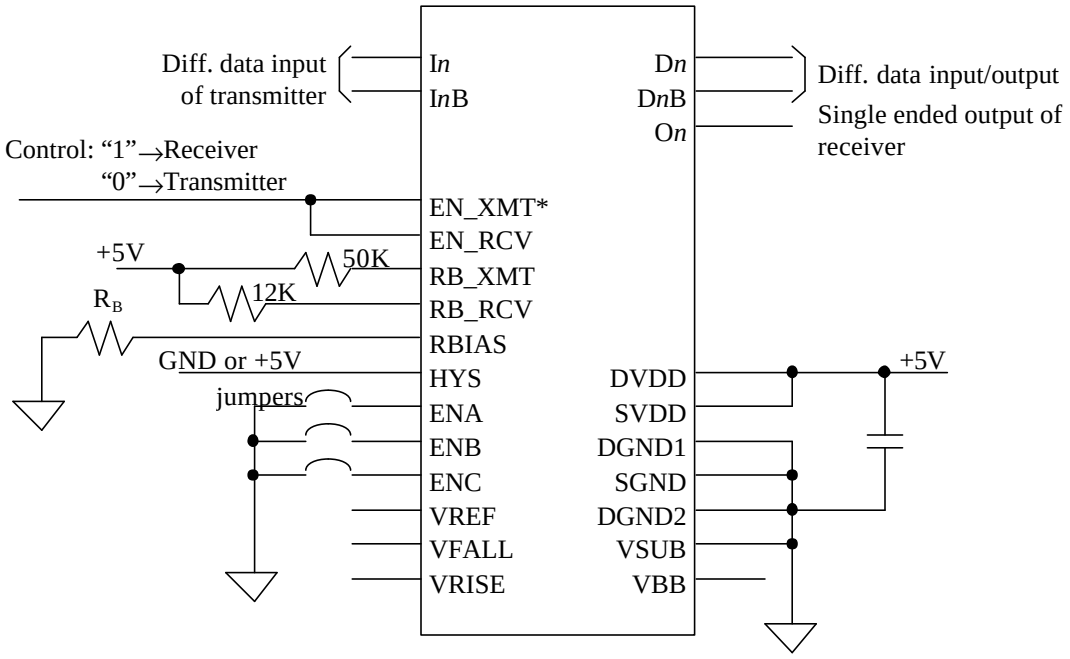
Figure 8. Version B, Honeywell Submission, Transceiver as a Transmitter

7.1.3 Version B, Honeywell Submission, Transceiver as a Transmitter/Receiver

Of course, the Transceiver can also be used as a transmitter and receiver, for bi-directional operations. This operating mode is depicted in Figure 9. All comments previously done in Sections 7.1.1 and 7.1.2 are fully applicable.

Observe that one could conceive an application where both, the transmitter and receiver portions of the transceiver are enabled and operating at the same time (EN_RCV connected to +5V

and EN_XMT* connected to GND). In this way, the differential I*n*, I*n*B inputs would directly reflect in the single ended output O*n*, and the D*n* and D*n*B should be left floating (i.e., not terminated). The advantage of this application is associated with the layout. The pads for I*n*, I*n*B are located toward just one side of the chip, in contrast with D*n* and D*n*B that are located in both sides. The chip will still operate with differential inputs (connected to I*n*, I*n*B) and a single ended output (O*n*).



Note: One should use R_B or the jumpers, but not both at the same time. Read text and padout definition.

Figure 9. Version B, Honeywell Submission, Transceiver as a Transmitter/Receiver

7.1.4 Version B, MOSIS Submission

Section 5 describes the details of version B, MOSIS submission that were corrected in version B, Honeywell submission. These details have impact on the way one connects the chip to use as transmitter, receiver and transmitter/receiver. Below we will list this changes:

a) An external voltage divider should provide $V_{BB} \sim 1.5V$. Figure 10 shows a possible set of values. Observe that the 10 nF capacitor was added.

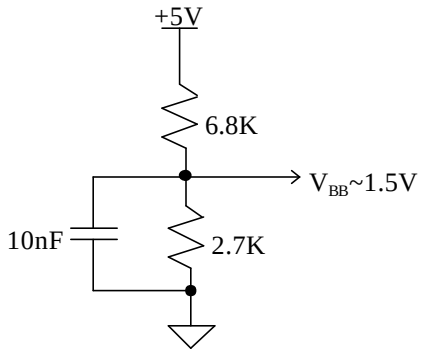


Figure 10. Voltage Divider for V_{BB}

b) Connect EN_XMT to +5V to enable the transmitter.
c) Observe that the polarity of the differential inputs of the receiver is inverted.

7.2 Version A

We will now suggest ways to connect the Transceiver chip, version A to supporting components. Observe that both, the Honeywell and the MOSIS submissions of version A require the same supporting components. Also, the same statement done for version B applies here: there are different ways to connect the chip, and meet different requirements. The proper knowledge of the chip will enable the user to take full advantage of all its facilities. Finally, note that version A requires the provision of an external V_{BB}.

7.2.1 Version A, Transceiver as a Receiver

Figure 11 shows the Transceiver chip connected to operate as a receiver. Observe that the hysteresis (HYS) can be enabled or disabled depending if it is connected to +5V or GND.

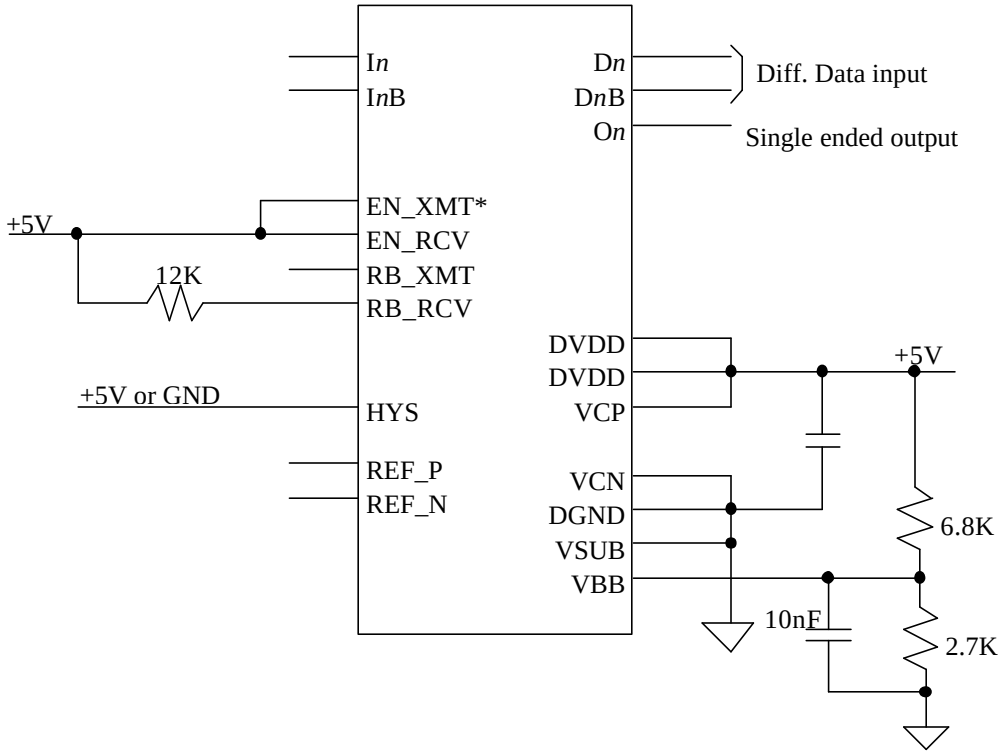


Figure 11. Version A, Transceiver as a Receiver

7.2.2 Version A, Transceiver as a Transmitter

Figure 12 shows the Transceiver chip, version A operating as a transmitter. R_C provides the reference for the differential output current of the transmitter. A 200Ω resistor provides an output current of approximately 6 mA, and a 12K resistor provides an output current of approximately 2 mA. Contrasting with version B, there is no control over the common mode voltage.

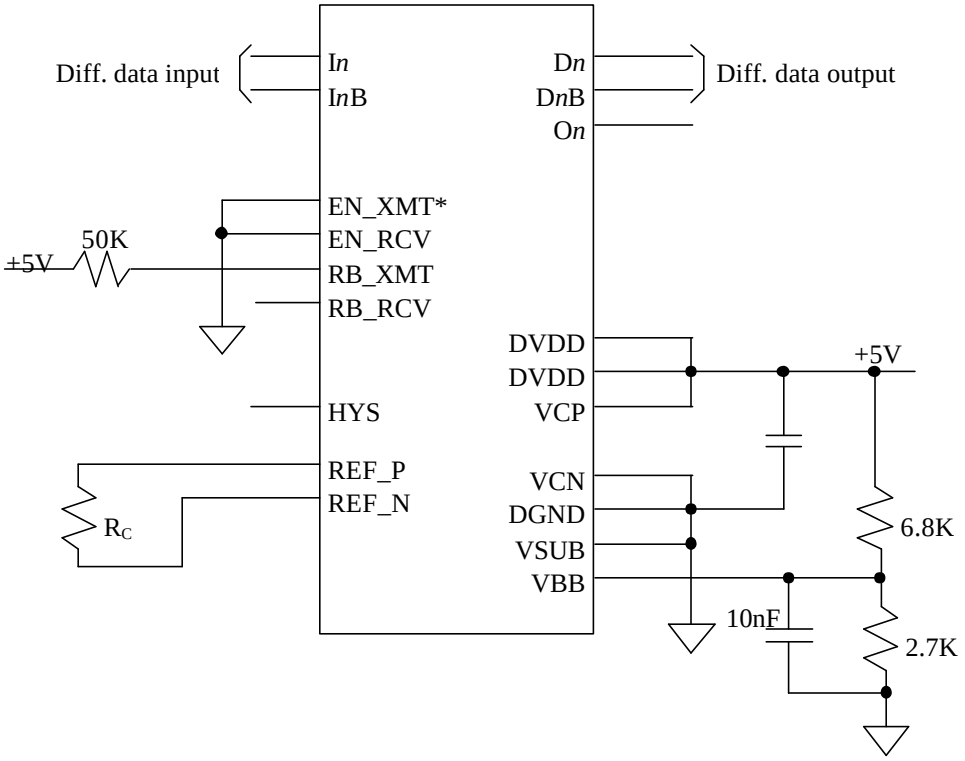


Figure 12. Version A, Transceiver as a Transmitter

7.2.3 Version A, Transceiver as a Transmitter/Receiver

Figure 13 shows the Transceiver chip connected to operate as a transmitter/receiver. All comments previously done in Sections 7.2.1 and 7.2.2 are fully applicable.

For the same reason discussed in Section 7.1.3, one may need to use the Transceiver operating as a transmitter and receiver at the same time. For this, EN_RCV should be connected to +5V and EN_XMT* to GND.

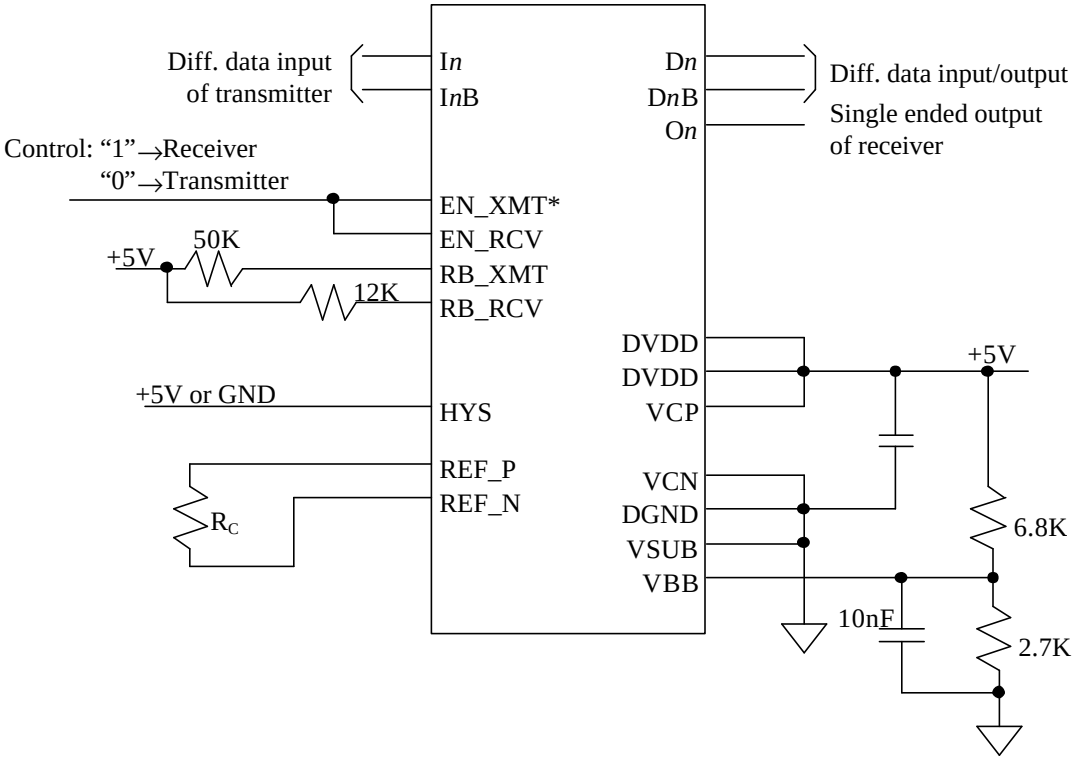


Figure 13. Version A, Transceiver as a Transmitter/Receiver

8. REFERENCES

[1] Zimmemann, S., "Port Card for the SVX-III Chip", Fermilab note.

[2] Woodbury, K., "Fiber Interface Board", Fermilab note.

[3] Strohmer, R. and Knopf, W., "Device Specifications for the SVX-III Readout Chip", Fermilab note.

[4] Barsotti, E., Zimmermann, S., "Low current differential signals", Fermilab note.

[5] Foor, J., "Ten Bit Differential Transceiver Testing," Fermilab note, August 1998.