6 Modules

6.1 Overview

The sensitive area of $\sim$1.7 m^2 of the ATLAS pixel detector is covered with 1744 identical modules, independent of their spatial position, with a small exception (see below). Each module has an active surface of $6.08 \times 1.86\,\mathrm{cm}^2$. A module is assembled from the following parts

- the sensor tile containing 47232 pixels as described in section 5
- sixteen front end electronics chips (FE) each containing 2880 pixel cells with amplifying circuitry, connected to the sensor by means of fine-pitch bump bonding (see section 6.2)
- a 50 μm thick, fine-pitch, double-sided, flexible printed circuit foil to route signals and power
- a module control chip (MCC) situated on the flexible printed circuit foil
- for the barrel modules, another flexible foil, called a pigtail, that provides the connection to electrical services via a micro-cable ; for the disk modules the micro cables are attached without the pigtail connection (see section 8.5 for a description of the microcables).

The concept of the ATLAS hybrid pixel module is illustrated in Figure 1. Sixteen front-end chips are connected to the sensor by means of bump bonding and flip-chip technology. Each chip covers an area of $0.74 \times 1.09\,\mathrm{cm}^2$ and has been thinned before the flip-chip process to $\approx$190 μm thickness by back-side grinding. A sizeable fraction ($\approx$25%) of the front-end chip is dedicated to the End of Column (EoC) logic. Once bonded, most of the EoC logic extends beyond the sensor area. Wire bonding pads at the output of the EoC logic are thus accessible to connect each front-end chip to the flexible-hybrid kapton foil by means of aluminum-wire wedge bonding. Copper traces on the foil route the signals to the MCC. The MCC receives and transmits digital data out of the modules. The flex-kapton circuitry is also used to distribute decoupled low voltages to all chips. The traces are dimensioned such that the voltage drop dispersion on the flex-circuit is limited to $\approx$50 mV in order to keep all chips in the same operating range. The flex-circuit substrate material must have a low pin-hole probability, as it also contains high voltage ($\approx$600 V) traces for the sensor bias. The kapton material must not degrade after the LHC irradiation dose(500 kGy). Passive components are added to the flex-hybrid for decoupling and filtering of the front-end chips.

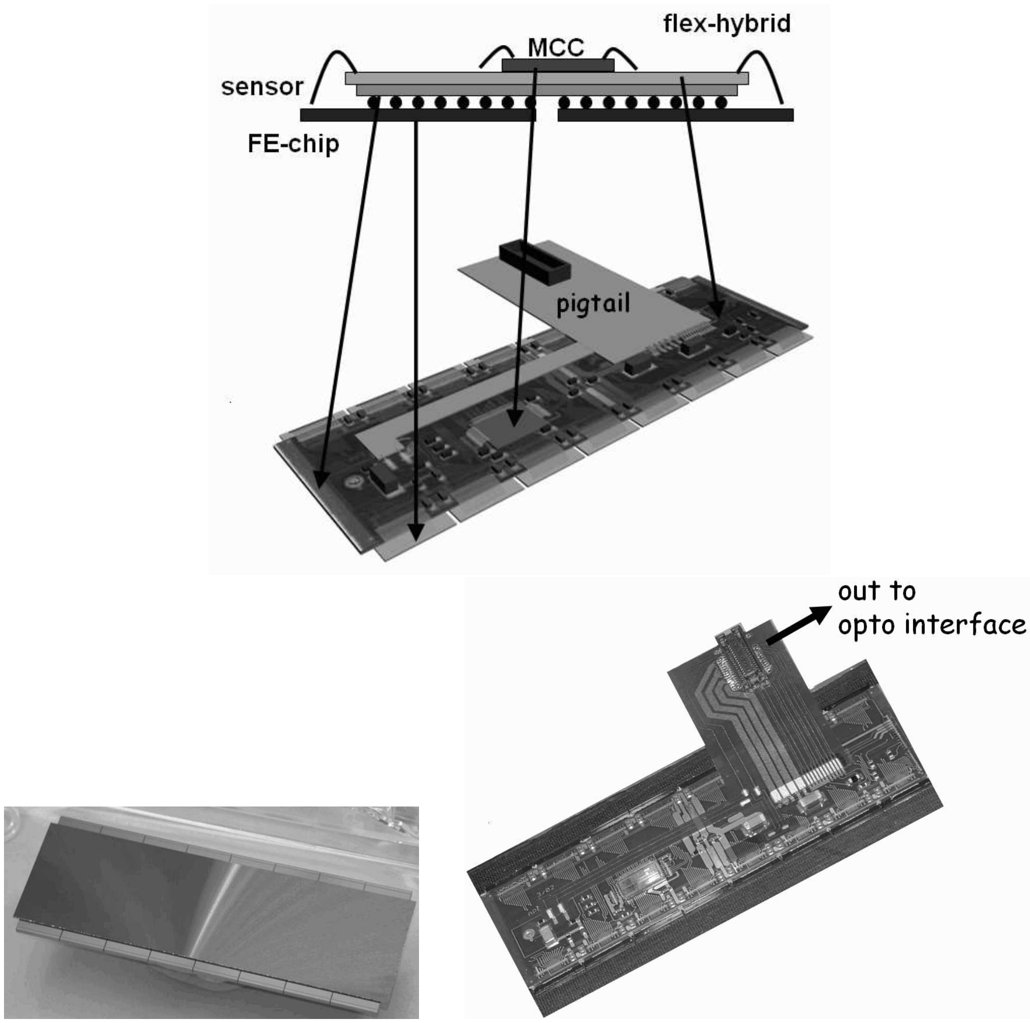

Figure 1: The barrel pixel module. (top) overview, showing the components of the module assembly: sensor, FE-chips, Flex-kapton-hybrid, module controcl chip (MCC), pigtail. (b) photograph of a bare module, (c) photograph of a fully assembled module.

The module temperature is remotely monitored via a Negative Temperature Coefficient (NTC) resistor placed on the kapton circuit, and a fast interlock powers off a module when overheating occurs.

A complete module draws 1.2 A at 1.6 V from the analog supply and 0.8 A at 2 V from the digital supply or about 3.5 W per module. This value is expected to increase to about 5 W after an accumulated dose of 500 kGy.

The bump bonding and flip-chip operation results in a so-called bare module. The sixteen chips of an assembled module are first tested on a probe station to detect defects such that rework on a module can be done at this point of the assembly sequence.

Region in between Chips

The sensor pixels have dimensions of $50\,\mu\text{m}\times400\,\mu\text{m}$, except for 11% which have a size of $50\,\mu\text{m}\times600\,\mu\text{m}$, to allow for a contiguous sensitive area between chip boundaries in the long pixel direction. In the perpendicular direction, two times four pixels under each of the two adjacent chips cannot be covered by active pixel circuitry. These off-side sensor pixels are connected through metal lines on the sensor to 4 + 4 neighboring electronics pixels at the top of the columns in addition to the cells which lie directly underneath as is illustrated in Figure 2. The resulting hit ambiguity is resolved by the off-line pattern recognition software. These special pixels (inter-ganged pixels)- the 600 μm size (long pixels), the pairs connected to a single readout channel (ganged pixels) and the ones below the metal line connecting two ganged cells - have slightly degraded electrical performance due to the increased sensor capacitance (see section 6.6).

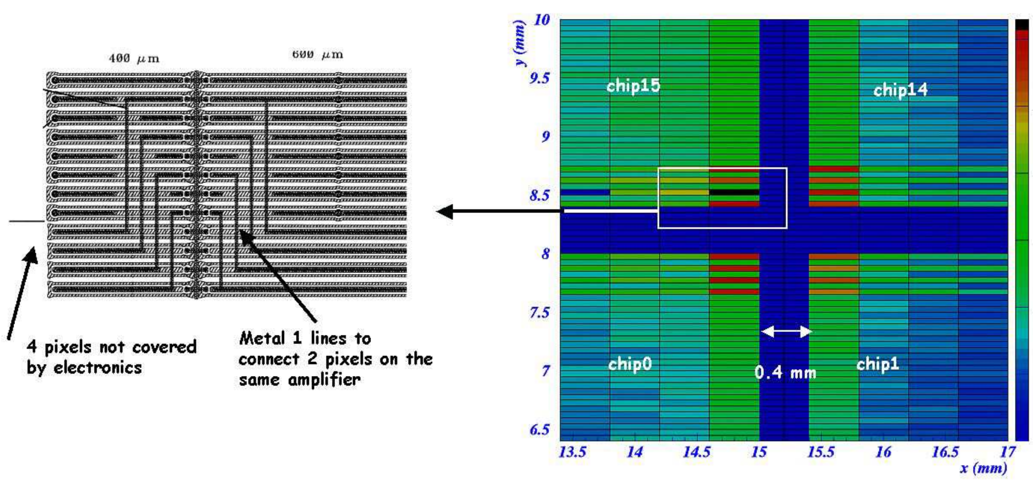

Figure 2: End region of the pixel detector at the edge of four FE-chips. The area of the sensor covered by the chip edges is marked in grey. The pixels in between the chips (white rectangles) are connected through metal lines to another pixel underneath the chips.

6.2 Bump Bonding

Bump bonding is extensively used in the electronics industry for the attachment of integrated circuit die to printed circuit boards or other substrates. Two different bump bonding techniques have been used for ATLAS: electroplated-solder(PbSn) bumping [1, 3] and evaporative - indium bumping [4]. Both bump deposition processes are done at the wafer level. The principle of a bumped sensor – electronics pixel element is sketched in Figure 3. The substantial demands on the handling

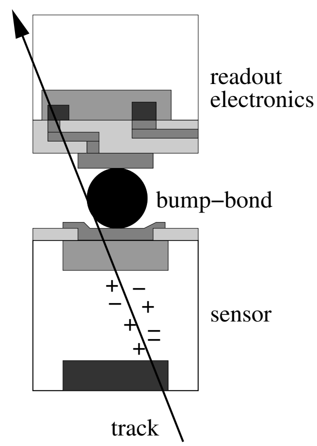

Figure 3: Blow-up sketch (not to scale) of the cross section of a hybrid pixel detector, showing one connection between a sensor and an electronics pixel cell. A particle track releases ionization in the sensor volume

require that the wafers get bumped with their original thickness ($\sim 700\mu m$ for the 20 cm integrated circuit wafers). Wafer thinning is done after bump deposition by covering the bumps with a photoresist layer and a UV releasing tape for bump protection and for handling. The integrated circuit wafers are then thinned by backside grinding to about 190 μm. They are diced immediately afterwards and then the die are tested again on a probe station to assure that they are still functional and ready for the flip-chip process.

6.2.1 The Solder Bumping and Bonding Process

In eutectic PbSn solder bumping [1, 3], the solder is deposited through electroplating. Under bump metallization (UBM), which consists of several metal layers is deposited on the contact pads. A PbSn cylinder is galvanically grown and melted to a sphere on the integrated circuit wafer, while the sensor wafer receives only the UBM [2, 5]. The parts are mated by flip-chipping with reflow which provides self-alignment. The process flow is described in [8]. The distance between chip and sensor is about 20 – 25 μm, thus minimizing the cross-talk between the electronics and sensor. The connection resistance is smaller than 1Ω and the ultimate shear stress is $\approx$50 MPa. A pictures of PbSn bumps after reflow on an ATLAS FE-chip are shown in Figure 4.

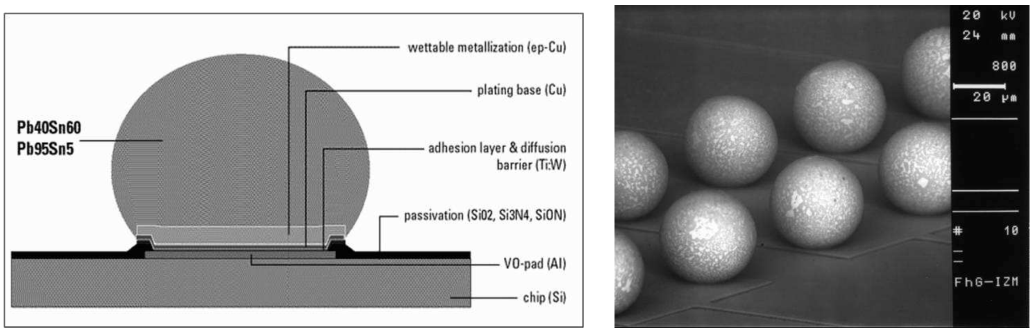

Figure 4: left) Schematic description of a eutectic PbSn solder bump [1, 3], (right) rows of a PbSn bumps (courtesy IZM-Berlin).

6.2.2 The Indium Bump Bonding Process

In the case of indium bonding, the bumps are grown by depositing evaporated indium on both mating parts [6].The bump pitch is also 50 μm, but the bump height is limited to 10 μm due to the use of a lift-off process for the removal of the polyimide evaporation mask. Bumps are deposited both on the sensor and on the electronics wafers. Mating is obtained by In-In thermocompression. The process flow is described in [8]. Figure 5 shows a micrograph of 50 μm pitch indium bumps deposited on two glass samples and then flip chipped together [4] at a temperature of $\sim$100°C applying a pressure of about 20 N/cm^2 per chip. The distance between chip and sensor after bonding is $\approx$10 μm.

6.3 Quality Control of Bump Bonded Assemblies

Inspections before and after flip-chip assembly are crucial to obtain the highest yield for functional pixel modules. Automated inspection of bumped wafers with the combined use of a television camera and laser interferometry allowed the manufacturer to find missing bumps, merged bumps,deformed bumps or other defects as well as to measure bump heights on wafers. Inspection with high resolution (2 μm) X-ray machines allowed one to detect misalignment or merged/bridged bumps previously not detected or caused by the flip-chip process. Both solder

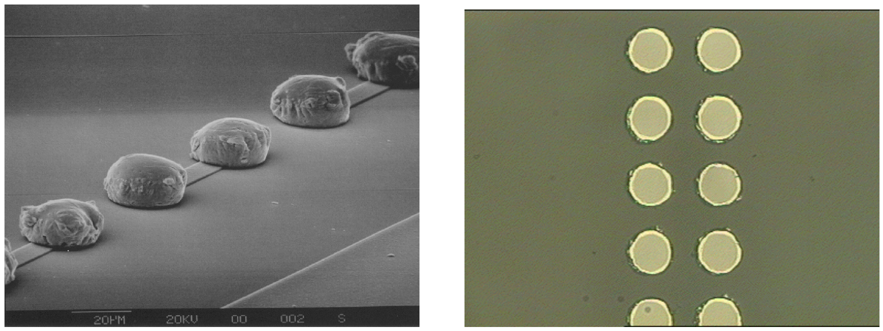

Figure 5: Micrograph of a Indium bump deposition on Silicon at 50 μm pitch (left) and of a flip-chip assembly of two 50 μm pitch bump arrays (right) on glass substrates (courtesy SELEX Sistemi Integrati, Rome) [4]

and indium bump bonding have been used to produce more than 2000 pixel modules by two different manufacturers with bump defect rates of $\approx 10^{-5}$–10^{-4} at the wafer level and $\approx 10^{-4}$–10^{-3} after the flip-chip process.

6.4 Reworking of Bump Bonded Assemblies

All modules were built with known good die (KGD), i.e. all die were tested prior to flip-chip and only the good ones are used. This is a crucial requirement as the module yield goes with the n^{th} power of the electronics chip yield, n being the number of chips per module.

All front-end chips were also electrically tested after bump bonding, in order to check for damage to the front-end electronics and to assess if the quality of the electrical contact is not adequate.

Both solder and indium bump bonded modules presenting have been successfully reworked [5, 7] with a success probability of more than 95%. In both cases, the operation requires heating and application of a force to remove the integrated circuit, while leaving some metal on the bond pads. Afterwards, a new IC is flipped to the sensor. The probability to properly connect all pixels in the second flipping is near 100%.

6.5 Module assembly

Once a bare module has passed the acceptance test, it is equipped with a flex-hybrid to provide the connections between the Module Controller Chip and the front-end electronics and from the Module Controller Chip to a microcable. A photograph of a barrel module is shown in Figure 6.

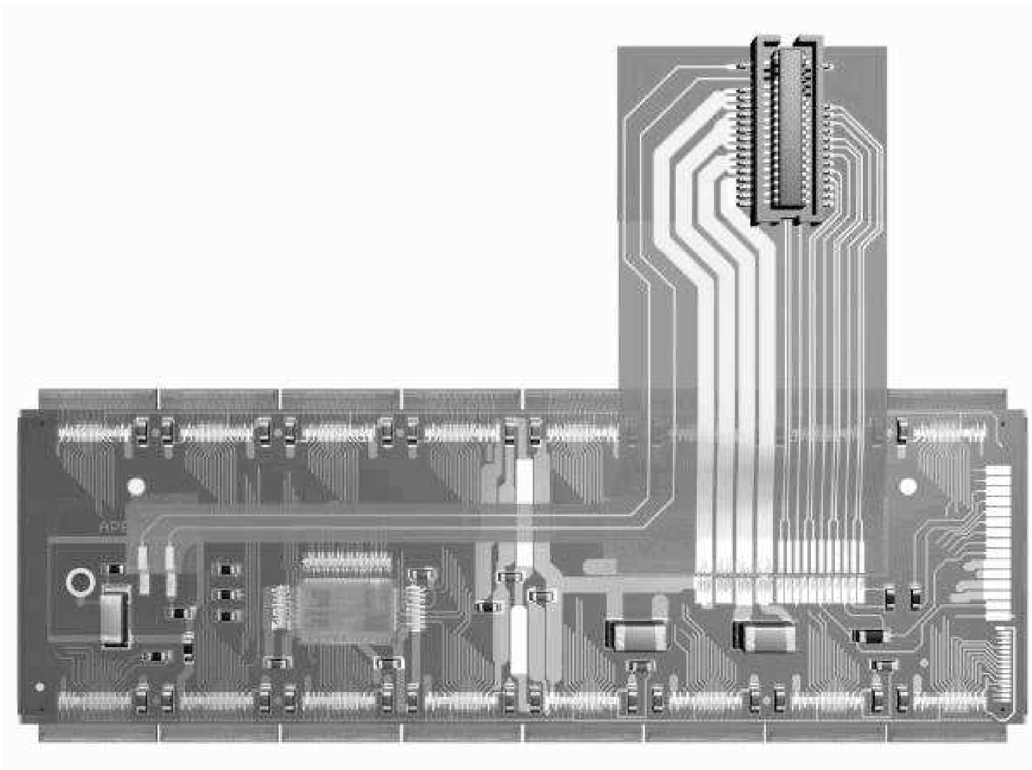

Figure 6: Picture of an ATLAS pixel barrel module

The flex-hybrid is a double-sided, flexible printed circuit with a 50 μm substrate thickness and 25 μm thick copper lines, (Manufactured by Dyconex AG (Bassersdorf, CH). It has been specifically designed to cope with the maximum 600 V depletion voltage applied to the sensor. It also includes passive components for local decoupling and an NTC for monitoring the module temperature.

To facilitate testing of flex hybrids, they are attached to a custom-made printed circuit boards (flex support card or FSC), which were used for handling of the flex-hybrids themselves and after attaching the hybrid to a module. A module is cut out from the FSC just prior to loading on a local support.

Flex hybrids for barrel and disk modules are identical. A difference appears only when the connector for the link to the services is attached. For barrel modules, an additional flex circuit (pigtail) is glued on top of the flex hybrid and electrically connected by wire bonding. It has a zero-insertion-force connector which is fixed to the back side of the stave and used for attachment of the low-mass. Type-0 microcables. Disk modules instead use thin copper wires for the Type-0 microcables that are soldered directly to the flex hybrid.

There is a significant difference in the coefficient of thermal expansion between kapton and silicon. The glue used for attachment of the flex hybrid to the bare modules needs to be distributed to avoid any excessive mechanical coupling between the two. On the other hand, a strong connection is required in the places where wire bonds are needed. Therefore, the glue (Dow Corning SE4445)1 is deposited along the pads lines used for the interconnection between the flex hybrids and the front-end electronics, below the MCC, near the high voltage bonding pad and, for barrel modules, below the pigtail attachment point.

6.6 Testing and Selection Procedures

After loading on a FSC, a module can be connected to a test setup using cables. The test setup in the laboratory uses LVDS signals. The readout chain and control software is the same as that used for the front-end electronics and bare module testing, except now configured to communicate via the MCC and uses the micro-cable instead of probe needles for communication with the integrated circuits.

The characterization procedure [9,10] aims to certify if a module is acceptable for operation, both electrically and mechanically. A ranking value is determined such that better modules can be selected for the most critical parts of the detector. In particular, a module must satisfy the following conditions:

- the electronics should be tunable and have enough operation range to guarantee there will be tuning capability to operate even after radiation damage;
- the bump bonding has not been damaged by the assembly procedure;
- the wire bonding of MCC and FE is done correctly.

The testing sequence proceeds as follows:

1. a basic series of electronics tests is performed at room temperature after module assembly;
2. modules undergo a mechanical stress test, being cycled 10 times between room temperature and -30 °C, with a cycle length of about 2 hours;
3. electronics tests at room temperature are repeated after thermal cycling and compared to the initial tests;
4. a complete module characterization is performed at about -10 °C, which is the expected operating temperature.

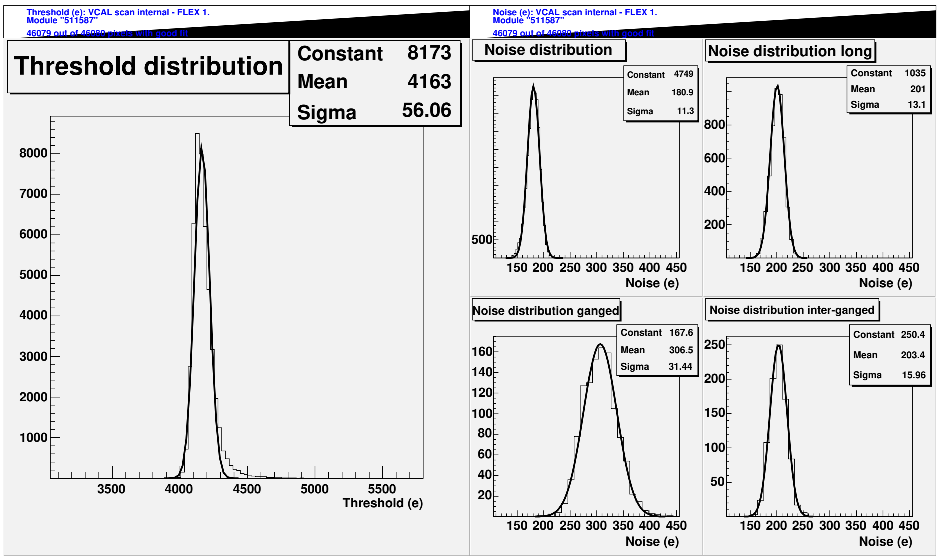

Figure 7: Threshold (left) and four noise (right) distributions - for different locations and types/sizes of pixels - of a typical module (normal, long, ganged, inner-ganged). The thresholds are uniform for the entire modules.

The last test is the most relevant for the definition of module quality and selection for usage in the detector. Reduced electronics test are also performed after loading of modules into the local supports, to monitor possible damage after loading, which may trigger the repair or replacement of a module.

The room temperature tests consist of:

1. a basic functionality test: the module is configured, the readout chain is tested by the digital injection and the amplifier cells by the analog injection;
2. a test of module tunability: thresholds are equalized to about 4000 e; and
3. a threshold scan without depletion voltage applied to the sensor.

The first test is mainly a check of the wire bonding or for forelectrostatic discharge damage to the electronics. In the second test, pixels can usually be tuned to the target threshold with a dispersion of 60 e, and a noise which ranges between 120 e for standard pixels to 300 e for long and ganged pixels (see Figure 7).

The second and third tests are also sensitive to bump bonding properties. Pixels that fail the tuning usually correspond to a cluster of merged bumps. In this case, several cell amplifiers are shorted together, resulting in reduced sensitivity to the injected pulse. In the case of an undepleted sensor, instead, normal pixels are affected by the large parasitic capacitance of the sensor, but pixels not connected to the detector stand out because the noise level remains low, independent of the bias voltage applied to the sensor side. Examples of modules with such defects are shown in Figure 8.

The test of modules before and after the thermal cycles has been of importance. A problem in the potting of wire bonds on the MCC was found, which resulted in unreliability of the wire bonds, which was corrected during the production. The comparison of bump damage between the initial assembly and after thermal cycling, allows one to disentangle damage due to bad handling during the assembly, and damage due to weak bump bonds, for which there is a steady increase of disconnected bumps with time. The full characterization at the nominal operational temperature of -10 °C included additional checks of tunability and operational range:

- the MCC operation was checked between 1.6 and 2.5 V, showing a typical turn-on at 1.8 V.
- front-end IC operation was tested within wide ranges of analog and digital low voltage supply values (VDDA 1.5-2.0, VDDD 1.9-2.3).
- The amplifier feedback current was tuned so that the average ToT response to a minimum ionising particle corresponded to 30 clock cycles: with the LVL1 trigger latency expected during operation, this setting provided 99.5% efficiency in a test beam [11]
- Timing measurements have been performed to check the timewalk performance of the FE electronics when attached to the sensor. The overdrive needed to assign a signal to the correct beam crossing is about 1000 e.
- A measurement with the 60 keV X-ray from an ^{241}Am source checked the sensors's response(see Figure 8).

The source measurement is especially relevant in assessing module quality, since, being self-triggering, it is very sensitive to noisy channels. The duration of the measurement is chosen to reach an expected occupancy of at least 10 hits in every pixel channel. Therefore it is also very effective in uncovering inefficient cells, due to merged or disconnected bumps.

The number of dead channels determined by the source test is the first entry in a ranking function which has been chosen in order to evaluate module quality. Besides defective channels this function includes:

- a χ^2-like term, describing how the analog performance of a module differs from the average one;

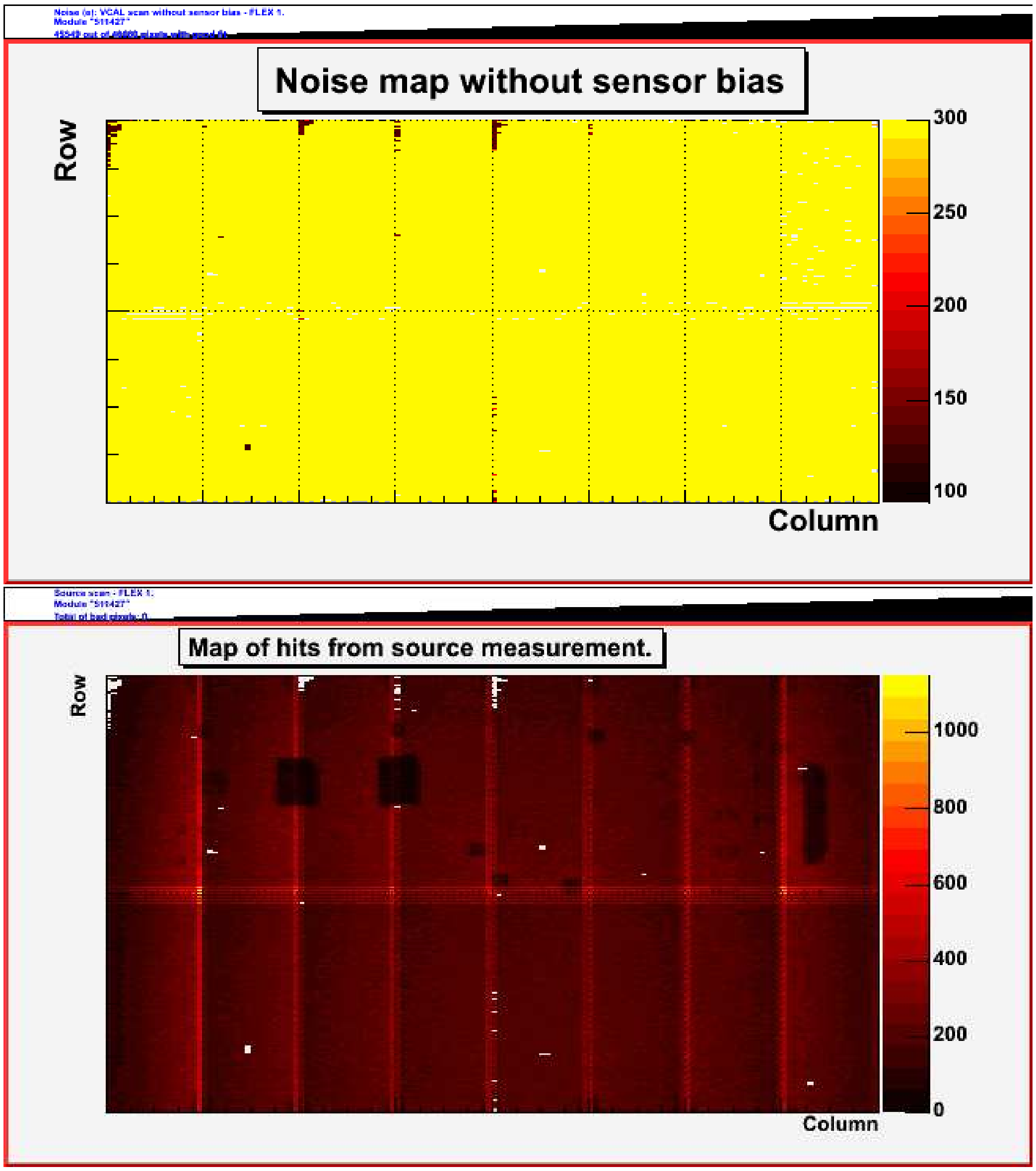

Figure 8: Noise distribution for an indium-bumped module without sensor bias (top). Disconnected regions are visible as low noise spots. For comparison below is a hitmap obtained with an ^{241}Am source.

- penalties for anomalous values of the leakage current or module bowing, which may give problems during operation;
- penalties for any repair operation performed on the modules.

This ranking function was used for module selection for further assembly. The distribution of the ranking function is displayed in Figure 9. The bump in the ranking distribution around 300 corresponds to the set of modules that needed a full rebonding of the MCC, because of the potting problem mentioned above. The B-Layer has been built using modules with penalty lower than 60, corresponding to a channel inefficiency better than 0.13%. Modules with penalties higher than 1000 were not accepted for assembly.

Analysis of the ranking showed an overall equivalence of all the assembly sites, while pointing out a clear difference between the two bump vendors. The main reason for the difference is the higher number of disconnected bumps in the In-bumped modules. As stated before, a clustered set of disconnected bumps may be the seed for a widening of a disconnected region. Because of this, a ranking penalty was added for each FE chip containing more than 30 disconnected bumps.In hindsight this penalty has been found to be quite conservative, but it is the main reason for the tails in Figure 9.

During the final phase of module production, when it was clear that there were a sufficient number of spare bare modules, only the ones with clusters of less than four disconnected bumps were selected for module assembly, resulting in an improvement of the module ranking.

6.7 Production Yield

The production yield of bare modules is summarized in Table 1. Most losses were due to sensor damage, bad bumping and front-end IC damage.

Sensor damage usually is detected by an early breakdown voltage in the sensor tiles previously passing the sensor quality cuts. This loss rate was similar for both bump vendors and results in about 3% of the modules being rejected.

Bad bump bonding and FE damage were repairable according to the reworking procedures outlined previously. The failure rate and the possibility of reworking differed between the two bump vendors. In the case of bump problems, the solder-bump vendor often performed internal reworking after the in-house X-ray inspection, reprocessing the bumps. For indium bumps, there was no possibility to reprocess the bump deposition. In this case, if the damage was too widespread, the module was not submitted for reworking. This resulted in an overall higher failure rate for indium bumping.

FE damage was due to silicon shards trapped between the sensor and the FE chip, which, during flip-chip break the surface of the FE chips, resulting in shorts

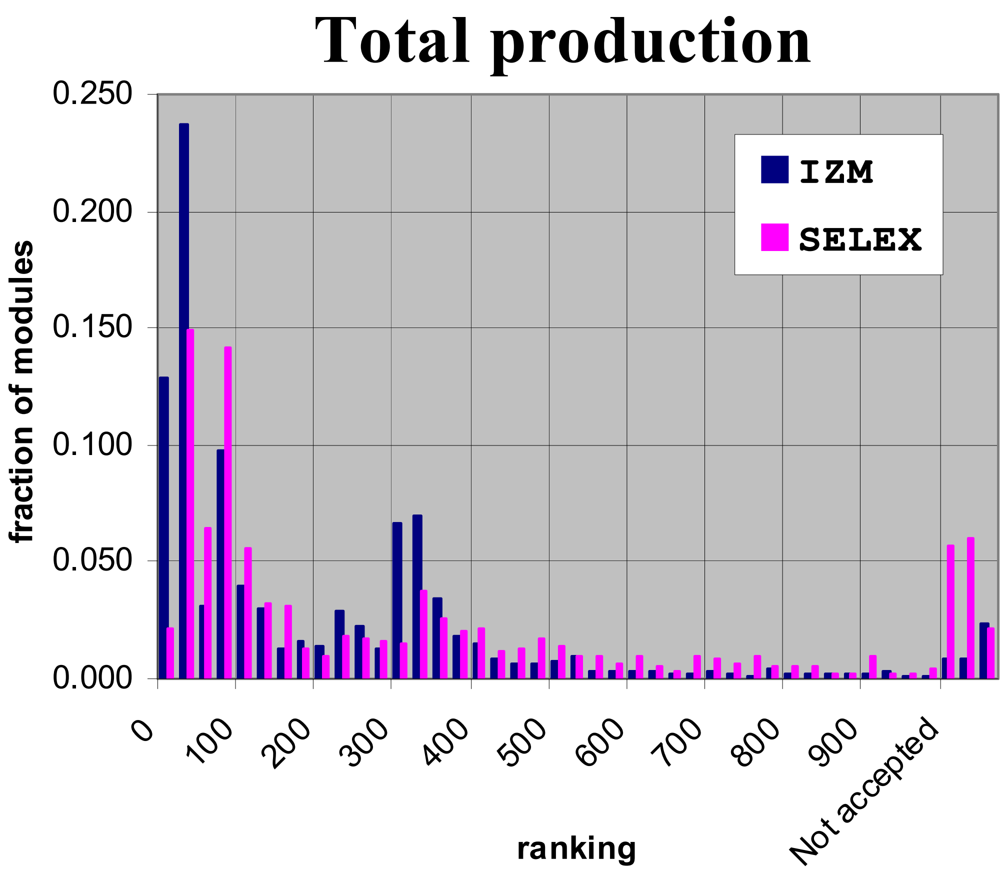

Figure 9: Module ranking distribution as described in the text.

	Indium		PbSn		Total	
	modules	**yield**	**modules**	**yield**	**modules**	**yield**
Assembled	**1468**		**1157**		**2625**	
Rejected	**172**	**11.7%**	**35**	**3.0%**	**207**	**7.9%**
Accepted	**1296**	**88.3%**	**1122**	**97.0%**	**2418**	**92.1%**
as delivered	1101	75.0%	1035	89.5%	2136	81.4%
after reworking	195	13.3%	87	7.5%	282	10.7%

Table 1: Bare module production yield.

between the metal layers. The problem was much more severe for indium-bumps, given the smaller bump height. Replacement of the FE chip usually resolved the problem, but manually removing the shards from the detector surface was needed to reach a good rework efficiency. The production yield of assembled modules is summarized in Table 2.

Modules which did not complete the testing were usually due to mechanical damage observed after the assembly procedure, either induced by handling or because of weak parts which had passed the previous quality control steps.

Modules containing one or more FE which could not be operated were also discarded from the production path. A loss of about 1% was due to defects in the path from the MCC to the FE through the flex hybrid. For Indium-bump modules, the additional yield loss is due to shorts on the FE, similar to the behavior observed on bare modules. These defects are concentrated on reworked modules and modules that underwent multiple shipments. They can be assumed to be the same defect of shards as seen on bare modules, which is not present after the initial bonding, but is finally produced by the additional mechanical stress in the module assembly.

Besides these two classes, all the other modules the operational, and a ranking is used to select the best ones. The difference in the ranking distribution between the Indium and solder bump modules is mainly due to regions of disconnected bumps, discussed in section 6.6.

Overall the yield for module production exceeded the target, which was 90%, for each step in the bare module assembly, and the full module assembly and characterization.

References

[1] O. Ehrmann, G. Engelmann, J. Simon, H. Reichl
A Bumping Technology for Reduced Pitch. In: *Proc. Second International TAB Symposium*. San Jose, USA, 1990, S. 41–48

	Indium		PbSn		Total	
	Modules	**Yield**	**Modules**	**Yield**	**Modules**	**Yield**
Assembled	**1190**		**1122**		**2312**	
Accepted	**1025**	**86.1%**	**1075**	**95.8%**	**2100**	**90.8%**
B-Layer quality	281	23.6%	445	39.7%	726	31.4%
not B-layer quality	744	62.5%	630	56.1%	1374	59.4%
Not accepted	**165**	**13.9%**	**47**	**4.2%**	**212**	**9.2%**
Ranking¿1000	68	5.7%	10	0.9%	78	3.4%
at least one dead FE	71	6.0%	10	0.9%	81	3.5%
could not complete testing	26	2.2%	27	2.4%	53	2.3%

Table 2: Assembled module production yield

[2] J. Wolf,
PbSn60 Solder Bumping by Electroplating. In: *Pixel 2000 Conference, Genova, Italy*, June 2000. – http://www.ge.infn.it/Pix2000/slides.html

[3] J. Wolf, G. Chmiel, H. Reichl,
Lead/Tin (95/5 %) solder bumps for flip chip applications based on Ti:W(N)/Au/Cu underbump metallization. In: *Proc. 5th Intl. TAB/Advanced Packaging Symposium ITAP*. San Jose, USA, 1993, S. 141–152

[4] A.M. Fiorello,
ATLAS bump bonding process. In: *Pixel 2000 Conference, Genoa, Italy*, June 2000

[5] T. Fritzsch et al., Experience in fabrication of multichip-modules for the ATLAS pixel detector. In: *Nucl. Inst. and Meth.* A565 (2006), S. 309–313

[6] G.L. Alimonti et al.,
Analysis of the production of ATLAS indium bonded pixel modules. In: *Nucl. Inst. and Meth.* A565 (2006), S. 296–302

[7] G.L. Alimonti et al.
Reworking of Indium bump bonded pixel detectors. In: *Pixel 2002 Conference, Carmel (CA), USA*, Sept. 2002

[8] L. Rossi, P. Fischer, T. Rohe, N. Wermes
Pixel Detectors: From Fundamentals to Applications,
Berlin, Heidelberg : Springer, 2006

[9] C. Gemme, Production of the ATLAS pixel detector modules, Nucl. Instr. and Meth. A560 (2006) 71-74

[10] J. Grosse-Knetter et al., Experience with module production and system tests for the ATLAS Pixel Detector

[11] A. Andreazza for the ATLAS Pixel Collaboration, Developments of the ATLAS pixel detector, Nucl. Instr. and Meth. A535 (2004) 357-361