DEC Data Acquisition Status

Monsoon and the SNAP CRIC Chip

Jon Thaler

Fermilab, Jan. 22, 2004

Some issues

Monsoon is both a DAQ framework (a set of specifications) and an instantiation (hardware and software).

- Is the framework sufficiently flexible to accommodate our anticipated needs (*e.g.*, wavefront sensors)? If so, we'll only need to redo some instantiations, not start from scratch.
- Does the existing hardware and software (especially the DHE) meet our needs (space, power, noise, speed)?
- Can the framework accommodate SNAP's CRIC chip? If so, what HW/SW would we have to redo?

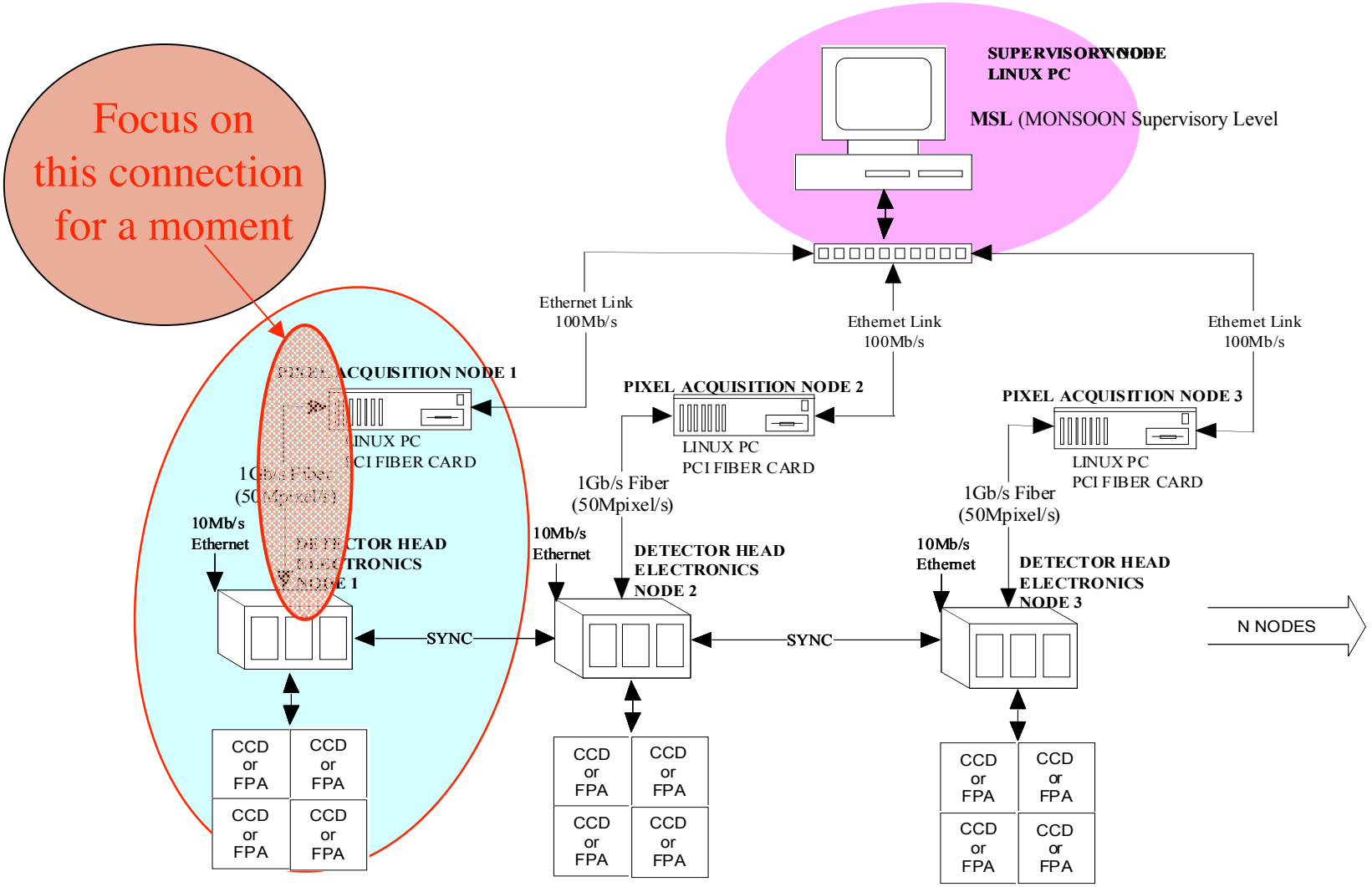
Crude specs

(updated since December)

Assume: (I'm trying to be conservative)

- 79 CCDs@ 2k×4.6k with 2 amps and ADC's (*i.e.*, 158 channels)
- 250 kHz pixel digitization rate ⇒18.4 s per CCD. (!)
- 2 bytes per pixel ⇒ 1.5×10^9 bytes per image
- 4 DHE crates (48 channels each) (34 spare channels)
- Exposure time > 60 sec (< 0.4 TB/night)
  - Dead time < 30%. (worst case)
  - <data rate> (DHE→PAN) < 50 Mbps/fiber (4 fibers)

MONSOON Pixel Server



Nick Buchholz (12/1/03)

Our Short Term Plan

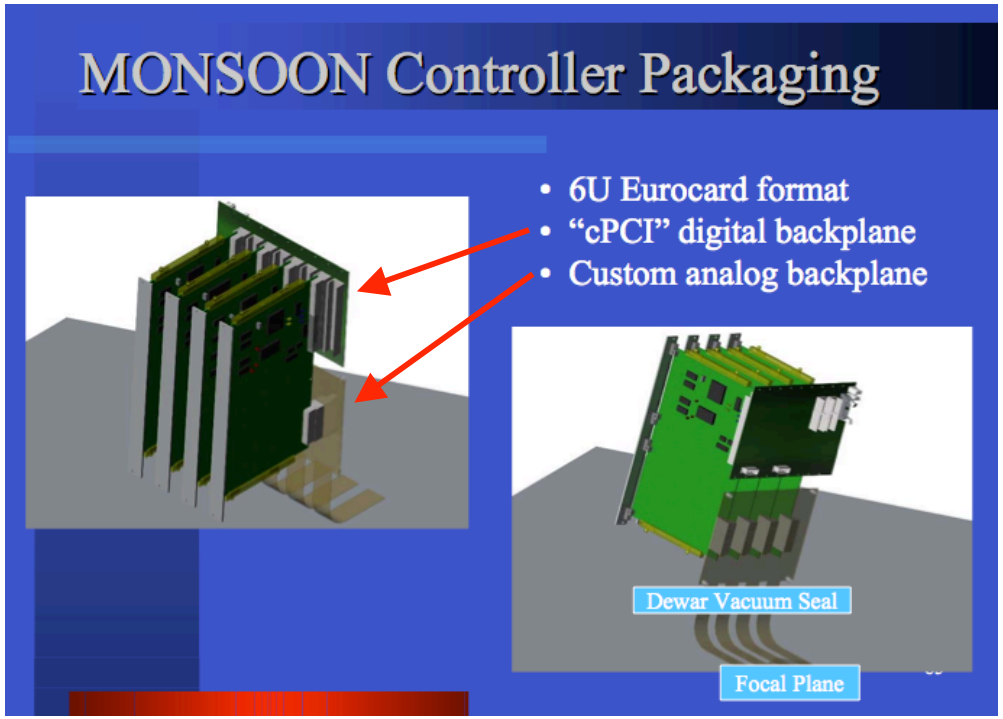
- Get the PAN software.
  We hope this is (close to) production DAQ SW.
- Get DHE emulation SW.
  We anticipate extensive revisions.
- Get a Systrans fiber communications link.

The SW was just made available to us by NOAO yesterday.
The fiber link is ordered $\Rightarrow$ 1st or 2nd week in Feb.

Can study the protocols with two PCs (A test setup exists.)
Use ethernet until the fiber arrives.

In the DHE Crate

(Physically, a 6U VME crate, but has only 8 slots)



- One Master Control Board Communicates with the PAN. (one fiber)
- One Clock/Bias Board. Can it accommodate SNAP's n-type chips?
- ≤ 6 Acquisition boards. ADC's reside here in the current implementation.

- Several crates can be synchronized by one MCB.
- CPU and FPGA implementations both exist. Do we need a CPU?

NEWFIRM Money and Power

(Mark Hunten's presentation at 12/1/03 Monsoon Status review)

Quantity	Item	Cost (est.)
1	Chassis & Backplane	$5k
1 set	Power Supplies	$1.3k
2 + 1	Master Control Board	$3.9k
1 + 1	Clock & Bias Board	$8k
8 + 1	**IR Acquisition**	**$73.8k**
2 + 9	Transition Cards	$1.6k
2 sets	SL100 (DHE & PAN)	$10k
1	PAN PC	$3k
	Total	$107k

8 channels each

Qty	Board	@Watts	Total
2	MCB	7.5	15
1	CBB	8	8
1	CBB Transition	5	5
8	**IR Acq**	**11.25**	**90**
8	IR Acq Transition	3	24
1	Power supplies (75% eff.)		35
	Total dissipated		177

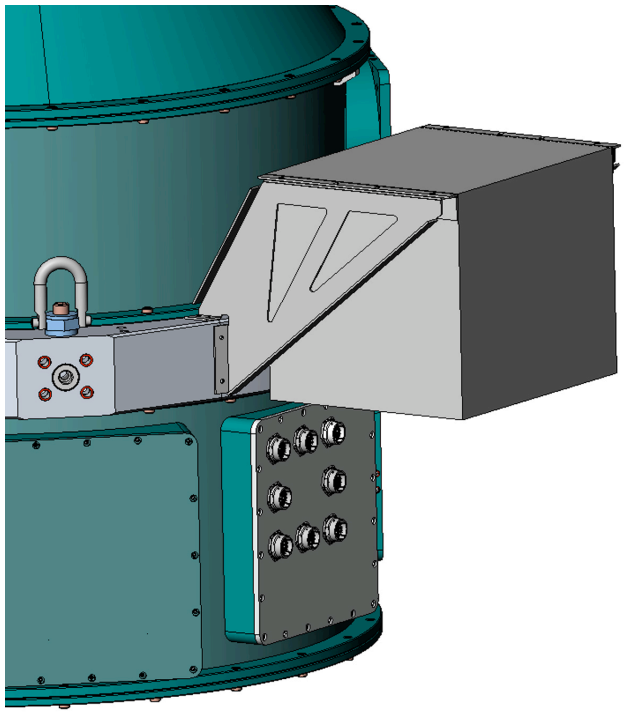
Naïve Scaling:

24 Acq cards ⇒ ×3

Cost ~ $320k

Power ~ 530 W

Space on the Telescope



NEWFIRM uses a standard "VME" crate (~11" × 7" × 19")
We need four, if this is the route we take.

We can't afford this much space Inside the telescope.

Relation to SNAP Efforts

- The current CRIC chip has amplifiers, but no ADC.
  (6.5 mW for 4 channels). They are working on adding ADC.

  This has important space and power implications.
  Digital electronics does not need to reside close to sensors.
  (*I.e.*, perhaps we can move the DHE electronics outside.)
  We would have to design a new acquisition card.
  More channels/card (?) $\Rightarrow$ fewer crates. Cost savings?

- SNAP currently uses the Leach (SDSU) controller.
  Can Monsoon duplicate the protocols? (We need to study…)

We need to establish good communications with LBL.