# A Multi-Channel Time-to-Digital Converter Chip for Drift Chamber Readout

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*Abstract*

A complete, multi-channel, timing and amplitude measurement IC for use in drift chamber applications is described. By targeting specific resolutions, i.e. 6-bits of resolution for both time and amplitude, area and power can be minimized while achieving the proper level of measurement accuracy. Time is digitized using one eight channel TDC comprised of a delay locked loop and eight sets of latches and encoders. Amplitude (for dE/dx) is digitized using a dual-range FADC for each channel. Eight bits of dynamic range with six bits of accuracy are achieved with the dual-range. The timing and amplitude information is multiplexed into one DRAM (Dynamic Random Access Memory) trigger latency buffer. Interesting events are then transferred into an SRAM (Static Random Access Memory) readout buffer before the latency time has expired. The design has been optimized to achieve the requisite resolution using the smallest area and lowest power. The circuit has been implemented in a 0.8µ triple metal CMOS process. The TDC sub-element has been measured to have better than 135 ps time resolution and 35 ps jitter. The DRAM has a measured cycle time of 80 MHz.

## I. INTRODUCTION

This paper describes the design of an integrated circuit for processing the signals from the wires of drift chambers. It is designed to be replicated in large quantities at a low cost per channel, and is therefore suitable for general application in instrumenting large drift chambers in large-scale physics detectors.

As shown in Figure 1, the electronics for a drift chamber channel is typically designed and implemented in two sections. The first section (the analog section) connects directly to a drift chamber wire and performs amplification, shaping and discrimination on the analog signals from the wire. The second section contains mainly digital electronics for digitizing the signals, saving them for the trigger latency period, and outputting packets of digital information selected by the triggers. This section of electronics has been implemented as an integrated circuit and is described here. The timing reference for the electronics is a clock whose frequency is 60 MHz.

## II. FUNCTIONAL DESCRIPTION OF THE ASIC

Figure 2 shows a simple block diagram of an ASIC, which is suitable for a description of its basic functions. The ASIC is designed to process the signals from eight drift chamber channels. Each channel has its own TDC (Time-to-Digital Converter) and FADC (Flash Analog-to-Digital Converter).

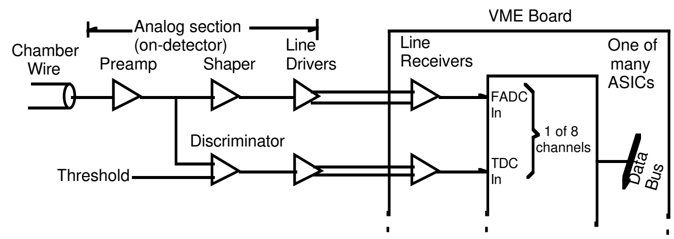


Figure 1. Simplified block diagram of the front-end electronics for a single drift chamber wire.

A single channel's worth of TDC and FADC functions are shown; all eight channels are merged into one DRAM (Dynamic Random Access Memory) and following blocks. A block diagram of the complete ASIC is shown in Figure 3.

The basic tasks of the ASIC are:

1) to continuously digitize, at a 30 MHz rate and a six to eight bit dynamic range, the waveforms of eight shaped signals from the analog section;
2) to record the time-of-arrival of each discriminated pulse with a resolution of 0.5 ns;
3) to save all information in 1) and 2) for a length of time equal to the trigger latency time of up to 12 µs;
4) for each trigger, create a packet in SRAM containing the history of 1) and 2) for a pre-determined time period no greater than 2.2 µs, this history being relevant to the event associated with the trigger;
5) output the packets and ancillary data, on command, for downstream processing.

Within the ASIC, all of these operations proceed simultaneously without interfering with each other.

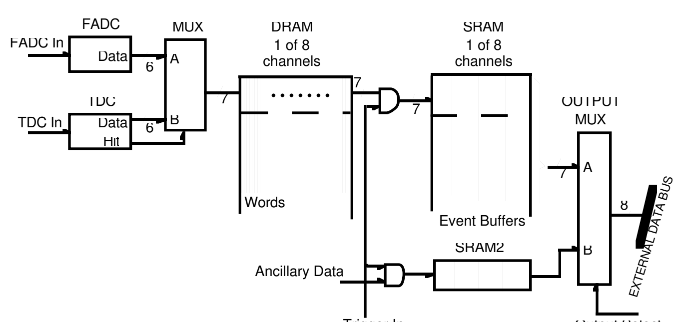


Figure 2. A simplified block diagram of one of eight channels on an ASIC.

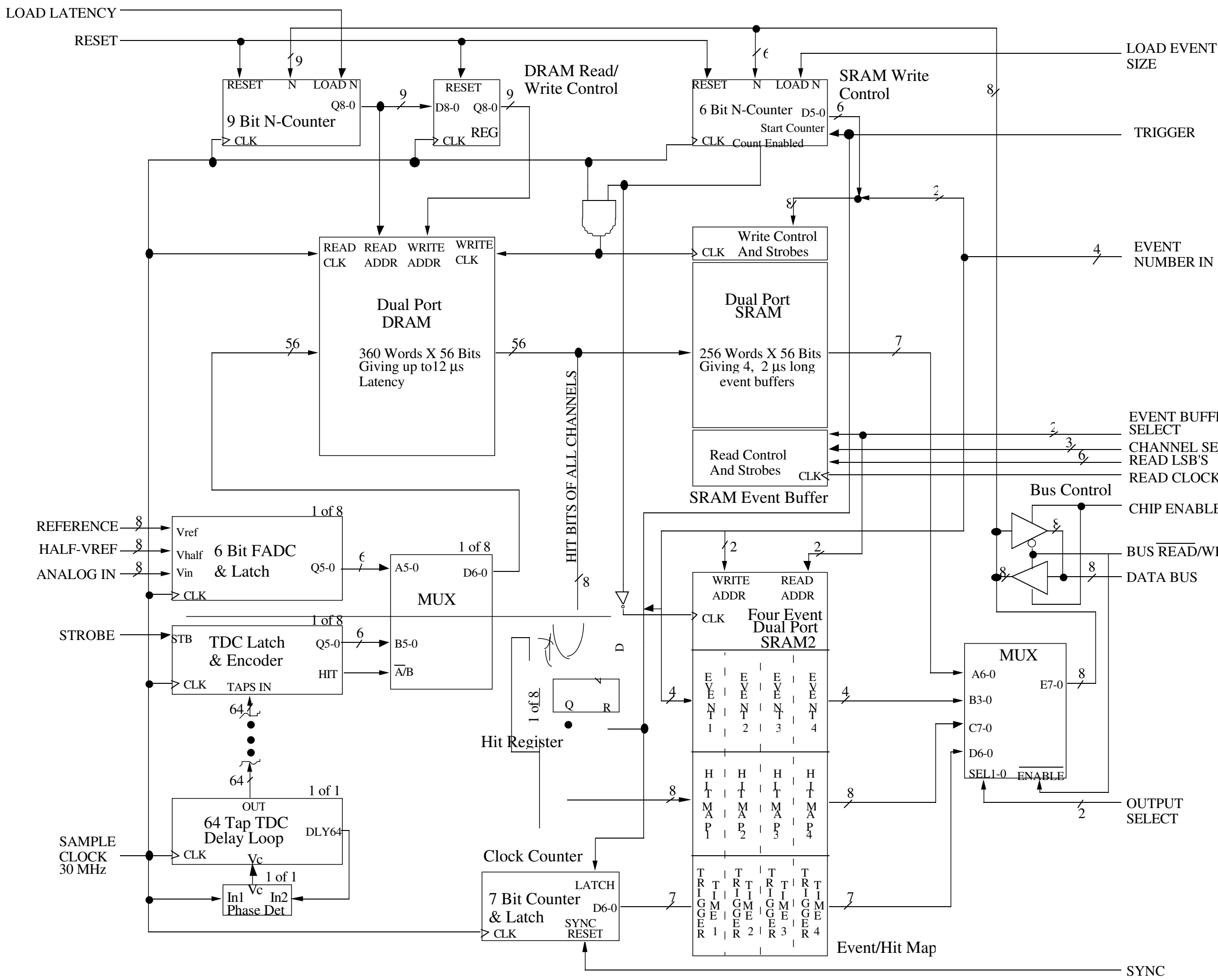


Figure 3. Block diagram of the complete Drift Chamber readout IC.

## III. FUNCTIONS OF THE TDC AND FADC

The two signals from a channel of the analog section are delivered to the TDC and to the FADC. The TDC Input Signal consists of the strobes generated by the discriminator in the analog section. The FADC Input Signal is the shaped pulses generated by the shaping amplifier in the analog section.

The System Clock signal is a square wave of 60 Mhz which is divided internally by 2. For brevity, the half-frequency clock signal is referred to in this report as Sample Clock. Both the FADC and the TDC synchronize their functions to the Sample Clock.

### *A. TDC*

Each ASIC includes eight TDCs (Time-to-Digital converters), one for each signal channel. The TDC measures the time of arrival of the discriminator output pulses (shown as the TDC In signal on Figure 2) to a 1/2 ns precision. This measurement is done relative to the most recent leading edge of the Sample Clock square-wave signal using a vernier technique. In this technique, each Sample Clock cycle is divided into 64 equal vernier periods of approximately 0.5 ns each. When the TDC receives a leading edge on its input ( a "hit"), it outputs a 6-bit binary number which depicts within which of the 64 periods the leading edge was received (a zero value means the hit was within 1/2 ns of the clock leading edge; a value of one, within 2/2 ns, etc.). This number is accompanied by a "HIT" signal, used to steer the following multiplexer (MUX). The properties of the TDC circuit are published in these proceedings[1]. Similar circuits of this type have been reported previously[2,3,4].

The time-of-arrival is measured with respect to the start (low-to-high transition) of the current Sample Clock cycle. The least count of the output number is 1/64 of a Sample Clock cycle (0.5 ns). The time of arrival of the discriminator pulse is thereby defined by two quantities. First, it is defined in units of 33.3 ns by the particular Sample Clock cycle during which the output occurs; second, it is defined in units of 0.5 ns by the value of the 6-bit number.

### *B. FADC*

The FADC measures the amplitude of the FADC Input signal once for every cycle of the Sample Clock and generates a 6-bit binary number that represents the instantaneous amplitude of the input signal.

A simplified block diagram of the FADC is shown in Figure 4. Since this is a 6-bit measurement, there are 63 comparators; for simplicity, Figure 4 shows a smaller number. Each comparator has two inputs. One input of every comparator is connected to the FADC In signal (the signal to be measured); the other to a fixed voltage that is the threshold value for that comparator. The threshold values are derived from the divider network, which is essentially a chain of 64 resistors of equal value; again a smaller number of divider nodes is shown in Figure 4. The bottom of the chain is at ground potential; the top is always connected to an input, Vref; the midpoint is optionally supplied by a second input HalfVref. The comparators are based on a published design[5].

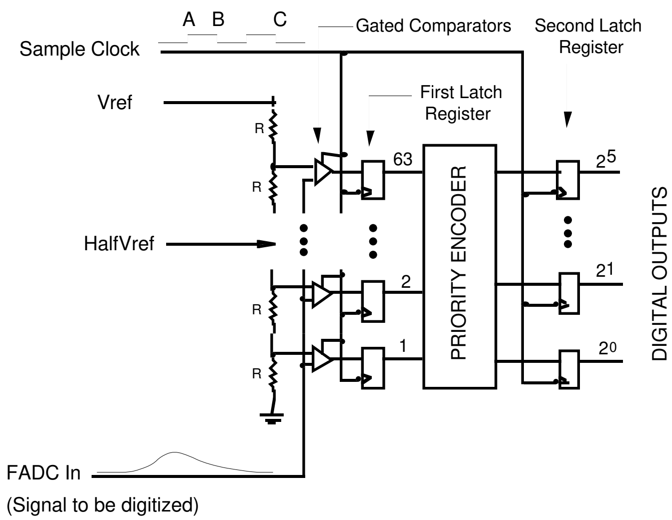


Figure 4. Simplified schematic of the FADC. Referring to the Sample Clock waveform, the gated comparators measure the signal amplitude at A; the result is strobed into the first latch register at B; the binary-encoded value is strobed into the second latch register at C.

The span of the 6-bit FADC is from 1 volt to Vref. The range of usable Vref values is 1 to 4 volts. A 7- or 8-bit dynamic range can be accomplished in at least two ways:

1) By applying an analog signal derived from the shaper output to Vref. This can result in a non-linear transfer characteristic which has a smooth curvature. In this case, HalfVref is probably left floating;
2) By applying a dc voltage to Vref, and another dc voltage to HalfVref, where, usually, HalfVref < 1/2 Vref. This results in double-sloped transfer characteristic, where the break point is at the output value of 31.

### *C. Multiplexing*

The six-bit numbers from the FADC and from the TDC are applied to a two-input MUX. To each number a seventh bit is added; a value of "0" denotes a FADC value, while a "1" denotes a TDC value. The output of the MUX consists of a continuous stream of 7-bit binary numbers, one each sample clock period. Most of these will be FADC numbers; however, each time the TDC detects a "hit," the MUX substitutes the binary number from the TDC for the one from the FADC. (Note that this does not result in a "hole" in the stream of amplitude information, since the amplitude of the shaped signal at the time of the "hit" is taken prior to the rise over threshold of the input signal.) As shown in Figure 4, each FADC includes a second D-latch register. The object of this configuration is to provide a one cycle digital delay so the FADC and TDC data are synchronized.

A typical pattern at the output of the MUX therefore consists of a succession of numbers from the FADC, followed by a single number from the TDC, followed by a succession of numbers from the FADC. The TDC number is recognized by the fact that its most significant bit is a "1". Only FADC information following the TDC hit up to the maximum value of the drift time is of interest.

### *D. DRAM*

The continual stream of 7-bit numbers from the MUX is fed into a DRAM along with the streams from the other seven channels in the ASIC. Because all streams are delivered in synchronism with the Sample Clock, all 56 bits of the eight streams can be stored in the DRAM each Sample Clock cycle.

The DRAM is functionally organized as eight fixed-length FIFOs, having a fixed fall-through time that is equal to the trigger latency time (i.e., the time following the actual physics event at which a trigger related to that event arrives at the ASIC). In this design, the maximum value of trigger latency time is 12 µsec. The DRAM therefore is designed to have a storage capacity of eight channels of 360 words of 7 bits each. (360 x 33 ns $\cong$ 12 µs.) Accommodation is made to operate with shorter latency times by loading a "latency" register which controls the effective size of the DRAM.

The DRAM is implemented as a two-port memory, capable of simultaneously writing into a memory location while reading from another. In this application, the writing operation is going on continuously at the Sample Clock rate. Because of the steady writing, no other refreshing of the DRAM is necessary.

To minimize power consumption, Read Clocks are applied only when DRAM data words are being transferred to the SRAM. During a read cycle, all eight 7-bit words from the eight channels of the DRAM are read simultaneously onto a 56-bit bus leading to the SRAM. Because of the addressing scheme used in this ASIC, each word being read from the DRAM was written a fixed number (determined by the value of the latency register) of Sample Clock cycles earlier.

A 9-bit binary counter is used to generate the read address for the DRAM. This counter is incremented each Sample Clock cycle, and resets to zero after it reaches the same value as in the 9-bit latency register.

### *E. SRAM*

The SRAM has a capacity of 256 7-bit words for each of the eight channels. Logically, the space for each channel is organized as having four discrete "buffers," numbered 0 to 3, each having 64 words of storage. Each buffer can therefore accommodate one packet of data from a trigger.

Physically, the SRAM memory is 256 words long and 56 bits wide. As logically organized for writing, the SRAM partition for each channel contains 256 7-bit words, and therefore requires an 8-bit write address. All eight channels use the same write address.

The filling of an SRAM buffer with data originating from the DRAM is initiated by the receipt of a trigger at the Trigger input. The trigger is accompanied by a 4-bit event number, arriving via the Event Number In inputs. (This number remains static at the Event Number In port until the next trigger.) The two least-significant bits of the event number are used to select the buffer into which the DRAM data is to be written--i.e., they constitute the two most-significant bits of the SRAM write address. The lower six bits are provided by a 6-bit counter.

When enabled, the counter is incremented each Sample Clock cycle. The counter initially has a count of zero. The receipt of a trigger enables the counting, and also enables the receipt of Sample Clock "write strobes" by the SRAM. Sequential incoming words are thereby written into consecutive locations. Up to 64 words are transferred from DRAM to SRAM after a trigger. The number of words to be transferred is set at start-up by the Event Size Register.

The SRAM, like the DRAM, is a dual-port memory and can be storing data from the DRAM in one memory location while it is simultaneously outputting, toward an off-chip entity, data from another location.

*F. Ancillary data; aids to sparse readout*

The simplified block diagram of Figure 3 includes a second, small, SRAM memory, SRAM2, that has a capacity of four 20-bit words. Each word can be considered to be a mini-buffer, numbered 0 to 3, each of which is associated with the similarly numbered buffer of the main SRAM. Each buffer contains the 4-bit event number received with the corresponding trigger; an 8-bit number from a clock counter (used to verify time of arrival of the trigger signal); and an 8-bit hit map. The hit map gives the external system controller a method of determining which, if any, channels had "hits" in the current event. Each of its eight bits is assigned to a single channel, and is set to "1" if that channel had a hit (one or more TDC words) in the current data packet.

The hit map can be used to effect a sparse readout of the data in the corresponding SRAM buffer; it could do this by issuing only readout addresses that access those channels that have hits.

The Hit Register consists of eight clocked Set-Reset flip-flops, one per channel. The Set input of each flip-flop is connected to the MSB of the 7-bit field assigned to its particular channel. This bit is "1" only for words originating in the TDC. The presence of a "1" thereby denotes a hit on the drift chamber wire associated with that channel. The clocking of the flip-flops is by sets of up to 64 Sample Clock edges that are enabled during the filling of an SRAM buffer.

The flip-flop of each channel is reset at the start of a filling of an SRAM buffer. If a "1" is present on its Set input for any of the words relevant to its assigned channel, then the flip-flop is set, and remains set until reset at the start of the next buffer filling.

At the end of the buffer filling, the state of the eight flip-flops in the Hit Register is transferred into the current buffer (the same buffer number as for the SRAM) of SRAM2 in the 8-bit HITMAP field.

The Clock Counter is an 8-bit counter that counts Sample Clock cycles. It is initialized (set to zero count) by a signal called Sync, which is issued by the system controller at start-up and periodically thereafter. A Sync pulse therefore puts all the Clock Counters in all the ASICs of the system into count synchronization.

*G. Initialization & Readout*

There are three registers that are initialized by being loaded with data from the read/write bus. These are the Latency register, the Event Size register, and the Threshold register. The function of the first two registers has been described earlier; the third register (one for each channel), not shown in the block diagram, provides an on-the-fly comparision of the FADC data to a registered threshold value. This is used for deriving the fast detector trigger.

The readout of data from the SRAM is under control of an external system controller. In the readout protocol, the controller specifies the address of each 7-bit word to be read from the SRAM, and to be transferred to the downstream electronics. The address includes: a 2-bit field that specifies an SRAM and SRAM2 buffer; a 6-bit field that specifies a particular word in that SRAM buffer; and a 3-bit field that specifies a channel number. Data stored in the SRAM is read out in 7-bit words. Each 7-bit word carries a single datum from a particular channel. Data from any channel or buffer can be randomly accessed.

## IV. CONCLUSIONS

A complete, multi-channel, timing and amplitude measurement IC for use in drift chamber has been described. The individual major components (TDC, FADC, DRAM, SRAM) have been separately fabricated and then combined together to form the full ASIC. Performance results of the TDC has been described separately and is known to be accurate to 135 ps. The DRAM has been measured to have an 80 Mhz cycle time, which is more than adequate for this design. The complete 5 mm x 4 mm IC is currently in fabrication.

## REFERENCES

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