DRAFT

FEE Functional Requirements

Paul Barale*, Fred Bieser*, Jim Hunter*, Spencer Klein*,
Tom Noggle*, Chinh Vu*

*LBL

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1.0 Introduction

The STAR Time Projection Chamber (TPC) Front End Electronics (FEE) electronic functional requirements are detailed in this note. The requirements are related to the physics where possible. This document is arranged such that for each requirement there are, in general, three sections. The sections are:

- Requirements
- Justification
- Current Status

The current status section will be omitted when the justification is complete. Appendixes are added where additional background information is needed.

2.0 Executive Summary

The tables below provides an overview of the TPC FEE requirements. Justifications are included in later sections of this document.

Table 1
TPC Parameters Table

Parameter	Value	Units
Pad Size	See Table 2	
Pad Count (total)	136,608	pads/TPC
Pads/Sector	5692	pads/sector
Pads/Outer Sector	3942	pads/outer
Pads/Inner Sector	1750	pads/inner
Avg. Particles/Pad	2.7	
Max. Integrated Charge	0.22	pC
Min. Ionizing Signal	16K	electrons
Maximum expected Signal (including fluctuations)	640K,	electrons
Noise level	800	electrons
Signal-to-Noise Dynamic Range	800:1	
Crosstalk	0.3	%
Gain Differential Non-Linearity	±4.8	%
Tail Correction (@ 1 µS)	+0.5, -0.2	%
Tail Correction (@ 10 µS)	±0.2	%
Output Pulse Peaking Time	180	nS
Output Pulse FWHM Time	180	nS
Gas Drift Velocity (He-Ethane/P10)	2.5/5.0	cm/µS
Transverse Position Resolution	See Table 2	
Position Resolution in Drift Direction	700	microns
Sample Rate (He-Ethane / P10)	6.25 / 12.5	MHz
Number of Samples in Drift Direction	512/1024	
Power/Channel (512/1024 time samples)	0.11/0.12	W/ch
Digitization Time, all samples	10	mSec.
Event Size (uncompressed, 512/1024 time samples)	69/138	MBytes
Gas Gain (nominal)	5×10^3	
Energy Resolution	See Table 2	
Test Pulse Injection	yes	
Down Load Test Patterns	yes	
Local Event Data Buffer	yes	
Zero Suppression	no	
Redundancy	minimal	
Remote Power control	yes	

Table 2
Parameter Differences between Inner and Outer Sectors

Parameters	Inner Sector	Outer Sector
Pad Size	2.85 x 11.5 mm	6.2 x 19.5 mm
Pad Count (total)	42,000	94,608
Pads/Sector	1750	3,942
Transverse Position Resolution	280 µm	410 µm
Position Resolution in Drift Direction	700 µm	700 µm
Energy Resolution	XXX	YYY
Coupling Between Wire and Pad	15% -> 20%	15% -> 20%
Gas Gain (nominal)	5×10^3	5×10^3

Table 3
Interfaces to other Detector Components

Interface	Definition Document
DAQ Interface	**"Front-End Electronics <=> Receiver Card Fiber Optic Link Specification"** (In development)
Slow Controls Interface	**"ReadOut Card Slow Controls Interface"** (In development) **"FEE Low Voltage Slow Controls Interface"** (In development)
Clock/Trigger Interface	**"Trigger <=> Front-End Electronics Interface Specification"** (In development)
System power	**"FEE AC Power Interface Specification"** (In development)

3.0 On-Detector Electronics

3.1 TPC Data Collection, Control, and Transmission

3.1.1 FEE Card

3.1.1.1 Type of electronics

Requirement:

The FEE electronics chain will use a charge sensitive gated integrator, followed by a shaping amplifier, an analog memory, and digitizer per channel.

Justification:

Common engineering practice for electronics for Time Projection Chambers dictates a charge-sensitive integrator followed by a shaping amplifier matched to gas diffusion time constants for minimum system noise. Use of an analog memory for temporary signal storage provides minimum system noise and power, and a digitizer per channel provides the necessary high event data throughput.

3.1.1.2 Pad Sizes, Pad Counts, Pads per Sector

Requirement:

Pad sizes are set by physics requirements on dE/dx and position resolution (see STAR Conceptual Design Report PUB-5347 and STAR Notes 33, 34, and 88 for derivation). For the outer sector, the pad size is 6.2 x 19.5 mm and on the inner sector the pad size is 2.85 x 11.5 mm. The number of pads per sector and total pad counts are set by mechanical constraints and the pad size definitions defined in the previous documents.

Justification:

Pad sizes, pad counts, and pads per sector are set by the physics requirements and mechanical limitations of the STAR detector system.

3.1.1.3 Average Particles per Pad, Maximum Integrated Charge per Pad

Requirements:

The average number of particles per pad (2.7) and the maximum integrated charge per pad (0.22 pC) are established by theoretical analysis supported by simulation work.

Justification:

These numbers have been derived from work detailed in STAR Note 142 that details the theoretical analysis of these parameters as well as simulation work to support the analytical results.

3.1.1.4 Maximum Expected Signal

Requirements:

The electronics must be able to handle the maximum expected signal (96 fC) and accurately amplify and digitize this signal. This maximum signal covers all expected signal variations due to Landau fluctuations and dE/dx variations in the particle species.

Justification:

Good engineering practice dictates that a system dynamic range be established and that the design be adequate to accurately handle the largest expected signal.

3.1.1.5 Noise Level, Dynamic Range

Requirement:

The total noise level of the Front End Electronics is set to 800 e-, a factor of 20 below the minimum ionizing signal in the TPC. The system dynamic range is set to 800:1.

Justification:

Position resolution and dE/dx measurements accuracy depend on system signal-to-noise ratio. The S/N ratio is required to be 20:1 for adequate system accuracy (see STAR Note 137). The system dynamic range is set high enough to accommodate differing ionizations (due to differing velocities) and fluctuations expected from particle tracks in the gas volume.

3.1.1.6 Crosstalk

Requirement:

Crosstalk must be minimized so that weak signals can be accurately discerned from adjacent stronger signals and that position resolution and dE/dx measurements can be made to the required accuracy.

Justification:

Particle separation, position resolution and dE/dx measurements accuracy would be degraded if crosstalk is too high. Crosstalk limits are established by the required measurement accuracy as set in the STAR CDR and associated STAR Notes.

3.1.1.7 Gain Linearity

Requirement:

The Differential Gain Non-Linearity is set to ±4.8%.

Justification:

This parameter has been calculated in STAR Note 137 and the calculation has had supporting simulation work to verify the result.

3.1.1.8 Tail Correction Accuracy

Requirement:

The tail correction accuracy is established to levels that permit accurate track separation, particle resolution, and particle position.

Justification:

The tail correction accuracy is set to allow particle position resolution as defined in the STAR CDR (PUB-5347) and supporting STAR Notes.

3.1.1.9 Gas Drift Velocity, Sample Rate, Samples in Drift Volume

Requirements:

The sample rate (6.25 MHz for He-Ethane, 12.5 MHz for P10) is matched to the gas diffusion rate and required position resolution, which in turn is matched to the gas drift velocity. The number of samples is derived from the gas diffusion rate and sampling rate.

Justification:

The required number of samples is set by the gas longitudinal diffusion and is matched to the gas drift velocity. Given the possibility of two different gases, with different diffusion/drift velocities, leads to the requirement for two different sample counts.

3.1.1.10 Power per Channel

Requirement:

The power per channel in the electronics mounted on the pad plane must be minimized (and bounded) because of the strong dependence on gas drift velocity with temperature. The requirement is that the temperature variation across the pad plane be < ±0.7° C (RMS). The current limits on the power per channel are 0.11 W/channel (512 time samples) and 0.12 W/channel (1024 time samples).

Justification:

The power per channel of the must be minimized and a maximum value established so that proper pad plane cooling can be designed. The requirement of ±0.7° C (RMS) is set by the maximum variation in drift velocity allowed given the position resolution requirements (see STAR CDR).

3.1.1.11 Front End Card

Requirement:

A separate, small card is required to connect directly to the pad plane. The card is required to minimize trace capacitance between the pad plane board and the electronics and the card width is defined by the mechanical access slots.

Justification:

Use of a small card serving a modest number of channels (32) minimizes the trace length and capacitance between the TPC pad plane and the Front End Electronics. The card width is set to 2.9 inches, a width adequate to mount the custom analog ICs but narrow enough to fit within the mechanical limitations of the strongback. The Front End card provides a minimal amount of circuitry, only enough to provide the necessary amplification, shaping, analog storage, and digitization needed.

Current Status:

The Front End Card is currently at the operating prototype stage.

3.1.1.12 Test pulse injection to the Front End

Requirement:

Computer controlled analog test pulses must be injected into the earliest possible stage of the Front End Electronics (SAS Calibration on FEE card).

Justification:

Injection of test pulses is required to test the linearity and operational capability of the front end electronics. The test pulses serve a diagnostic capability as well.

3.1.2 ReadOut Card

3.1.2.1 ReadOut Card

Requirement:

The ReadOut Card is required to provide power regulation and control to the front end card and is required for local control, data multiplexing, and monitoring of the on-detector electronics.

Justification:

Good engineering practice dictates that expensive and complicated control electronics be minimized. The electronics on the ReadOut Card performs this function, preventing replication on each of the front end cards. In addition, the local electronics on the ReadOut Card provides power regulation and control for both the ReadOut Card and for the front end cards.

Current Status:

A prototype ReadOut Card is partially designed and sections are being prototyped.

3.1.2.2 Zero Suppression

Requirement:

Data collected from the front end cards will be collected by the ReadOut Card and passed to the DAQ system with no zero suppression.

Justification:

The fiber optic link speed is high enough and the operations to be performed for zero suppression are complicated enough (and require additional power and complexity) that transmitting the raw data off the detector is the preferred method. In addition, the exact method of zero suppression is undefined, so transmitting all the data off the detector allows significant flexibility in the design of future zero suppression algorithms.

3.1.2.3 ReadOut Card Output of Test Patterns to DAQ

Requirement:

There is a requirement for the ReadOut Card to be capable of outputing a limited set of test patterns to the DAQ system in order to exercise and debug the data path into the Data Acquisition System.

Justification:

The ability to output known data patternsfrom the ReadOut Card to the DAQ System is a powerful diagnostic tool. Good engineering practice requires real time, online diagnostic capabilities to ensure correct operation of the system.

3.1.2.4 Local Event Data Buffer

Requirement:

A local data buffer able to store at least one full event's worth of data needs to be present on the ReadOut Card.

Justification:

Allows simultaneous multiple users to test/debug the front end electronics (from the RDO level down) in situ using individual pad monitors via the Slow Controls link.

3.1.2.5 Redundancy

Requirement:

Little or no redundancy is provided in the Front End Electronics system.

Justification:

Failures of sections of the Front End Electronics system will have a relatively small impact on the detector tracking capability because of the relatively small granularity of the on-detector electronics. The small granularity has been chosen, in part, because the detector is inaccessible during normal operation, hence a small granularity of electronics on the detector means that individual failures have minimal effect on the total detector tracking capability.

3.1.2.6 Defect location for the ReadOut Card and Front End Card

Requirement:

The electronic will be constructed so that defects can be located through the Slow Controls connection and electronics can be replaced at the board level. This strategy assumes that the Slow Controls connection, cables, and drivers are not defective, however.

Justification:

The requirement is set based on good engineering practice and budget constraints.

3.1.2.7 Repairability

Requirement:

The electronics will be constructed such that diagnostics can be performed to locate a failure to the board level. Repair will take place off-line and a diagnostic test stand will enable repair at the component level.

Justification:

The requirement is set based on good engineering practice and budget constraints.

3.1.2.8 Spares

Requirement:

Spare boards and components will be provided, along with board-level testers able to identify failures down to the component level.

Justification:

Spare boards will be provided to minimize detector down-time. Spare components will be provided for off-line diagnosis and repair of faulty electronics. Good engineering practice dictates that spare boards and components be provided for a system of this scale. Spares provision is subject to budget constraints and is estimated to be at the 5% level for boards and individual components.

3.1.2.9 Remote Power Control

Requirement:

Groups of front end cards must be able to be turned off remotely.

Justification:

During normal detector operation, the Front End Electronics is, in general, inaccessible. Good engineering practice dictates that front end cards must be able to be turned off in case of oscillating or excessively noisy front end cards without disabling large sections of the detector. It is not required that each individual FEE card be turned off separately - blocks of 6 FEE cards (3 cables worth) is deemed an acceptable granularity without compromising the system usability.

3.1.2.10 Trigger System Interface

Requirement:

It is required that the ReadOut Card connect to the Trigger System through a standard set of signals (defined in "Trigger <=> Front-End Electronics Interface Specification") to sample event data in coordination with other subsystems.

Justification:

The Trigger System provides the basic signals for selecting promising event data and coordinating the operation of all subsystems within the detector. The interface is defined in the document "Trigger <=> Front-End Electronics Interface Specification" (in development). Good engineering practice dictates that system interface specifications be adhered to.

Current Status:

Interface specification document is in development.

3.1.2.11 DAQ Interface

Requirement:

It is required that the ReadOut Card transmit its data to the DAQ system on demand.

Justification:

The Front End Electronics needs to be able to pass its data on to the DAQ system. The interface is defined in the document "Front-End Electronics <=> Receiver Board Fiber Optics Interface Specification" (in development).

Current Status:

Interface specification document is in development.

3.1.2.12 DAQ Interface via Fiber Optic Link

Requirement:

It is required that data from the Front End Electronics to the Data Acquisition System be passed on fiber optic cables.

Justification:

Fiber optic cables support the necessary high frequency of data transmission for the data volume off the detector. In addition, the use of fiber optic cables breaks up any potential ground loops. Good engineering practice dictates that system interface specifications be adhered to. If these system interface specifications are not adhered to, the flogging of engineers will begin immediately and continue until morale improves.

3.1.2.13 Slow Controls Interface

Requirement:

It is required that the ReadOut Card interface to Slow Controls for system operation.

Justification:

Slow Controls provides the monitoring and control capability for the ReadOut Card. This interface is defined in the document "ReadOut Card Slow Controls Interface" (in development). Good engineering practice dictates that system interface specifications be adhered to. Cost and operational complexity require that a commercially available network based system with good software support be used.

Current Status:

Interface specification document is in development.

3.1.2.14 Geographic ID, Thermistor Connection

Requirement:

It is required that the ReadOut Card have a connection to the "ID and Thermistor Connector". It is a requirement that the Front End Electronics monitor the aluminum strongback temperature and this connection is made on the "ID and Thermistor Connector".

Justification:

Good engineering practice dictates that a unique geographic ID be provided to identify the on-detector location of a given ReadOut Card. The requirement for temperature monitoring on the strongback via the thermistor and the need for a geographic IC provides the justification for this connector.

3.1.2.15 Low Voltage Power Connection

Requirement:

Low voltage power is required for operation of the ReadOut Card and is required to be provided to the Front End Cards.

Justification:

The electronics on the ReadOut Cards and the Front End Cards will not work without a proper power source. It is estimated that each ReadOut card pair and associated 36 FEE cards will require ~20 amps of both +8 and - 8 volts of "raw" (regulated at the remote power supply). The +/- 8 V is nominal and is allowed to be in the range of +/-6.5 V to +/- 8.5 V, depending on regulators used and voltage drops in the cabling.

3.2 Clock/Trigger Local Fanout

3.2.1. Sector Clock/Trigger Signal Relationships

Requirement:

The interface to the Trigger System is through the standard set of signals defined in "Trigger <=> Front-End Electronics Interface Specification"

Justification:

Good practices dictate that interface specification will be followed.

Status:

An interface document describing the Clock/Trigger interface is in development.

3.2.2 Sector Clock/Trigger Fanout - RDO Drive
Requirement:
Each Sector Clock/Trigger Fanout shall be able to drive at least 6 RDO boards.

Justification:
Present sector layout and front-end electronics requires 6 master ReadOut cards / sector.

3.2.3 FEE Clock/Trigger and Timing Fanout Signal Noise
Requirement:
The FEE Clock/Trigger and Timing Fanout signals line shall generate minimum noise and EMI.

Justification
The signals distributed on-detector for the clock and trigger will be shielded, differential signals to minimize noise and EMI. It is good engineering practice to minimize noise sources on the detector.

Current Status:
In development.

3.2.4 FEE Sector Clock/Trigger Fanout Skew between ReadOut Cards
Requirement:
There should be minimum signal skew on fanned-out signals provided to ReadOut Cards

Justification:
Signal skews can effect the quality of the physics data. Good engineering practice dictates that cable lengths be equalized and that skews be minimized.

3.2.5 FEE Sector Clock/Trigger Fanout Power
Requirement:
Each FEE Sector Clock/Trigger Fanout Chassis shall use minimum power and dissipate minimum heat.

Justification
Minimize heat load on-detector.

3.2.6 Cable Lengths

Requirement:

The cables between the FEE cards and the ReadOut card must all be the same length and as short as possible.

Justification

A common length of cable minimizes skew between Front End cards during the detector sampling phase. Keeping the cables as short as possible is good engineering practice to minimize radiated noise from the cables. Timing variations due to cable skews needs to be **<** ±3.5 nS to keep skews below the position resolution figures.

3.2.7 Open cable states

Requirement:

All circuitry shall be designed so that an open input places a signal into an inactive state.

Justification:

Good engineering practice.

4.0 Off-Detector Electronics

4.1 FEE Power Supply System

4.1.1 Power Supplies

4.1.1.1 Power supply location

Requirement:

The low voltage power supplies must be located off detector.

Justification:

DC power supplies should not operate in a strong magnetic field due to magnetic material causing magnetic field distortions in the detector. Additionally, any possible sources of EMI or other noise should be moved as far as practical from the sensitive Front End electronics.

The end cap area of the STAR TPC is populated, among other things, with Front End Electronics printed circuit boards, ReadOut boards, the steel of the solenoid, and other subsystem electronics and mechanical structures. There is no space available for power supplies on the detector.

4.1.1.2 AC power for power supplies

Requirement:

Alternating current electrical power is needed for the generation of low voltage direct current power.

Justification:

Filtered AC power is the power input provided by RHIC.

Current status:

DC power supplies for FEE have not yet been selected.

4.1.1.3 Active Spares

Requirement:

Spare supplies connected to AC power and with proper power connectors will be present in the TPC Low Voltage racks. Active spares will be provided at the 5% level (approximately).

Justification:

In the event of failure of a DC power supply, personnel must be able to replace a faulty power supply safely and without interrupting DC or AC power to the rest of the detector. Providing active spares limits downtime to swap out a faulty spare. Budgetary constraints limit this sparing to the 5% level.

4.1.1.4 Power supply spares

Requirement:

Spare supplies will be available on-site for repair.

Justification:

Supplies are considered replaceable as a "module". Individual failing supplies will be returned to the manufacturer. Good engineering practice dictates having spare supplies on hand, the number of supplies is subject to budgetary limitations.

4.1.2 Power Cabling

4.1.2.1 Power Cabling

Requirement:

Cables are required to connect the low voltage DC power supplies to the ReadOut cards.

Justification:

Since the power supplies are required to be located off detector, power cables must be supplied in order to deliver the DC power to the ReadOut cards and the FEE boards.

4.1.2.2 Power Cable

Requirement:

Cable of sufficient AWG size and number of conductors to minimize DC voltage loss and heating of the cables and to safely carry the full load current rating of the DC voltage supplies.

Justification:

The power supplies location relative to the ReadOut cards may require a cable length run of the order of one hundred feet. Since the STAR TPC is a temperature sensitive detector and there will be limited air conditioning capability in the detector hall, heat generation must be controlled. For safety reasons, the cable AWG size will be selected to safely carry the full load current without cable overheating.

4.1.2.3 Power Cable Shielding

Requirement:

The low voltage DC power cable must be shielded.

Justification:

To provide as low noise as practical DC power to the Front End Electronics boards.

4.1.3 Interlocks

4.1.3.1 Power Supply Interlocks

Requirement:

Interlocks for DC and AC power will protect equipment and personnel.

Justification:

In the event of failure of one or more of the DC voltages and/or power supplies, an interlock system is needed to protect sensitive front end electronic components and to provide personnel safety.

4.2 Clock/Trigger Off-Detector Fanout

4.2.1 FEE Clock/Trigger and Timing Signal Relationships

Requirement:

The interface defined in the "Trigger <=> Front-End Electronics Interface Specification" shall be used.

Justification:

Good practices dictate that interface specification will be followed.

Current Status:

In development.

4.2.2 FEE Trigger Fanout Power

Requirement:

Each Endcap Trigger Fanout Chassis and Sector Trigger Fanout Chassis will be designed to use minimum power and dissipate minimum heat.

Justification:

Minimize on-detector head load.

Current Status:

In development.

4.2.3 FEE Endcap Trigger Fanout Skew between Sector Trigger Fanouts

Requirement:

There should be minimum signal skew on fanned-out signals provided to Sector Fanouts

Justification:

Signal skews can effect the quality of the physics data. Good engineering practice dictates that cable lengths be equalized and that skews be minimized.

4.2.4 Clock Edge Rise and Fall Time
Requirement:
The distributed clock signal pulses shall have rise and fall times of no more than xxx nanoseconds

Justification
It is good engineering practice to keep clock skew low by keeping the rise and fall times short.

4.2.5 Trigger Delay
Requirement:
The delay before the TPC Front End electronics begins to sample data from the TPC shall be initiated by the Trigger Signal and have no more than xxx microseconds delay.

Justification:
Operation of the Front End Electronics for data collection is initiated by the Trigger Signal (as defined by the **"Trigger <=> Front-End Electronics Interface Specification"**) and should have a short latency delay to maximize the detector drift volume sampled.

4.2.6 Trigger Repetition Rate
Requirement:
Trigger signal repetition rates are determined by possible combinations of 'normal' and aborted cycles.

Justification:
Maximum rep. rate shall be < 10 KHz [limited by Gated Grid cycling requirements].

4.2.7 Gated Grid Control
Requirement:
The Gated Grid open and close shall be generated Trigger System

Justification
Trigger System is the place where TPC FEE timing is generated and known