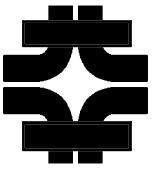

Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project

Circuitry & Artwork Layout
For PC Boards Containing HP G-Link ICs
&
PC Boards Connecting To Finisar HP G-Link Boards

Sept 23, 1997

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Revised 9/23/97 by James Franzen
(with considerable help from several others
including a review by Finisar)

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Table of Contents

1. GENERAL INFORMATION

This document contains a list of circuitry and artwork items for PC boards containing HP G-Link ICs or PC boards connecting to other PC boards containing HP G-Link ICs. Items are marked as either:

A. Mandatory (must be done unless there are strong technical reasons to the contrary)
B. Recommended (should be done)

This list is based on long independent technical discussions with both Finisar & HP experts and our past experience using HP G-Link ICs.

When reading this document, remember that our goals are to basically never have 'out of sync' errors and to have at least less than one bit in 10^{14} data bit error rates. These goals are very hard to achieve.

Important Notes:

1) ***Two quad receiver PC boards are being fabricated to study which is less noisy and thus more reliable. The first has 'Moated (On Three Sides) Ground Planes' for each of the four channels of G-Link ICs and Finisar Optics as shown in Figure 2 of this document. The second has both a 'Voltage (Power Return) Ground Plane' and 'Impedance (Control) Ground Planes'. The 'Voltage Ground Plane' has notches to separate the Finisar optics power return currents, the G-Link power return currents and the TTL/TTL buffer power return currents from each other for each of the four channels. These two types of ground planes are connected only at the J3 (J5/J6) and J0 connectors of this VME Transition Module (VTM). The TTL/TTL buffers close to the G-Link ICs are connected to the Impedance Ground Planes. The G-Link ICs and the Finisar optics are connected to the Voltage Ground Plane. Contact Ed {barsotti@fnal.gov} or Bob {rwd@fnal.gov} before finalizing your board layout for our test results and recommendations at to which type of ground plane(s) board to build.)***
2) ***Special care is needed at the TTL/TTL buffer (or ECL/ECL translator) interface to the G-Link IC regarding grounding, power voltage bypassing and power voltage charge (current) surges. Return currents from circuitry signals and from power supply surges <u>both</u> flow through the same ground plane. Provide extra storage and bypass capacitance in this area.***

2. MANDATORY CIRCUITRY & ARTWORK LAYOUT ITEMS

2.1 Overvoltage & Overcurrent Protection

A. At the closest point from connector power pins connect fuses to each input voltage (see Figure 1).
B. At the closest point from the downstream side of each fuse, connect a transient suppresser from that point to voltage common of each voltage .

2.2 Power LEDs

A. Just after each fuse and transient suppresser, add a resistor and (front-panel) LED to voltage common of each voltage.

2.3 Module & Transition Module Front Panels

A. Electrically isolate Module and/or Transition Module front panel.

2.4 "Ground" Planes

A. All GND pins on all connectors should be connected together on the boards Ground Plane (GND).
B. In the vicinity of the Finisar board connector or G-Link ground pins, isolate the ground plane "moat" as shown in Figure 2. This will steer the ground current from other circuits away from these pins and reduce the possibility of ground noise affecting circuitry connected to the Moated Ground Plane. (See Section 2.13)
C. Ground plane thickness must be at least that of one ounce (1 oz.) copper.

2.5 Component Connections To The Ground Plane

A. Connect all "Ground" pins of all circuits to the Ground Plane as close to these pins as possible.

2.6 Filter Input Switching Power Supply Noise

A. To prevent power supply switching frequency noise from getting into the board, add a filter such as that on the VRB Transition Module (VTM) just after the fuse and transient suppresser of each voltage.
B. The VTM filter includes:
   1. 33μF and 0.01μF capacitors on the upstream side of the filter
   2. 33μF and 0.01μF capacitors on the downstream stream side of the filter
   3. A 10 μHy inductor (DT1608C-103) separating the two pairs of capacitors

2.7 Power Planes As AC Ground Planes

A. Do not use power (voltage) planes as AC ground planes.

2.8 Power Supply Voltage Planes

A. After each fuse, input filter capacitors and transient suppresser, create a *Voltage Plane* for each voltage as shown in Figure 3.
B. These *Voltage Planes* should be "contained" between ground planes (see Figure 4).
C. This *Ground Plane* may be the same plane for several *Voltage Planes*. Filter components (see "Filter Each Voltage Into Finisar Board(s) Separately") to various circuit components (TTL/TTL & ECL/TTL translators, etc.) and/or to Finisar G-Link board voltages connect directly to *Voltage Planes* and the *Ground Planes*.

2.9 Filter Each Voltage Into Blocks Of Circuitry Separately

A. To prevent electrical noise in the 10s to low 100s of Megabytes per second range from getting into or out of circuitry blocks (e.g., G-Link IC, Finisar optics, ECL/TTL translators, etc. filter each voltage into these blocks separately (see Figures 2 and 4).

B. Use Kerry Woodbury's pi (or T) integrated filter (preferred) or Bill Haynes' discrete pi filter
C. The lower side of the filter connects to the *Ground Plane*.
D. Contact Kerry Woodbury (woodbury@fnal.gov) or Bill Haynes (haynes@fnal.gov) for filter details.

2.10 Isolation Of Components With (Kerry's or Bill's) Filters

A. Isolate the +5 V voltage needed for Finisar optics from any other +5 V power such as the +5 V power needed for ECL/TTL translators or TTL/TTL buffers for received or transmitted G-Link data and data strobes. Figure 3 illustrates the connection for this or other voltages.
B. Isolate the +5 V voltage needed for TTL/TTL buffers for received or transmitted G-Link data or data strobes from the +5 V voltage needed for other circuitry on the board.
C. Isolate the -5.2 V voltage needed for Finisar boards from any other -5.2 V power such as the -5.2 V power needed for ECL/TTL translators for received or transmitted G-Link data and data strobes.
D. Isolate the -5.2 V voltage needed for ECL/TTL translators for received or transmitted G-Link data or data strobe from the -5.2 V voltage needed for other circuitry on the board.
E. Isolate the -2.0 V voltage needed for G-Link data or data strobe termination from the -2.0V voltage needed for other circuitry on the board.

2.11 Isolation Within a Component

A. As in the case of the Hewlett-Packard G-Link Receiver IC, when an integrated circuit manufacturer specifically isolates similar supply voltages by name and functionality, each voltage must be independently filtered for that device. This means that for a solitary IC there may be multiple filtered sub-blocks of the same potential. The HP G-Link Receiver (HDMP 1024) requires three—VCC, VCC_HS and VCCTTL. Each VCC is derived from the same 5volt source, but each has its own VTM filter circuit.
B. VCC filters to device pins defined as high-speed are to include, in addition to the normal complement of components, a 100 pF capacitor placed as close as physically possible to the device pins drawing current from that filter.

2.12 G-Link Data & Data Strobe ECL/TTL Translators Or TTL/TTL Buffers

A. Placement (see Figure 5 and 6):
    1. Place ECL/TTL translators or TTL/TTL buffers for G-Link data and data strobes as close to the G-Link ICs as possible.
B. If the electrical design does not employ 'soft drive' logic (i.e. low-current output drivers—less than 10 mA) then the design is to use a separate translator or buffer for data strobe from those used for data. An example of a soft-drive buffer is the Cypress CY74FCT162244.
C. If the electrical design does not employ 'soft drive' logic (i.e. low-current output drivers—less than 10 mA) then the design is to use series R or series R & L in parallel:
    1. At the G-Link receiver end:
        a) Place a 33 to 45 ohm resistor in series with each translator or buffer TTL output data and data strobe line as close as possible to the translator or buffer output (see Figures 3a and 3b). These resistors are both for limiting current (and thus lessening 'ground bounce') and for back terminating the signal trace.
        b) The edge speed of the translator or buffer output for the data strobe line should be limited to three nanoseconds for noise control. A controlled rise time driver is a good choice. If a fast edge speed driver is used, an inductor in parallel with the series resistor should be used to limit the rise and fall time. These techniques slow the rise and fall time and minimize spikes in the clock line.
    2. At the G-Link transmitter end, if there is a need to translate from TTL to ECL:
        a) Slow-edge devices such as BTL devices are strongly recommended for driving the translator data and data strobe inputs.

b) If slow-edge devices are not used for driving the translator inputs, place a 33 to 45 ohm resistor in series with each output of the TTL components which drive the translator data and data strobe inputs (see Figure 5). These resistors should be as close as possible to those outputs.

c) The edge speed of the TTL component driving the data strobe translator input should be limited to three nanoseconds for noise control. A controlled rise time driver is a good choice. If a fast edge speed driver is used, an inductor in parallel with the series resistor should be used to limit the rise and fall time. These techniques slow the rise and fall time and minimize spikes in the clock line. Do not make the rise and fall times too slow as errors at the receiving end will result (see "G-Link Transmitter Clock Source", item E).

2.13 G-Link Transmitter Clock Source

Several items regarding the signal 'purity' of the G-Link transmitter's input data strobe affect reliable operation of G-Links. Most are listed below:

A. Use no FPGA or other programmable logic to drive the G-Link data strobe. Thresholds change causing too much jitter.

B. The data strobe driving a G-Link transmitter IC must be clean (e.g., almost no jitter). It is strongly recommended that the data strobe be driven directly from the output of a crystal oscillator or minimally a fast logic gate to buffer the crystal from the data strobe signal.

C. If the G-Link data strobe signal needs to be synchronized to another (external) signal, use a phase-locked loop before the data strobe signal to minimize jitter. Do <u>not</u> drive the G-Link transmitter IC data strobe from the output of a PLL frequency generator that has an internal multiplication factor greater than one. The jitter will have that same multiplication factor!

D. If any other circuitry must be in series with a G-Link data strobe circuit, take measurements to insure that data strobe jitter is well below 50 picoseconds (statistical tails included).

E. If G-Link transmitter IC input data strobe rise time is too slow, errors will occur because the IC will see this as jitter and/or double clocks.

F. Amplitude variations in the G-Link transmitter IC data strobe will result in errors at the G-Link receiver. Keep amplitude variations in the data strobe signal to a minimum.

G. Too fast of a rise time into G-Link transmitter IC is also bad because of ringing, undershoot and resulting noise. Design for minimal ringing and undershoot.

H. The driver output going to the G-Link transmitter data strobe input must not be connected to more circuitry than just the one data strobe input.

2.14 Multiple G-Link Receivers On A Board

A. If ECL G-Link receivers are used, use a separate -2.0 V regulator for each receiver circuit. (see Figure 3)

B. Use the moated ground technique as shown in Figure 2.

C. Don't route signal traces from one channel under the translators, G-Link IC and optics of another layer.

D. To minimize coupling of data strobe and data signal traces of one channel to each other or to that of other channels, route signal traces at the output of the TTL/TTL buffers (or ECL/TTL translators) as strip lines.

E. Signal trace layout at the backplane connector (see Figure 4):
   1. To reduce layer count, artwork such that two signals go between vertical and horizontal connector pins.
   2. Hand routing may be necessary
   3. For example, 6 mil traces with 6 mil spacing between traces, etc. is acceptable. The trace width and spacing may depend on the PCB vendors capabilities - check!

F. Other signal trace layout items:
   1. Do not route data and data strobe signal traces on the outer layers. All other signal traces can be routed on the outer layers.

G. Copper 'pours' on outer signal layers:
   1. To aid in the oscilloscope probing of fast signals if the outer layers are signal traces, 'pour' in (fill in everywhere possible) copper around the signal traces.
   2. To avoid soldering shorts, leave at least 0.025 inch between copper pours and component pads.
   3. If grounds of circuitry near the copper pours are connected to the Ground Plane, connect all those copper pours to the Ground Plane.
   4. If grounds of circuitry near the copper pours are connected to the Ground Plane, connect all those copper pours to all Ground Plane layers.
   5. Again to aid in oscilloscope probing of fast signals, do not solder mask the outer layers in areas where a high quality ground is useful. For inner layer signals this will be near the IC pins connected to the trace(s).
   6. Connect all cooper pour 'islands' to the appropriate ground plane.

2.15 Multiple G-Link Drivers On A Board

A. If ECL G-Link drivers are used, use a separate -2.0 V regulator for each driver circuit. (see Figure 3)
B. Use the moated ground technique as shown in Figure 2.
C. Don't route signal traces from one channel under the translators, G-Link IC and optics of another layer.
D. To minimize coupling of data strobe and data signal traces of one channel to each other or to that of other channels, route signal traces at the output of the TTL/TTL buffers (or ECL/TTL translators) as strip lines.
E. Signal trace layout at the backplane connector (see Figure 4):
   1. To reduce layer count, artwork such that two signals go between vertical and horizontal connector pins.
   2. Hand routing may be necessary
   3. For example, 6 mil traces with 6 mil spacing between traces, etc. is acceptable. The trace width and spacing may depend on the PCB vendors capabilities - check!
F. Other signal trace layout items:
   1. Do not route data and data strobe signal traces on the outer layers. All other signal traces can be routed on the outer layers.
G. Copper 'pours' on outer signal layers:
   1. To aid in the oscilloscope probing of fast signals if the outer layers are signal traces, 'pour' in (fill in everywhere possible) copper around the signal traces.
   2. To avoid soldering shorts, leave at least 0.025 inch between copper pours and component pads.
   3. If grounds of circuitry near the copper pours are connected to the Ground Plane, connect all those copper pours to the Ground Plane.
   4. If grounds of circuitry near the copper pours are connected to the Ground Plane, connect all those copper pours to all Ground Plane layers.
   5. Again to aid in oscilloscope probing of fast signals, do not solder mask the outer layers in areas where a high quality ground is useful. For inner layer signals this will be near the IC pins connected to the trace(s).
   6. Connect all cooper pour 'islands' to the appropriate ground plane.

2.16 ECL/TTL Translator Types

A. Use 100324 ECL/TTL and 100325 TTL/ECL differential translators by Synergy. Other manufacturers "equivalent" parts can generate extra noise and should not be used.

2.17 ECL Terminations

A. Do not use sip termination resistors; use discrete resistors (e.g., type 1206, 330 ohm resistors) with each resistor bypassed with its own 0.01 μF capacitor as shown in Figure 6. If layout is tight the

capacitor could be shared between two resistors. Bypassing each resistor separately is necessary because even feed throughs to voltage planes introduce ½ to 1 μHy inductance to the circuit.

2.18 ECL Device Grounding

1. It has been observed that Finisar uses a separate 10 ohm series resistor when connecting any ECL device pin to ECL ground. The benefit/risk of this practice has not been studied prior to the writing of this technical note. It is merely suggested here that Finisar's reputation and success require us to consider following that design practice for new Fermilab designs.

2.19 PECL Circuitry

A. Do not use PECL circuitry with either transmitter or receiver G-Link ICs.

2.20 G-Link Receiver Data & Data Strobe Signal Line Impedance

A. The signal line from the G-Link to the buffers should be less than 1 inch long so the signals are not in the transmission line mode. Item B below is not recommended and should be avoided if at all possible.

B. To properly terminate G-Link receiver lines which are over 1 inch long, use controlled impedance lines and terminate them in their characteristic impedance to -2 V.

2.21 G-Link Receiver Non-True ECL Data & Data Strobe Differential Outputs

A. The differential data and data strobe outputs from G-Link receiver ICs vary in peak-to-peak levels and may not be centered on the translators V_{bb} reference voltage. If these outputs directly drive ECL/TTL translator inputs, low noise margins result.

B. To increase reliability, use Synergy 100325 differential input ECL/TTL translators to receive G-Link receiver data and data strobe signals as shown in Figure 6 and 3c. (Note that Figure 6 does not address the details of the receiver inputs) These devices generate less noise than other types tested.

C. Use the adjustable voltage reference (or similar circuit) shown in Figure 7. The resistors should be adjusted so the reference voltage at the input to the ECL to TTL translators is centered on the output voltage swing of the G-Link ECL signals. Note that the -5.2 V shown in Figure 7 is the filtered -5.2 V detailed in Figure 6.

D. The resistors in the reference voltage circuit are all 1% chip resistors. The reference voltage should be set to the center of the ECL signal to 10%.

E. The reference circuit shown in Figure 7 has a simple temperature compensation using a dual transistor package.

F. One reference circuit should be provided for each G-Link chip. The assumption is that the G-Link will have uniform output signals with in each chip.

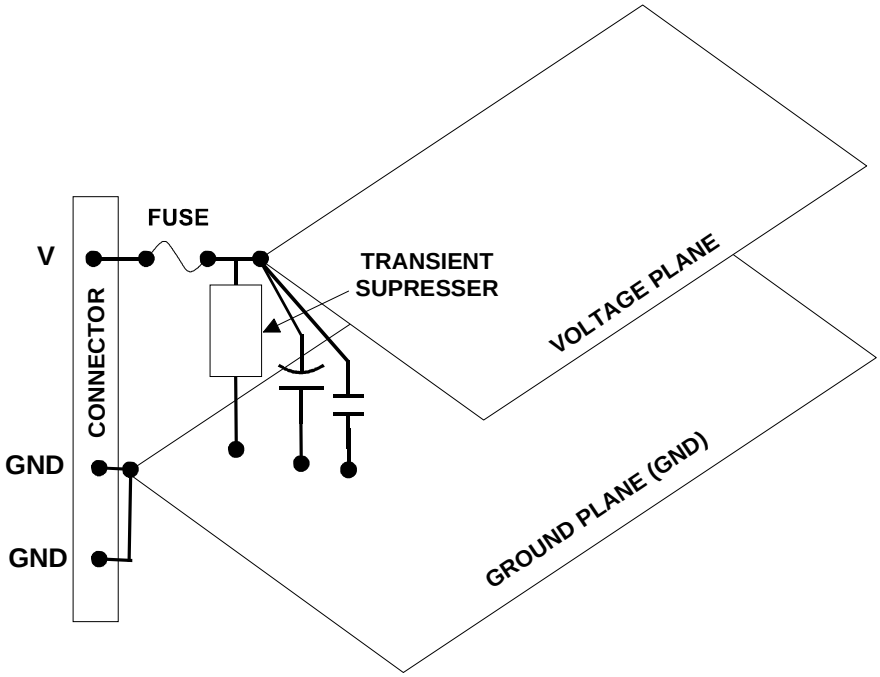

Figure 1
Input Circuitry

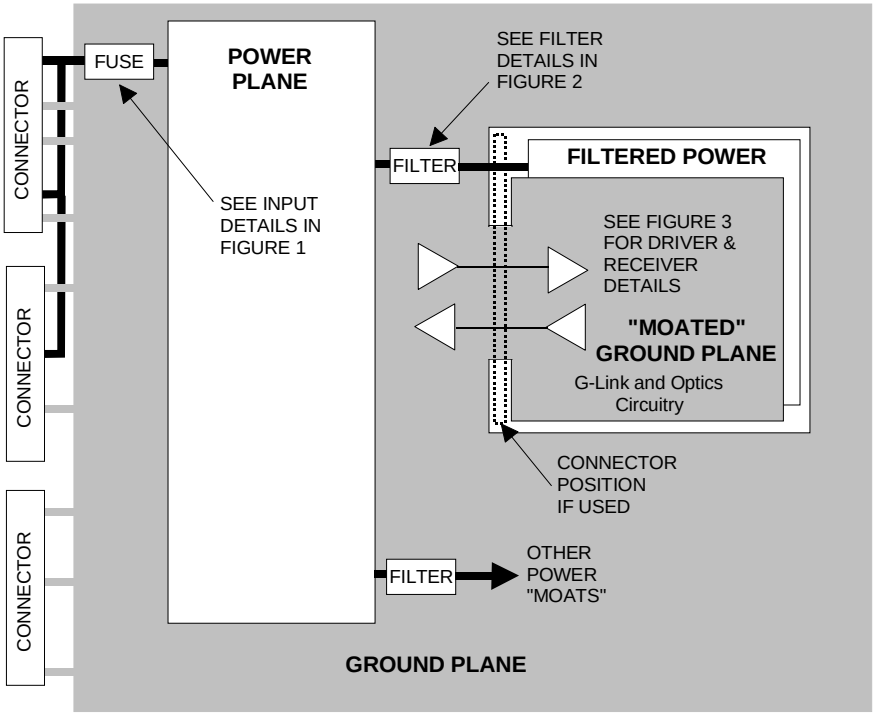

Figure 2
Overall Power and Ground Diagram

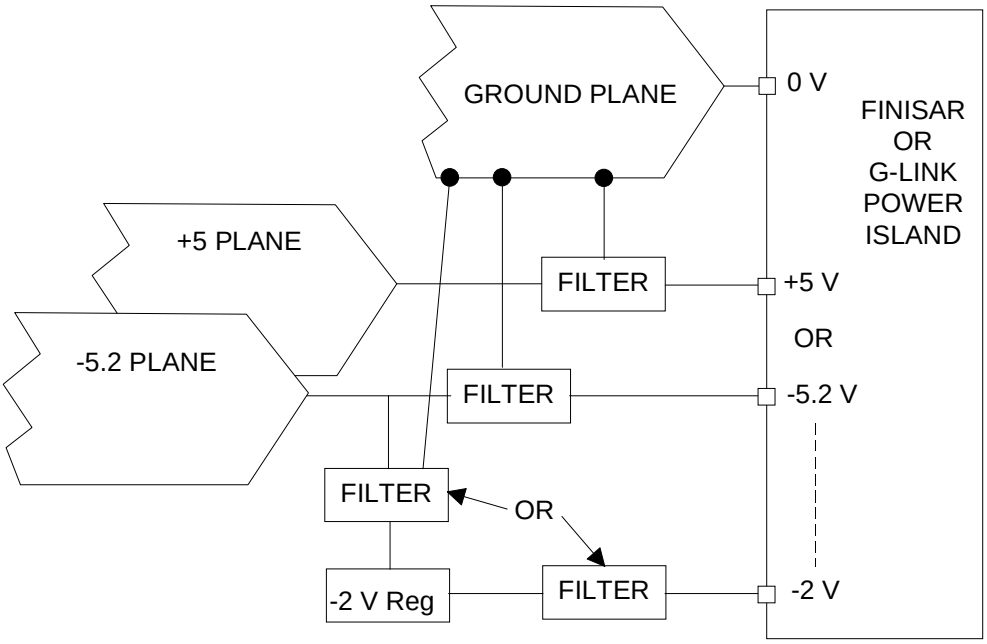

Figure 3
Power Feeds to Moated Power

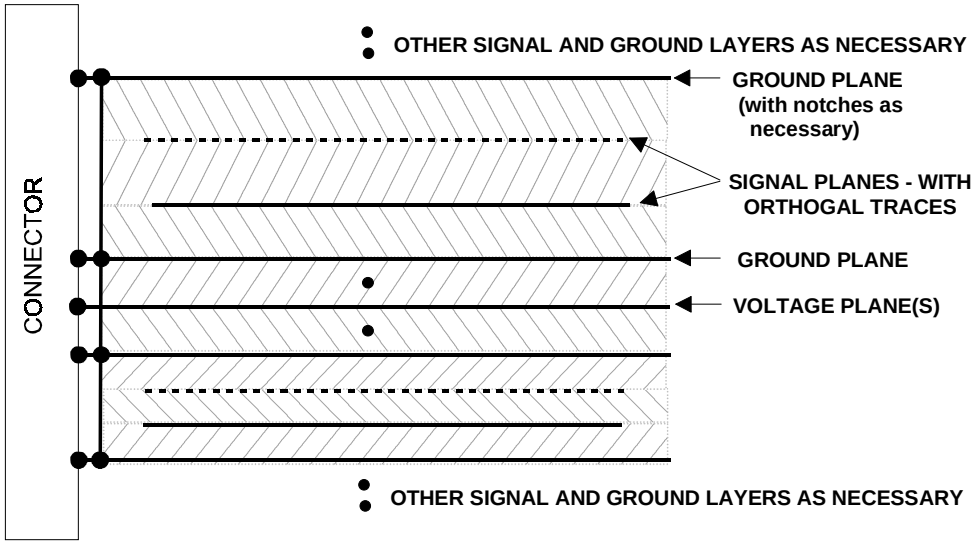

Figure 4
Printed Circuit Board Layer Stackup

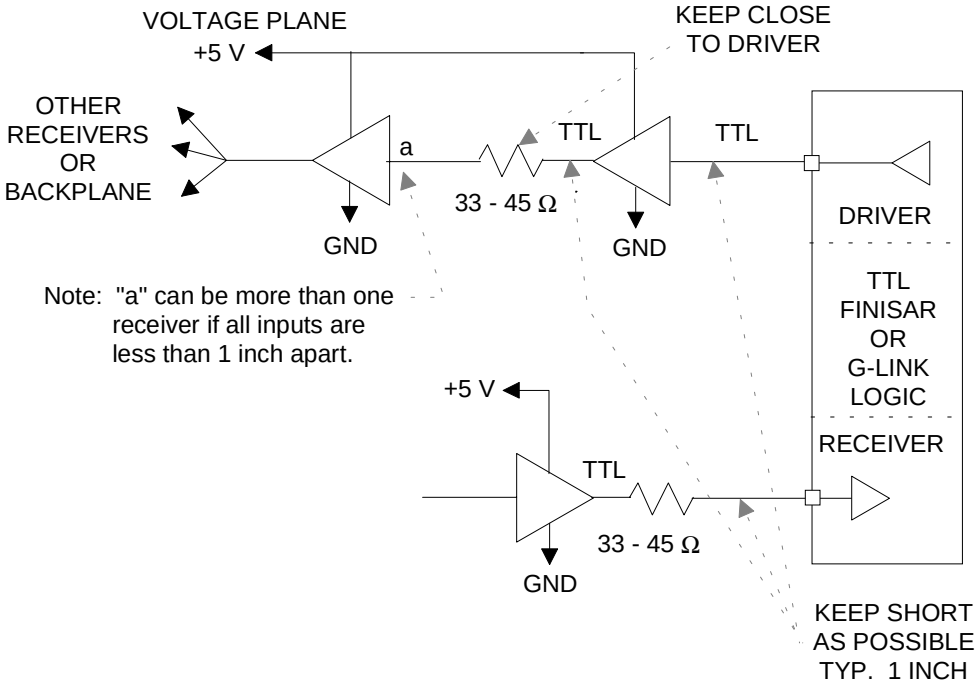

Figure 5
TTL Signal Connections from external to "Moats"

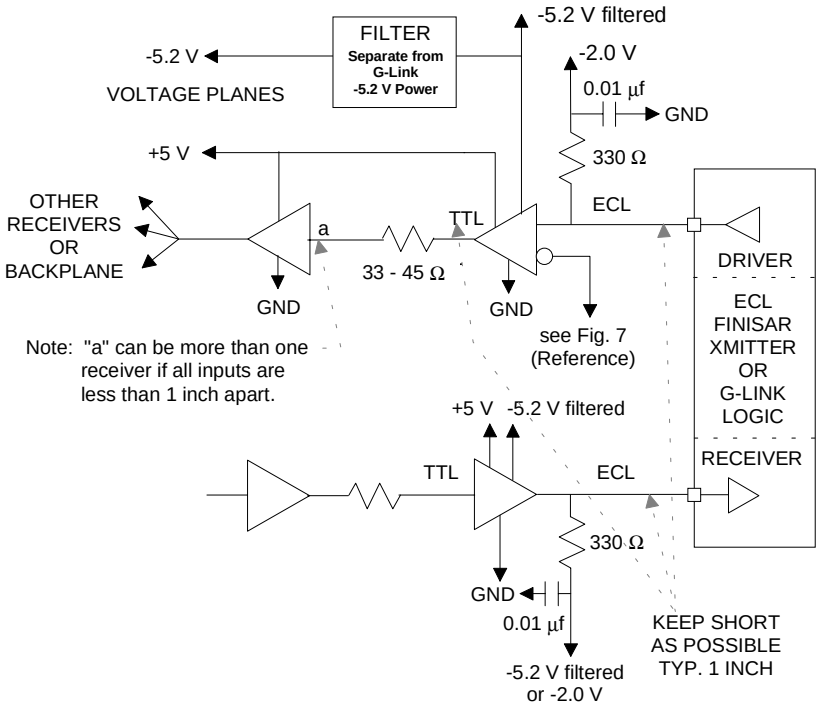

Figure 6
ECL Signal Connections
&
Filtered Power from external to "Moats"

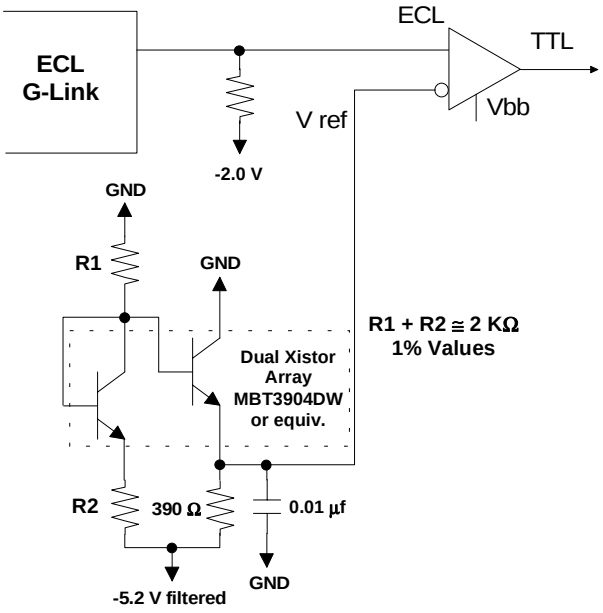

Figure 7
ECL Translator Adjustable Reference Voltage