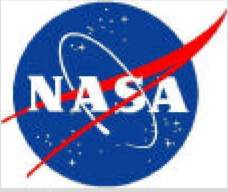

ELECTRONIC PACKAGING & SPACE PARTS NEWS

EEE Links

December 1998, Vol. 4 No. 4

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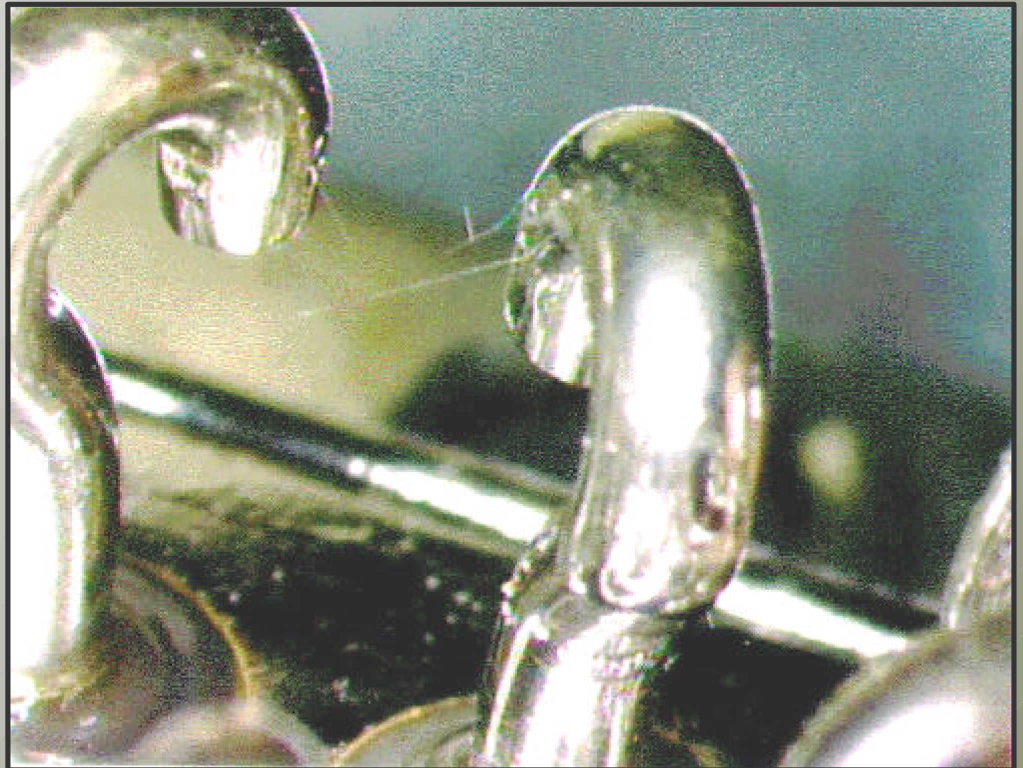

- ***Solid-State Non-Evaporable Getters to Maintain Vacuum in Hermetic MEMS Device Packages for Space Applications***

Editor: **Robert Humphrey, (301) 731-8625**
rhumphre@pop300.gsfc.nasa.gov
Mailing List Information and Article Submissions: (301) 731-8625
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An example of a tin whisker growing between pure tin plated hook terminals of an electromagnetic relay similar to MIL-R-6106 (LDC 8913)
Photo courtesy of Andre Pelham (Intern) Goddard Space Flight Center

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Letter from the Editor

Robert Humphrey
Editor of EEE Links
(301) 731-8625
rhumphre@pop300.gsfc.nasa.gov

Welcome to the December issue of EEE Links. As I mentioned in the last issue of EEE Links our URL address has changed. The new URL for EEE Links on the Web is http://misspiggy.gsfc.nasa.gov/ctre/hq/eee_links.

As always, please keep us informed of your questions and needs so that we may be able to serve you better.

Quality Assurance and Reliability: A System Approach

Dr. Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
(818) 354-2059
email: Reza.Ghaffarian@JPL.NASA.Gov

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of product development. Product development is a process that must provide a method for supplying measurement of customer expectations and preferences, competitive development, and existing product performance and respond to those results with continuous improvement. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment.

Chip scale package (CSP) rapid development and introduction into the market is a good example of this trend. The use of new materials, processes, and new applications obscure the traditional definition of quality and reliability assurance. New system approaches are needed to assure quality and reliability as well as to manage risks. Quality should be assured by design for reliability, controls for processes, tailored testing methods for qualification, and use of unique accelerated environmental testing along with credible analytical prediction. In other words, an efficient concurrent engineering system approach must be implemented.

Among the many environmental accelerated testing methodologies for assessing reliability of electronic systems, thermal cycling is the most commonly used for characterization of devices as well as interconnections. Among the many predefined thermal cycling profiles, the military and commercial aspects represent the two extremes. Previously, NASA also had a preset specific thermal cycling requirement. Although the Military Standard (MIL-STD-883) recently was obsoleted, it is still used for benchmark testing. Within MIL-STD-883, there are three levels of accelerated cycling temperatures:

- Condition A, -55/85°C
- Condition B, -55/125°C
- Condition C, -65/150°C

For benchmark conditions, devices are generally subjected to condition C and assemblies most often to condition B. The assemblies were traditionally considered qualified when they last 1,000 cycles. A commercial cycling profile from the J-12 IPC specification recommends a thermal cycle in the range of 0° to 100° C. Within a temperature range, the dwell, heat and cool down rates are critical parameters and also affect cycles to failure.

The NASA thermal cycling requirements are stringent and are specified in various revisions of NASA Handbooks. For example, in a previous revision, NHB 5300.4 (3A-1), there was a well defined requirement for number of cycles and solder condition after exposure. No cracking of any solder joint was allowed after 200 thermal cycles (-55 to 100°C with 245 minutes duration). In a subsequent revision, the requirements were based on meeting the specific mission condition. The build and test methodology is expected to yield confidence in reliability to satisfy the mission conditions. Mission requirements are emphasized rather than a universal cycle and a value for all missions.

Test to "establish the confidence in reliability" adopted by NASA a long-time ago is now "the reliability theme" for the commercial sector. Discussions on "Breaking Traditional Paradigms" and "Rethinking of Environmental Reliability Testing" by authors from the commercial sector are becoming hot topics with the introduction of new miniaturized CSPs. These packages have their own unique form factor

not seen in SMT. Unable to meet the stringent requirements established by the previous military standards, a new "paradigm shift" is considered to be the solution. The "shift" is further motivated by the reduction in life expectancy of electronic products in consumer applications. Rapid changes in electronic technology is given as another reason for adopting the paradigm shift. Obsolescence of many military specifications also has helped in such themes.

Additional unique tests are now adopted to meet the specific consumer products. For portable electronics, bend test, drop test, and possible "washing machine test" are used or suggested. IPC 9701, Qualification and Performance Test Methods for Surface Mount Solder Attachments, is aimed to include some of these requirements. It must be recognized that no accelerated tests can be truly universal. Field reliability is the ultimate test, and either substantiates or invalidates the experimental tests. For space missions, gathering information on the root cause field failure is almost impossible. For commercial applications, rapid changes in technology render field information almost useless for new product development. The only solution is to understand key reliability parameters and to design for reliability. Subsequent process controls, as well as efficient qualification and inspection, also help assure sufficient field reliability. In other words, risk control and risk management must be practiced.

Diamond Microstructures for Microelectromechanical Systems (MEMS)

Rajeshuni Ramesham
JPL, California Institute of Technology
(818) 354-7190 Fax: (818) 393-5245
e-mail: rajeshuni.ramesham@jpl.nasa.gov

Diamond thin film has been grown on Si and SiO_2 substrates using microwave plasma Chemical Vapor Deposition (CVD) from a gas mixture of CH_4 and H_2 at a substrate temperature of 950°C.

- A process flow has been developed to fabricate diamond membranes employing Reactive Ion Etching (RIE) of silicon using e-beam evaporated aluminum mask pattern formed by photolithography.
- Selective diamond film has been grown on a SiO_2/Si substrate using microwave plasma CVD. A simple process flow has been developed to fabricate diamond microstructures such as diamond beams and cantilever beams using surface micromachining and photolithography.

Growth of diamond films using microwave plasma CVD has received significant interest in recent years, since it has unique chemical and physical properties for potential MEMS applications. In order to facilitate application of diamond films for MEMS, a technique to fabricate diamond microstructures or mechanical components is desirable.

MEMS is a microelectronics fabrication approach to miniaturize the electromechanical sensor devices and integrate with the IC fabrication processes. MEMS devices may have a significant application in automotive, displays, printers, fluid thrusters, analytical instruments, communications, biomedical, and aerospace industry. Operation, reliability, sensitivity, and stability of smaller, lighter, and cheaper MEMS devices is very critical in any chosen application particularly under extreme shock and ambient temperature conditions. These MEMS devices should be built in along with other semiconductor devices using integrated semiconductor fabrication technologies. New material such as silicon carbide and diamond and their process technology to fabricate the MEMS devices is necessary for high temperature applications where silicon may not be applicable at temperature more than 150°C. MEMS devices may have a use to monitor a wide variety of parameters such as temperature, accelerations, flow rates, pressures, vibrations, surface wear rates, fluid contaminants, position sensing, etc.

A. DIAMOND MEMBRANES BY USING REACTIVE ION ETCHING

We describe a process flow combined with photolithography and reactive ion etching of silicon to fabricate diamond membranes for MEMS applications. We have used a well-established reactive ion high etching of silicon to fabricate diamond membranes to enhance the yield of diamond microstructures. This approach is three to six times faster than the hot KOH anisotropic etching process.

A microwave plasma CVD system was used in our experiments to grow diamond films. Starting substrates were mirror-smooth finished n- or p-type, (100) oriented single crystal silicon wafers with a resistivity of <20 ohm-cm. The wafers were cleaned in acetone, methanol, deionized (DI) water, and dried with nitrogen gas. A continuous film of polycrystalline diamond was usually obtained after 15 - 20 hours of growth. Growth rate of microwave plasma CVD diamond is typically 1 μm/hour.

The aluminum was deposited on the backside of the CVD diamond grown silicon substrate by e-beam evaporation. The aluminum was then photolithographically patterned and etched using phosphoric and acetic acid etching solution. The photoresist was cleaned with acetone, rinsed with methanol, DI water, and finally dried with nitrogen gas.

RIE has been employed to etch silicon to fabricate diamond membranes. The parameters employed in this etching process are as follows:

- SF_6 flow rate = 10 sccm,
- O_2 flow rate = 10 sccm,
- RF forward power = 295 watts,
- Reflected RF power = 0 watts, and
- DC bias = 22 watts.

The total silicon wafer thickness was 630 μm in this study.

A process has been developed and demonstrated to fabricate diamond membranes on a silicon substrate using RIE of silicon. Bulk micromachining of silicon has been performed using KOH solution in the literature to fabricate diamond membrane. The etching rate of silicon in hot KOH solution is ~1 μm/min and is anisotropic in nature. It has been quite a routine process such as bulk micromachining the silicon for MEMS applications. Therefore, we have attempted to fabricate diamond membranes using silicon bulk micromachining process using dry reactive ion etching process. In silicon MEMS devices, an etch stop layer is needed to fabricate microstructures. RIE plasma will not attack the diamond, which will be an advantage for diamond MEMS applications. This approach can be used to fabricate any diamond microstructure successfully for MEMS applications.

B. DIAMOND CANTILEVERS AND BRIDGES BY SURFACE MICROMACHINING

It is necessary to ultrasonically damage the silicon dioxide/silicon substrate to enhance the nucleation density of diamond. In order to facilitate application of diamond films for MEMS, a surface micromachining technique has been developed to fabricate diamond microstructures such as bridges and cantilever beams.

Bulk micromachining means that three-dimensional features are etched into the bulk of crystalline. In contrast, surface micromachined features are built up, layer by layer, on the surface of a single crystal silicon substrate. Dry etching or selective deposition defines the surface features in the x,y plane and wet etching releases them from the plane by undercutting.

The nature of the deposition processes involved determined the very flat surface micromachined features. The CVD diamond films generally are only a few microns high such as low z. In contrast with wet bulk micromachining only the wafer thickness limits the feature height.

Microscale movable mechanical pin joints, springs, gears, sliders, sealed cavities, and many other mechanical and optical components have been fabricated using surface micromachining of polysilicon. Analog Devices have commercialized ADXL-50 a 50-g accelerometer that was developed using surface micromachining for activating air-bag deployment. Texas Instruments' Digital Micromirror Device is also based on surface micromachining.

We describe a process flow combined with conventional photolithography and a technique of selective deposition of diamond over silicon dioxide/silicon substrate to fabricate diamond beams and cantilever beams for MEMS applications using surface micromachining approach. This is only possible since we can grow diamond over the silicon dioxide/silicon substrate. We have used an approach of selective deposition of diamond over silicon dioxide/silicon substrate to fabricate diamond microstructures to enhance the yield of diamond microstructure fabrication.

Starting substrates were mirror-smooth finished n- or p-type, (100) oriented single crystal silicon wafers with a resistivity of <20 ohm-cm. Cleaned silicon wafers were thermally oxidized to a thickness of 1 to 1.5 µm. Selectivity of diamond films on silicon dioxide was achieved by the following two distinct processes described below.

- Oxidized silicon wafer was damaged by ultrasonic agitation for 15 – 60 minutes. The ultrasonically damaged SiO_2 was then photolithographically patterned and partially chemically etched in the opening of the photoresist using a solution of BOE to smooth the surface so that no diamond growth would result. The photoresist was removed with a stripper solution, and the resist residue was removed with oxygen plasma.
- The silicon dioxide was photolithographically patterned and hard baked with the photoresist at 150 – 200°C for 1 – 2 hours. The sample was ultrasonically agitated for 15 – 60 minutes and the photoresist was stripped with a stripper solution. The substrate was eventually cleaned in oxygen plasma. This approach resulted in selectively damaged patterns of silicon dioxide so as to yield diamond growth only there.

The wafers were cleaned in acetone, methanol, deionized water, and dried with nitrogen gas. A continuous film of diamond was usually obtained after 15 - 20 hours of growth. The silicon dioxide/silicon substrate was cleaned thoroughly with various solvents after the selective CVD diamond growth over the silicon dioxide. The substrate was baked at 175 – 200°C for 15-20 minutes and later spin coated the adhesion promoter and subsequently spin coated thick photoresist. Soft baking the substrate for 30 minutes, patterned the photoresist using optical photolithography. The photoresist was developed using developer solution. The patterned diamond/silicon dioxide/silicon substrate was hard baked at 110 –120°C for 15 – 20 minutes and the silicon dioxide was etched using BOE, which is a surface micromachining process, to yield diamond microstructures. Diamond microstructures for MEMS were fabricated using selective diamond deposition over silicon dioxide/silicon substrate and surface micromachining of silicon dioxide process using BOE. A process has been developed and demonstrated to fabricate diamond beams and cantilever beams on a SiO_2/Si substrate using selective diamond deposition and surface micromachining process.

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NASA Eastern Region Training Center Update

Theresa James
Hernandez Engineering
NASA/GSFC
Teresa.A.James.1@gsfc.nasa.gov
(301) 731-8604

The NASA Training Center has added two new courses, namely Fiber Optics training based on NASA 8739.5 "Fiber Optic Termination, Cable Assemblies and Installation" and Poly Applications training referencing NAS 5300.4 (3J-1) "Workmanship Standard For Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies".

The Polymeric Applications course provides instruction to those who are responsible for applying polymeric materials. The course emphasizes practical, hands-on training for staking, conformal coating, potting, shielding, and bonding requirements for space flight hardware. In addition students will become familiar with the NASA workmanship standard and inspection techniques unique to polymer coated assemblies.

The Fiber Optic course teaches operators, inspectors and engineers how to prepare optical fibers and fiber optic cables for termination, the proper techniques for splicing or installing connectors, and acceptance criteria. Extensive laboratory research has identified specific procedures necessary for installing connectors whose performance must remain reliable throughout mission lifetimes. These procedures are a key part of this course. Students will build inspect and test their own fiber optic cable assemblies using techniques developed specifically to address reliability issues unique to fiber optic technology intended for space applications. Illustrations, detailed documentation, and demonstrations of techniques are

used to explain each process from stripping the fiber through polishing, and then inspection and testing of the completed assembly.

To learn more about these classes or any of the other many classes currently offered, call the Training Center at (301) 286-8632 or visit our web site at

http://arioch.gsfc.nasa.gov/312/train.htm

Tin Whiskers: Revisiting an Old Problem

Jay Brusse
Unisys Corp. at NASA Goddard
(301) 286-2019
Jay.A.Brusse.1@gsfc.nasa.gov
http://misspiggy.gsfc.nasa.gov/ctre

Recent events have reminded the space community of the potential risks associated with the use of pure tin-plated finishes on electronic components and assemblies. Pure tin finishes are susceptible to the spontaneous growth of single crystal structures known as ***tin whiskers***. Tin whiskers are capable of causing electrical failures ranging from parametric deviations to catastrophic short circuits. Although the tin whisker phenomenon has been documented for decades and is reasonably well understood, it is still a reliability hazard that warrants special attention.

This article does not provide a complete explanation of the tin whisker growth mechanism; numerous (often contradictory) publications have attempted this task. The intent is to provide a comprehensive explanation of generally accepted understandings of tin whiskers along with some suggestions for how to reduce the risk of tin whiskers on spaceflight hardware. In addition, Goddard Space Flight Center is maintaining a Tin Whisker Information Homepage to provide regular updates to facts and findings as they become available. This homepage can be found at the following URL:

http://misspiggy.gsfc.nasa.gov/ctre

WHY TIN?

The electronics industry has utilized pure tin plated finishes for decades. Tin forms an excellent protective coating that resists oxidation and corrosion and also provides good solderability. In addition, pure bright tin finishes (those which use chemicals called "brighteners" in the plating bath) maintain an aesthetically pleasing shiny surface even when exposed to air and moisture. Tin is also preferred by manufacturers over tin-lead plating because lead in waste streams increases the cost and complexity of disposal. These are a few reasons why pure tin plating has become a common termination finish for Commercial-Off-The-Shelf (COTS) components.

PURE TIN PROHIBITION IN THE MILITARY SPECIFICATION SYSTEM:

Following a series of tin whisker related failures in the late 1980's and early 1990's the U.S. Military sought to eliminate pure tin from its systems. Between 1992 and 1993, language was introduced into most of the MIL EEE part specifications to specifically prohibit the use of pure tin plating. Notable exceptions were the specifications for electromechanical relays. Two of these specifications, MIL-R-6106 and MIL-R-83536, did not prohibit tin on external surfaces until they were converted to performance specifications (PRF) in 1997.

In some Military EEE part specifications, pure tin finishes are still a specifiable option (i.e., the user can choose pure tin finishes and clearly identify this option by a character in the part number). One example of this situation exists with ceramic chip capacitors made in accordance with MIL-PRF-55681.

A BRIEF DESCRIPTION OF TIN WHISKERS:

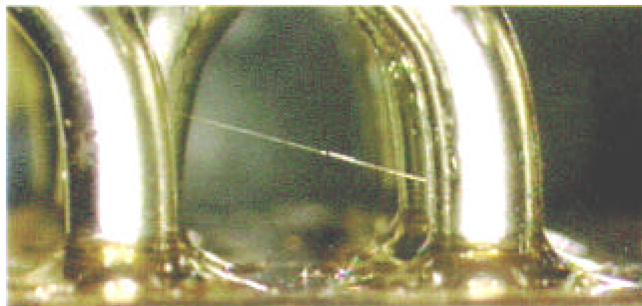
The following list describes some of the generally accepted characteristics of tin whiskers and their formation:

Whiskers are elongated single crystals of pure tin that have been reported to grow to more than 4 mm (160 mils) in length and from 0.3 to 10 μm in diameter (typically ~1 μm).

Whiskers grow spontaneously without an applied electric field or moisture (unlike dendrites) and independent of atmospheric pressure (they grow in vacuum).

They may be straight, kinked, hooked or forked and some are reported to be hollow. Their outer surfaces are usually grooved.

Whisker growth may begin soon after plating or may take years to initiate.



An example of a tin whisker growing between pure tin plated hook terminals of an electromagnetic relay similar to MIL-R-6106 (LDC 8913)
Photo Courtesy of Andre Pelham (Intern)
Goddard Space Flight Center

TIN WHISKER GROWTH MECHANISM:

The mechanism(s) by which tin whiskers grow has been studied for many years. A single accepted explanation of this mechanism has not been established but there are some commonly agreed upon factors involved in tin whisker formation. Tin whisker growth is primarily attributed to stresses in the tin plating. These stresses may be from many sources including:

- Residual stresses in the tin resulting from the plating process. Electrodeposited finishes are most susceptible due to the high current densities involved in the plating process.
- Compressive stresses such as those introduced by torquing of a nut or a screw
- Bending or stretching of the surface after plating
- Scratches or nicks in the plating introduced by handling
- Coefficient of Thermal Expansion mismatches between the plating material and substrate
- The change in lattice spacing that occurs from the formation of intermetallic compounds such as those between copper and tin.
- Whiskers appear to grow more readily at temperatures approaching 50°C. Whiskers growth appears to cease at temperatures higher than about 140°C and lower than around –40°C.
- Bright tin finishes (shiny) seem to be worse than matte finishes due to some influence of the organic compounds used as brighteners.

POTENTIAL RISKS OF TIN WHISKERS:

Tin whiskers pose a serious reliability risk to electronic assemblies. Several instances have been reported where tin whiskers have caused system failures. The general risks fall into four categories:

(a) Whiskers or parts of whiskers, may break loose and bridge isolated conductors or interfere with optical surfaces

(b) In low voltage, high impedance circuits, there may be insufficient current available to fuse the whisker open and a stable short circuit results. Depending on the diameter and length of the whisker, it can take more than 50 milliamps (mA) to fuse one open. More typical is ~10 mA

(c) At atmospheric pressure, if the available current exceeds the fusing current of the whisker, the circuit only experiences a transient glitch as the whisker opens.

(d) ***In space vacuum*** however, a much more destructive phenomenon can occur. If currents of above a few amps are available, the whisker will fuse open but ***the vaporized tin may initiate a plasma that can conduct over 200 amps!*** An adequate supply of tin from the plated surface is necessary to sustain the arc.

OFFICIAL ALERT HISTORY:

Numerous GIDEP Alerts and Problem Advisories have been issued that cover specific occurrences of tin whisker related failures. Although these alerts and advisories show a bias towards relays and other devices typically packaged in metal cans, any surface plated with pure tin is potentially at risk for tin whisker formation.

SUGGESTIONS FOR REDUCING THE RISK OF TIN WHISKERS:

At this time, the only sure way of avoiding tin whiskers is not to use pure tin plating. Utilization of procurement specifications that have clear restrictions against the use of pure tin plating is highly recommended. Most (but probably not all) of the commonly used military specifications currently have prohibitions against pure tin plating. Studies have shown that alloying tin with a second metal reduces the propensity for

whisker growth. Alloys of tin and lead are acceptable where the alloy contains a minimum of 3% lead by weight.

If there is no alternative to using pure tin plated finishes, it is recommended to solder dip the plated surfaces sufficiently to completely reflow and alloy the tin plating. Obviously, special precautions are required to prevent thermal shock induced damage, to prevent loss of hermeticity and to avoid thermal degradation. Some manufacturers may be willing to strip the pure tin plate from finished products and re-plate using a suitable alternate plating material such as tin/lead.

Other treatments such as conformal coating and foam encapsulation appear to be beneficial but the limitations are not understood. It has been reported that tin whiskers can grow through conformal coating. It has also been demonstrated experimentally that conformal coating can restrict the availability of tin sufficiently to prevent plasma formation. However, such factors as the minimum thickness of coating necessary to prevent whisker growth or plasma formation have not been determined. Similarly, it has been shown that foam can prevent sustained arcing but the effects of foam type, foam density, pore size etc. have not been evaluated.

Additional studies and evaluations are underway to try to answer the critical open questions in order to provide more detailed suggestions in the future. For the latest available information visit the tin whisker homepage at:

http://misspiggy.gsfc.nasa.gov/ctre

Solid-State Non-Evaporable Getters to Maintain Vacuum in Hermetic MEMS Device Packages for Space Applications

Rajeshuni Ramesham
JPL, California Institute of Technology
(818) 354-7190 Fax: (818) 393-5245
e-mail: rajeshuni.ramesham@jpl.nasa.gov

Many high sensitivity microelectromechanical systems (MEMS) need to operate in a hermetically sealed vacuum electronic package to realize their full performance. This vacuum is destroyed by outgassing of various species such as water vapor, hydrogen, carbon monoxide, nitrogen, oxygen, and carbon dioxide from the package surfaces and microleaking or permeation through the package body. The loss of vacuum is particularly serious if organic materials are used in an isolated MEMS packaging device. A getter material is needed to eliminate this problem and achieve successful MEMS device operation for long duration space applications. The term "getter" refers to materials, which chemically sorb active gases in a vacuum environment. A solution is proposed using a SAES non-evaporable high porosity getter material family (Zirconium-aluminum-iron, titanium, thorium, etc.) to solve the hermetic sealing problem associated with the micro-gyro and other similar MEMS devices where hermetic sealing is required. The getter consists of a highly porous and mechanically stable packaging component that will be installed inside the MEMS vacuum packaging chamber and activated.

A variety of sealed-off devices such as cathode ray tubes (CRT's), electron tubes, plasma displays, particle accelerators and colliders, vacuum thermal insulation, ultra-high vacuum systems for semiconductor processing, X-ray tubes, lamps, field emission displays (FEDs) require a vacuum for their successful operation. Maintaining vacuum in extremely small volume packages depends on the surface area of materials exposed to that volume that are sources for species to be outgassed and finally that will destroy the vacuum. Getters are routinely used in larger static systems and similarly getters will be needed if the desired system lifetimes of many years are to be obtained in MEMS packages for space applications.

The solid-state getters may be either planar or three-dimensional and exhibit good mechanical strength. They must be particle free under the stringent operational conditions in space and on the ground, and they should have a high active surface area that can easily be activated at low temperatures. This minimizes problems such as high ambient temperature that may be detrimental to MEMS devices during activation. High porosity combined with a large active surface area will assure excellent sorption performances at room temperature. There should not be any loss of getter particles before, during, or after activation of the getter in a packaged MEMS device

as this may cause failure of the MEMS device. It is critical to maintain the getter's mechanical structure during shocks and vibrations at the time of spacecraft launch and during operation of the MEMS device. The presence of an activated getter material inside the MEMS package will allow achievement of a better vacuum in the hermetically sealed vacuum package. The presence of a getter material inside a MEMS package is needed to avoid a pressure increase above the operational limit of the MEMS device. Sorption of outgassed species by getters permits a greater anticipated lifetime for MEMS devices in hermetically sealed packages. A procedure to activate the getter inside a MEMS package for possible space applications is proposed.

Activation of the non-evaporable getter may be achieved using the following procedure that may be appropriately modified for a particular MEMS device:

- The activation parameters are temperature, pressure, time, and method of heating.
- Getters should be handled only with clean tools, rubber or plastic gloves and never with bare hands.
- Getters may be ultrasonically agitated in high purity isopropyl alcohol (IPA) for a few seconds and dried in an oven.
- For long-term storage, a clean, dry ambient is desirable. Getter may be stored in a phosphorus pentoxide or a silica gel air desiccator, a vacuum desiccator, or under a dry nitrogen atmosphere.
- Weld the getter appropriately in the MEMS packaging container.
- Pump until the pressure in the MEMS packaging chamber is less than 1×10^{-6} Torr or 1×10^{-4} Pascals.
- Activate the getter by heating to the activation temperature of the getter material. The activation temperature and time are functions of the getter material and the activation technique.
- Activation of the getters may be accomplished by joule heating or resistance heating.
- The heating rate of the getter should be controlled to avoid excessively high system pressure due to outgassing. The time required to attain activation temperature should not be included in activation time at the activation temperature.
- Monitor the maximum pressure during activation using pressure gauge; this will give the relative value of the gas content of the getter.
- Allow the getter to cool to its test temperature while pumping down. Pinch off will be performed carefully at the final stage.

Specification Coordination Meeting for Space-Level Stacked Ceramic Capacitors

Jocelyn Siplon
The Aerospace Corporation
Jocelyn.P.Siplon@aero.org

During the week of September 14, 1998 a coordination meeting was held at the Defense Supply Center Columbus (DSCC) in Ohio to discuss the minimum requirements for military specified "***space/hi-rel***" stacked ceramic capacitors (also known as switch-mode-power-supply [SMPS] capacitors). The objective of the meeting was to determine an appropriate vehicle for developing space level requirements for SMPS capacitors. SMPS capacitors are becoming more popular with power supply designers because of the high capacitance values, volumetric efficiency and performance characteristics they offer. However, the present revisions of military specifications covering SMPS capacitors (DSCC-DWG-87106 and the new MIL-PRF-49470) do not have adequate requirements to provide the long-term reliability required for some space applications.

All domestic suppliers of stacked ceramic capacitors were represented at the meeting. In addition, the U.S. Military, NASA Goddard, the Jet Propulsion Laboratory (JPL) and the Naval Surface Warfare Center (NSWC)-Crane were also in attendance. In general, the government representatives received agreements from the manufacturers on the most critical issues. Some compromises were made, particularly with respect to sample sizes required for space level lot conformance testing. These compromises will not degrade the quality of the parts delivered because the rest of the requirements should be sufficient to disqualify any marginally designed parts. The space-level SMPS capacitors will have to

meet requirements very similar to MIL-PRF-123 (the current military specification that provides space-level requirements for non-stacked ceramic capacitors). These requirements include the 4,000-hour life test qualification.

The following highlights the discussion points and agreements arrived at during the meeting with respect to space level ("T" level) product:

- The space-level (presently designated as "T" level) requirements will be incorporated into the main body, qualification, Group A, and Group B tables of the existing MIL-PRF-49470 as an option for manufacturers who wish to supply the high reliability product. Suppliers who qualify to T-level will automatically be QPL listed for the equivalent general-specification (non-space) parts.
- New slash sheets will be generated for space-level parts. These slash sheets will then become the designators for T-level parts in the part numbering scheme. (For example, the slash sheet designation in the part number will uniquely define whether the part is "space level" or general level).
- Chip-level in-process inspection, which includes 100% non-destructive testing (such as Acoustic Microscopy [SLAM or CSAM]), lot-sample DPA, and 100% visual examination, will be required for every chip lot used to make the capacitor stacks.
- Single-chip-lot requirement is imposed when forming each lot of stacked capacitors.
- Qualification will consist of the tests described in the present qualification table in MIL-PRF-49470 except:
  - (a) All stacks will be subjected to 100 cycles of thermal shock at the beginning of qualification,
  - (b) Burn-in will have the reduced Percent Defective Allowable (PDA) during the last 48 hours much like in MIL-PRF-123,
  - (c) Terminal strength will be performed,
  - (d) Low-voltage humidity test (85°C/85% Relative Humidity) and DPA on the stacks are required, and
  - (e) 4,000 hrs of life test is required.
- No "C" level reliability (commercial version) will be added to MIL-PRF-49470, since the present DSCC-DWG-87106 parts are already considered to be "commercial".
- The 0.8 mil minimum dielectric thickness will be added to the specification. However, no maximum dielectric constant requirement (such as in MIL-PRF-123) will be specified. Users will have to rely on performance requirements (such as VTC, and lot-by-lot Group A & B testing) to gain confidence in the electrical, thermal and mechanical properties of the ceramic.
- Solder temperature requirement will be the same as in MIL-PRF-123.
- Para. 5.1 "Delaminations" in EIA RS-469 Rev B will be added to the DPA requirements in MIL-PRF-49470, because the present language in the latest revision of RS-469 (Rev C) does not apply to large ceramic capacitors.
- Leadframe brackets (or tabs) will not be removed from the drawings even for the low-profile parts.
- All of the Group A & B test sequence in MIL-PRF-123 will be adopted for T-level stacked capacitors except voltage-temp limits, which will not be a lot-by-lot Group B requirement. Instead, this parameter will be monitored through the qualification maintenance program. Also, the post burn-in hot IR test will follow immediately after burn-in so that parts can be IR tested while still in the burn-in oven.
- Failure during the last 48-hours of burn-in will be indicated by either a blown fuse, or high-temp IR measurement that does not meet the minimum specification limit.
- Under "Verification of Qualification", para. 4.5.b will be changed to read: "The basic capacitor design & construction, basic materials and critical processes have not been modified without prior approval from the qualifying activity."
- Para. 4.7.10.2.e "Insulation Resistance at 125°C" will be changed to read: "The vendor may determine criteria tighter than the specification limits to which parts may be screened. Only parts which do not meet the specification limit shall be considered against PDA." This allows the manufacturers to guardband the hot IR values of outgoing parts, which is better for the user, with-

out penalizing them for those that fail to meet the "guardband" values.

- An expanded visual inspection criteria will be incorporated in MIL-PRF-49470, and will apply to both T-level and general-specification parts.
- The manufacturer will be allowed to downgrade a lot from T-level to general-specification if a failure occurred after 1,000 hours of life testing. During T-level qualification, intermediate readings during the 4,000-hr life test will be required at 250 hrs and 1,000 hrs, but the manufacturer has the option of doing additional intermediate measurements, such as at 2,000 hrs.
- The statement "Each voltage and case size produced should be represented at least once every 12 months." provides assurance that the same part types/designs are NOT being life tested all the time.
- The life test requirement "No more than 1 failure allowed in two consecutive quarters" will not apply when the manufacturer is maintaining T-level qualification.

One, if not more, manufacturer has already started the qualification process for the general specification product offered by MIL-PRF-49470. This supplier is expected to complete qualification by the end of 1998 or early next year. Qualification to the space-level product offered by MIL-PRF-49470 will likely follow in 1999 pending the development and release of the revised base specification with the "T" level requirements and the accompanying space level slash sheets. Please contact Mr. Mike Radecki of DSCC at 614-692-0561 for progress and/or release dates of these documents.

Cable Bundle Wire Derating

Ray A. Lundquist
NASA Goddard/Code 565
Ray.A.Lundquist.1@gsfc.nasa.gov
Dr. Henning Leidecker
NASA Goddard/Code 562
ME@Leidecker.gsfc.nasa.gov

A proposed redesign of a power distribution system in the Hubble Space Telescope (HST) would increase the current passed through each of four 20 AWG wires at the core of a particular wire bundle from 2 A to as much as 6.0 A. There are twenty-four other wires acting as a shell around the core wires; the maximum current per wire is 3.0 A. The governing specification document applies to a surrounding enclosure at 70°C, and prohibits currents above 3.7 A through each 20 AWG wire in a bundle of 15 (or more) wires. However, the surrounding enclosure during HST operations would usually be near 12°C, and would never be above 25°C; this, together with the 3.0 A (not 3.7 A) current through the shell wires, means that the conditions of the governing specification document do not apply.

The steady-state temperature T_{core} of the core wires must be the temperature of the surrounding enclosure T_e plus increases caused by the joule powers dissipated in the core and in the surrounding shell. These powers must in turn be related to the squares of the current I_{core} in the core wires and the current I_{shell} in the shell wires:

$$T_{core} = T_e + \alpha(T_{core}) \cdot I^2_{core} + \beta(T_{shell}) \cdot I^2_{shell},$$

where $\alpha(T)$ and $\beta(T)$ measure the temperature-dependent effects of the wires' electrical resistances and heat-shedding abilities. Available documents do not provide guidance for estimating the temperature increase of the core wires for any currents of interest, nor guidance for estimating $\alpha(T)$ or $\beta(T)$. Further, the fundamental parameters of the system were not known well enough to permit a computation of $\alpha(T)$ or $\beta(T)$ using thermal modeling methods.

Therefore, a thermal vacuum test was conducted on a wire bundle constructed to closely resemble the one in the power distribution system. The results were used to determine $\alpha(T)$ and $\beta(T)$. The measured temperature T_{core} of the core wires is fit to within several degrees (usually better) over conditions spanning more than the full range of conditions expected to be encountered during HST operating conditions. The temperature T_{core} of the core wires was always well under the maximum allowed for the wires, under all planned HST operating conditions.

Raising the temperature of the surrounding enclosure to 70°C, and passing the same 3.7 A current through each shell and core wires, increased the temperature T_{core} of the core wires to 139°C. The fitted model predicts that increasing the current to 5.3 A would raise the temperature to 200°C, which is

the rated maximum. Thus, the specification has a tacit derating, and limits the current to 70% of the value that would bring the wires' temperature to the rated maximum value, for this particular bundle.

1.0 INTRODUCTION

The Hubble Space Telescope (HST) Power Distribution Units (PDUs) are the primary distribution points of electrical power for the HST electrical system. The PDUs accept high power, fused, solar array and battery power from the Power Control Unit (PCU), fuse this power into lower current services, and distribute it to all the HST loads.

The output services from the PCU use either 16 AWG or 20 AWG wiring, depending on load requirements that were set two decades ago. The wire used within the PDU is Kapton-insulated, multistranded, silver-coated copper wire with a maximum temperature limit of 200°C. (Connections are either crimped, or are heat-sunk such that the connections remain well below the melting temperature of eutectic lead-tin solder, 183°C.) The specification for the wire is MIL-W-81381/17-20-4.

A proposed design modification would increase to as much as 6.0 A the current through each of four 20 AWG wires in a bundle of 28 wires within the PDU. This produces a possible conflict with the Goddard Space Flight Center (GSFC) Preferred Parts List (PPL). The PPL specifies that the maximum current through a single 20 AWG wire be limited to 3.7 A when that wire is present in a bundle of 15 wires or more, in a vacuum, and in an environment whose ambient temperature is 70°C.

However, the PDU wiring of concern is operating in an environment whose nominal temperature is 12°C and whose maximum temperature is 25°C, not 70°C. In addition, most of the other wires in the bundle (24 of the 28) will be carrying no more than 3.0 A at any time: not all 28 wires will be simultaneously loaded to 6.0 A. Further, not all the wires in the bundle are 20 AWG; many are 16 AWG. Each of these factors lowers the temperature of the four core wires relative to the case considered by the PPL. Since the precise conditions named by the PPL are not present, then the 3.7 A limit specified by the PPL does not apply; the PPL does not provide guidance in the case of present interest. Other guideline documents were also consulted, but offered no guidance. Finally, estimating the temperature rise using a radiative transfer model is not an option since various required parameters, such as the surface emissivity of these wires and the heat current coupling between the wires, are not known to the required accuracy.

To determine if the operating conditions described above will present a potential failure point, or even a hazard, a thermal vacuum test was performed under conditions designed to match the actual operating conditions to the greatest extent possible.

2.0 TEST SET-UP

A bundle was constructed using the same wire and assembly procedures that had been used to construct the PCU bundle. In particular, the Kapton insulation was matched in color, to match the radiative properties of that used in the PCU bundle. The bundle is two feet in length, and contains a total of 28 wire segments. One long wire was zigzagged back and forth to create the shell of 24 wire segments, and another wire was zigzagged to create the four core wires of present interest. This arrangement ensured that the same core current I_{core} passed through each of the core wires, and the same shell current I_{shell} passed through each of the shell wires.

There are two differences. Only 20 AWG wire is used in the test bundle, while the HST bundle has many 16 AWG wires in it. The ends of the test bundle are not attached to connectors, while the HST bundle has a multipin connector at each end. Both differences lower the temperature of the HST bundle relative to the test bundle, making the test a conservative one.

Four thermocouples were installed into the test bundle. These were type T thermocouples, with 30 AWG wire diameter. Each thermocouple (TC) was placed next to a selected wire being measured, and fastened with lacing cord. To provide a measure of the bulk temperature of the wires being measured, 7 mil aluminum tape was wrapped around the bundle and the thermocouple. A Kapton tape over-wrap of the aluminum tape was provided to maintain thermal radiative properties similar to the Kapton wire insulation. TC#1 and TC#4 were each fastened to an outer wire (shell wire); TC#1 was about 6.5 inches from the bottom of the bundle and TC#4 was about

6.5 inches from the top. TC#2 and TC#3 were fastened to an inner wire (core wire); TC#2 was about 10 inches from the bottom of the bundle and TC#4 was about 10 inches from the top.

The wires were collected into a bundle so that each wire retains its relative position radially within the bundle, as it moves from one end to the other. (The wires were not "woven" into a braid or a rope.) In particular, the core wires are at (or near) the radial center, everywhere from one end of the bundle to the other, and the shell wires are at (or near) the surface of the bundle, everywhere from one end to the other. Cable ties were used every four inches along the bundle and tensioned using a Panduit Tie-Wrap tool with a setting of 4. The bundle was placed into the thermal chamber, in a nearly vertical orientation; thus, the thermocouples are classified as "top" and "bottom" in the table, rather than "left" and "right."

3.0 TEST RESULTS

The effects of three parameters were measured: the temperature of the thermal vacuum chamber enclosure T_e, the core current I_{core} driving the 4 wires of special interest to this study, and the shell current I_{shell} driving the 24 enclosing wires.

Values were set and then held constant for each of these parameters until the steady state temperature was either established, or could be estimated. The values of the parameters, and the history of the four temperatures, are shown in Figure 1.

Inspection shows that these temperatures approach steady state values for each set of test parameters, with a time constant (the time to achieve ~ 70% of the steady state value) ranging from 6 minutes to 60 minutes. Estimates of the steady state values are given in Table 1.

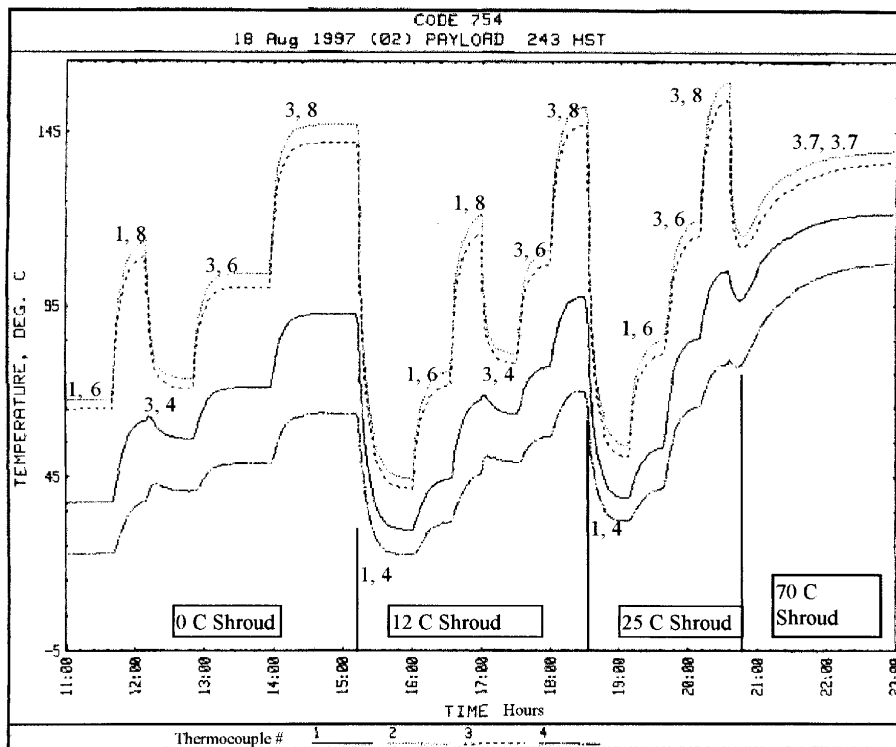


Figure 1. The Wire Bundle Temperature History.

The duration of each value of the enclosure temperature (here called the "shroud" temperature) is shown. The number-pairs in the figure are the currents carried by the shell and the core wires. The first number is the shell current: the current carried by the 24 wires in the test bundle. The second number is the core current: the current carried by the 4 wires in the bundle. For example, "3, 8" designates 3 A through each of the 24 shell wires, and 8 A through each of the 4 core wires.

Table 1:Steady-State Temperatures

Enclosure Temperature T_e (°C)	Shell Current I_{shell} (A)	Core Current I_{core} (A)	TC#1 shell, top (°C)	TC#2 core, top (°C)	TC#3 core, bot (°C)	TC#4 shell, bot (°C)
0	1	6	38	68	65	32
0	1	4	18	32	31	13
0	1	8	61	113	108	38
0	3	4	56	73	71	41
0	3	6	71	104	100	49
0	3	8	92	147	141	63
12	1	4	29	44	41	22
12	1	6	44	76	71	32
12	1	8	67	121	116	46
12	3	4	63	80	78	49
12	3	6	77	111	107	57
12	3	8	97	152	147	70
25	1	4	39	54	51	33
25	1	6	53	85	81	42
25	3	6	85	119	115	65
25	3	8	109	160	155	78
70	3.7	8	122	140	137	109

Thermocouples #1 and #4 measure the temperatures in apparently equivalent locations: we would expect these temperatures to be identical except for differences in the construction of the bundle, or differences in the effectiveness of the heat-sinking at the two ends. We would expect the same of thermocouples #2 and #3. In fact, the observed difference T(#1)-T(#4) ranges from 5°C to 29°C, and the difference T(#2)-T(#3) ranges from 1°C to 6°C. Since we are most interested in the temperature of the inner wires, and these are well determined for our present purposes, we can use the averages of thermocouples #1 and #4, and of #2 and #3:

$$T_{core} = (TC\#2 + TC\#3)/2 \qquad (1)$$
$$T_{shell} = (TC\#1 + TC\#4)/2 \qquad (2)$$

To the extent that the properties of the wires do not depend on temperature, and that the temperature differences between the outer shell wires and the enclosing shroud are relatively small (on an absolute temperature scale), then the rise in the core temperature above the enclosing shroud's temperature should be the same for each shroud temperature. Table 1 displays the steady state shell temperature minus the temperature of the enclosing shroud, T_{core} - T_e, for each combination of shell and core currents except the PPL current (3.7 A).

Table 2. The Core Temperature versus Enclosure Temperature, At Various Currents.

Enclosure Temperature T_e(°C)	Shell Current I_{shell}(A)	Core Current I_{core}(A)	Rise: T_{core} - T_e (°C)
0	1	4	31.5
12	1	4	30.5
25	1	4	27.5
0	1	6	66.5
12	1	6	61.5
25	1	6	58.0
0	1	8	110.5
12	1	8	106.5
25	1	8	---
0	3	4	72.0
12	3	4	67.0
25	3	4	---
0	3	6	102.0
12	3	6	97.0
25	3	6	92.0
0	3	8	144.0
12	3	8	137.5
25	3	8	132.5

Inspection shows that the values do not depend on the temperature of the enclosure T_e, to a first approximation. To a second approximation, there is a clear, small decrease with increasing enclosure tem-

perature. This is caused in part by the temperature dependence of the electrical resistance of the wire, and in part by end effects, which, while small, are not completely absent.

In steady state, the temperatures of the wires should rise above the temperature of the enclosure T_e by an amount that is proportional to the joule heats dissipated in the core and in the shell:

$$T_{core} = T_e + \kappa_{cc} \cdot R_{core}(T_{core}) \cdot I^2_{core} + \kappa_{cs} \cdot R_{shell}(T_{shell}) \cdot I^2_{shell} \quad (3)$$
$$T_{shell} = T_e + \kappa_{sc} \cdot R_{core}(T_{core}) \cdot I^2_{core} + \kappa_{ss} \cdot R_{shell}(T_{shell}) \cdot I^2_{shell} \quad (4)$$

where R(T) is the resistance of the wire at the temperature T and the set of κ are thermal resistance constants. (The details of the variation of the temperature of the wire along the length of the bundle is ignored here, but at least some of this variation can be absorbed into the values of the κ's.) These are implicit, and not explicit, equations for T_{core} and T_{shell} because these temperatures affect the resistances of the wires: R(T). Since the dependence of R on T is weak, we can solve the equations iteratively. We use approximate values for T_{core} and T_{shell} to evaluate the resistances on the right hand side, to get an improved set of values for T_{core} and T_{shell}. We can repeat this iteration until the results are satisfactorily stable.

The T_{core} values are uncertain to several degrees: this is the order of the difference between TC#2 and TC#3. We found that the variation of the T_{core} values is described to this precision by a substantially simplified model: (1)

We can hope that both temperature-dependent coefficients have essentially the same dependence on temperature up to a scalar multiple, so that their ratio has only a weak (at most) dependence on temperature: $\gamma \sim \beta(T) / \alpha(T)$. Also, we can hope that the temperature of the core and shell wires are nearly enough proportional to the enclosure temperature, that, we can replace T_{core} and T_{shell} with T_e with at most a re-scaling of the coefficients $\alpha(T)$ and $\beta(T)$. In fact, we find that the temperatures of the core wires are fit with an average error of ±1.3°C by the expression

$$T_{core} = T_e + \alpha(T_e) \cdot [I^2_{core} + \gamma \cdot I^2_{shell}] \quad (5)$$
$$\alpha(T_e) = [\, 1.644 - T_e / (150.8°C) \,] \cdot (°C/A^2) \quad (6)$$
$$\gamma = 2.873 \quad (7)$$

which has the expected theoretical form. This equation, with just three parameters, usefully summarizes 16 test results. Table 3 compares the observed average core temperature T_{core} with the result of Equations 5, 6, and 7.

Table 3. The Observed Core Temperature versus the Computed Core Temperature.

Enclosure Temperature T_e (°C)	Shell Current I_{shell} (A)	Core Current I_{core} (A)	Observed T_{core} (°C)	Computed T_{core} (°C)	Diff: obs-comp (°C)
0	1	4	31.5	31.0	0.5
12	1	4	42.5	41.5	1.0
25	1	4	52.5	52.9	-0.4
0	1	6	66.5	63.9	2.6
12	1	6	73.5	72.8	0.7
25	1	6	83.0	82.5	0.5
0	1	8	110.5	109.9	0.6
12	1	8	118.5	116.6	1.9
25	1	8	---	123.9	---
0	3	4	72.0	68.8	3.2
12	3	4	79.0	77.5	1.5
25	3	4	---	86.9	---
0	3	6	102.0	101.7	0.3
12	3	6	109.0	108.8	0.2
25	3	6	117.0	116.4	0.6
0	3	8	144.0	147.7	3.7
12	3	8	149.5	152.6	-3.1
25	3	8	157.5	157.8	-0.3
70	3.7	3.7	138.5	132.6	5.6

The coefficient of the shell current I_{shell} is about three times larger than the coefficient of the core current I_{core}. There are 24 shell wires and 4 core wires: this is a factor of six times greater. However, the shell wires are more tightly coupled to each other than to the typically more distant shell wires, and this reduces the effect of the shell wires on the core wires. Thus, the observed ratio of the current-coefficients is plausible.

Inspection of Table 1 shows that the temperature of the core wires is far below their rated maximum value for the most stressful expected operating conditions of the HST: $T_{core} < 120°C$ when $T_e = 25°C$, $I_{core} = 6.0$ A, and $I_{shell} = 3.0$ A. The model shows that all the test data form a consistent whole, and so this particular result is not a fluke. And the model will permit computation of accurate values of the core temperature, should there be further modifications in the requirements of the PDU of the HST.

The thermal vacuum test included the special case $I_{core} = I_{shell} = 3.7$ A. This was not included in data set used to obtain the fitted expression. Using the expression, we compute $T_{core} = T_e + 63°C$, while the experimental value is $T_e + 69°C$. The computational value is 6°C smaller than the observed value. Using the model defined by Equations 5, 6, and 7 we compute that the core temperature reaches the specified maximum value of 200°C when $I_{core} = I_{shell} = 5.3$ A. The PPL-specified maximum is 3.7 A, which is 70% of 5.3 A. Thus, the PPL is derating the current to 70% of the value that produces the maximum operating temperature for these wires, under the conditions of the present thermal vacuum test and bundle. That is, these test results show that the recommendation of the PPL keeps all wires under their rated maximum temperature, as it should.

The values of the coefficients of the fitting equation must depend on the emissivity of the insulation, and so must not be used to predict the behavior of other sorts of wire. It might prove possible to usefully estimate this effect, so that an approach like this one could be used to compliment guidebook recommendations. The form of the fitting equation should be general: the temperature rise of any wire above that of the shroud must be a linear combination of the squares of the currents through the other wires with weakly temperature-dependent coefficients.

4.0 CONCLUSION

There is a high level of confidence that the wires within the PDU of the HST will not approach their maximum operating temperature. This is true even when as much as 8 A is passing through the subject wires, when no more than 3 A is passing through the remaining wires and the PDU is no hotter thn 25°C.

Under the conditions named in the PPL, some wires reached a maximum temperature of 140°C, which is safe. The PPL is using an implicit derating to 70% of the current that would take core wires to the maximum operating temperature of 200°C.

A variety of test data were brought under the control of a single equation with three parameters. The form of this equation is general, and should apply to other wire bundles as well. Experiments are presently required to determine the parameters.

Jet Propulsion Laboratory Parts Analyses

Joan Westgate
NASA/JPL
818-354-9529
joan.c.westgate@jpl.nasa.gov

Failure analyses (FA), destructive physical analyses DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

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FAILURE ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6868	Linear Technology	9142A	Operational Amplifier	RH108AW
6976	Rosemont Aerospace Inc.	None	Temperature Transducer	ST11784-0002
6877	Harris Semiconductor	9250A	High-Speed CMOS/SOS Octal D Flip-Flop With Master Reset	54HCS273
6977	Solid State Devices, Inc.	9026	NPN Power Transistor	8838
6984	Hewlett Packard Advanced Microdevices	Various	CMOS Optocoupler Differential Line Driver	HCPL-7101 AM26LS31
7066	Compensated Devices, Inc.	Unknown	Surface Mount Schottky Barrier Diode	JANTXV1N5711UR-1
7070	PPC Products Corp.	9433	NPN, Silicon Power Transistor	2N5339
7079	Micropac	9649	Opto-Isolator	66099-105
DESTRUCTIVE PHYSICAL ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6911	Merrimac	None	RF Directional Coupler	CRM-20-500
6940	ADI	9613	OP Amp	OP270
6941	Harris Semiconductor	9622	ACTS	74
6942	Harris Semiconductor	9644	ACTS	244
6943	Harris Semiconductor	9549	HCS	04
6944	NSC	9630	AC00	N/A
6979	United Technologies	9731	ACTS244	5962H9657101VCX
6980	United Technologies	9726	UTC69151	R9466304QCY
6981	UTMC	9647	Programmable Array Logic	5962R9475401QXC
6982	Harris Semiconductor	9716	64K PROM, HS9-6664RH-Q	5962F956201VYC
6986	International Rectifier	9727	HEXFET	IRHE9130
6987	International Rectifier	9729	HEXFET	IRHE7230
6991	Siliconix	9718	Quad Transistor	SD50001-2
6995	Linear Technology	9615A	Rad Hard, Dual Precision OP-AMP	RH1013MJ8
7001	Harris Semiconductor	9642	Quad Receiver 26C32	5962-F9568901VXC
7002	Retcon	9645	Photodiode Array	RL0128KAU
7005	BEI	N/A	IR Light Emitting Diode	611-0024-101
7007	Interpoint	9646	Unregulated ±15V DC-DC Converter Hybrid	DCH0515D/ES
7009	Lambda Advanced Analog	9637	DC-DC Converter	ATR2812D/CH
7011	CTS	9730	PC Preamp Hybrid	21053819-101

DESTRUCTIVE PHYSICAL ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
7012	CTS	9730	Relay Driver Hybrid	21053819-101
7014	International Manufacturing Service	N/A	50K Ohm Resistor	IMS 007-1-5002J
7029	KD	9721	Capacitor	87106-075
7030	KEM	9534KA	Tantalum Capacitor	95158-11KH
7031	KEM	9709	Tantalum Capacitor	95158-19KH
7032	KEM	9709	Tantalum Capacitor	95158-23KH
7033	Unknown	9703	Tantalum Capacitor	93026-47KS
7034	KEM	9644	Capacitor	M39014/01-1305
7036	KD	9740	Capacitor	SM20B103K501M
7037	VIT	9620A	Capacitor	VJ0805Y332KFCAB
7038	Unknown	9626	Capacitor	M39014/01-1305
7039	VIT	9726A	Capacitor	VJ0805Y561KFCAB
7040	VIT	9741	Capacitor	5VJ0805A681JXBMT
7054	Comm. Instruments, Inc.	9642	Relay	M39016/9-060M
7060	Watkins-Johnson	9740	Hybrid RF Amplifier Module	CRA89-1S
7061	JCA Technology	9746	Hybrid RF Amplifier Module	JCA56-4116W
7062	Zeta	None	X15 RF Multiplier Hybrid Module	071657-001
7084	BKC Semiconductors	Unknown	Surface Mount Schottky Diode	LL101A
8008	National Semiconductor	A8050	Octal Buffer, Inverted output	54ACT240
8009	National Semiconductor	9717	Octal Buffer Line Driver	54ACT244
8010	National Semiconductor	9737	Octal Bus Transceiver	54FCT245
8011	Harris	9634	RS422 Receiver	HS0-26C32RH-Q
8012	Texas Instruments	9809	Octal Buffer	54AC240
8021	Teledyne Relay	None	DPDT Latching Relay	422K12PL
8035	National Semiconductor	9718L	Octal Buffer/Line Driver	54ACG244FMQB
8036	National Semiconductor	9728B	Octal Buffer/Line Driver	54ACT244FMQB
8037	National Semiconductor	9731A	Octal Buffer/Line Driver	54ACT244FMQB
8038	Apex Micro Tech	9723	Hybrid DC/DC Converter, 3 Volt, 5 Watt, Single Output	DHC2803S
8040	Datel, Inc.	9827	Encapsulated Dual Output, 3 Watt, ±5 Volt, DC/DC Converter	BWR-5/250-D12
8041	Pico Electronics, Inc.	9745	Encapsulated DC/DC Converter	LRF12D
8042	Analog Devices	9822	Hybrid 100W DC/DC Converter	ADDC02812DATV/QMLH(5962-9684101HXC)
8043	Analog Devices	9820	Hybrid DC/DC Converter	ADDC02812DAKV
8047	Datel, Inc.	9830	Encapsulated Dual Output, ±15 Volt, DC/DC Converter	BWR-15/670-D12A
8049	Analog Devices	AR9821	Dual, 16MHz, Rail-to-Rail FET Input Amplifier	AD823
8051	Teledyne	9832	Up to 23 Watts, Triple Output DC/DC Converter	2297425-8 J
8056	Maxim	None	Regulated 125 mA Output, Charge Pump DC/DC Inverter	MAX 1673

PART CONSTRUCTION ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6852	Analog Devices, Inc.	9627	3V, CMOS, 500 µA Signal Conditioning ADC	AD7714
6853	Burr-Brown Corporation	9621	24-Bit Delta-Sigma A/D Converter	ADS1210
8039	Hewlett Packard	N/A	Custom Auto Digital Correlator Specrometer	128

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

EV JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
88555	EV	IDT	9832	49C465	49C465	P	10/14/98
CA JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
88579	CA	DALE	9820	M83401	M8340109K1002JC	P	10/06/98
88574	CA	NATIONAL SEMICONDUCTOR	9605	JK137BYA	JM38510/11804BYA	P	10/20/98
88573	CA	NATIONAL SEMICONDUCTOR	9801	54ACTQ244DMQB	5962-9218601MRA	P	10/09/98
88572	CA	NATIONAL SEMICONDUCTOR	9821, 9823	54ABT245J-QML	5962-9214801QRA	F	10/27/98
88570	CA	ASI	9827	MICROCIRCUIT	AS58C1001SF-15	P	10/26/98
88569	CA	MICROPAC	9803	OPTO-COUPLER	JANTXV4N49	P	10/20/98
88561	CA	MICROSEMI CORPORATION	9633	1N4153-1	JANTXV1N4153-1	P	09/30/98
88558	CA	NATIONAL SEMICONDUCTOR	9722	54ACTQ245DMQB	5962-9218701MRA	P	10/08/98
88551	CA	NATIONAL SEMICONDUCTOR	9803	JL147BCA	JM38510/11906BCA	P	09/22/98
88547	CA	MICROSEMI CORPORATION	8608	1N4961	JANTXV1N4961	P	09/08/98
88546	CA	HEWLETT PACKARD	9825	HSSR-7111#200	5962-9314001HPA	P	09/11/98
88541	CA	ANALOG DEVICES	9814	OP400AY/883	5962-8777101MCA	P	09/15/98
88522	CA	INTERNATIONAL RECTIFIER	9818	2N7334	JANTXV2N7334	P	10/01/98
88517	CA	LINEAR TECHNOLOGY CORP.	9742	LT1021CMH-5/883B	5962-8876202GA	P	09/08/98
88517	CA	LINEAR TECHNOLOGY CORP.	9742	LT1021CMH-5/883B	5962-8876202GA	P	09/08/98
88514	CA	LINEAR TECHNOLOGY CORP.	9808	LT1010MH/883	5962-8856201XA	P	08/26/98
88513	CA	LINEAR TECHNOLOGY CORP.	9705	LT1009MH/883	5962-8961001XA	P	08/10/98
88512	CA	MICROSEMI CORPORATION	9749A	1N5940A	JANTXV1N5640A	P	08/19/98
88511	CA	SEMICON COMPONENTS	9803	1N5926A	JANTXV1N5629A	P	08/18/98
88510	CA	COMPENSATED DEVICES, INC.	9811	1N4106-1	JANTXV1N4106-1	P	08/10/98
88508	CA	MICROSEMI CORPORATION	9808	1N758A-1	JANTXV1N758A-1	P	08/06/98
88507	CA	BKC SEMICONDUCTORS	9719	1N3595-1	JANTXV1N3595-1	P	08/07/98
CA JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
88503	CA	HARRIS SEMICONDUCTOR	9745	MICROCIRCUIT	M38510/19001BXA	P	08/13/98
88502	CA	BKC SEMICONDUCTORS	9808	1N5806	JANS1N5806	P	08/11/98
88258	CA	NATIONAL SEMICONDUCTOR	9802	54ACTQ08DMQB	5962-8954702CA	P	08/28/98

Job Number		Manufacturer	Date Code	Part Type	Part Number	Result	Date
FA JOBS							
80936	FA	NATIONAL SEMICONDUCTOR	9616	LMC6062	LMC6062 (CHIP)	F	08/07/98
EC JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
89574	EC	PENTADYNE	9831	P W BOARD	346021-1	P	09/03/98
89573	EC	COLONIAL CIRCUITS	9823, 9834	P W BOARD	2022018-1	F	08/27/98
89572	EC	ADVANCED QUICK	2898	P W BOARD	IM-OR-5006	P	09/02/98
89571	EC	CIMULEC	9824	P W BOARD	RBUS06	F	09/03/98
89570	EC	SPEEDY CIRCUITS	9833	P W BOARD	9021102-01 REV B	P	08/25/98
89569	EC	ADVANCED QUICK	2598	P W BOARD	IM-EP-5131	P	09/01/98
89568	EC	ADVANCED QUICK	2498	P W BOARD	IM-EP-5231	P	09/01/98
89567	EC	ADVANCED QUICK	2498	P W BOARD	IM-EP-5051	P	09/01/98
89566	EC	ELECTRO PLATE	980730	P W BOARD	324005-1 REV A	P	08/28/98
89565	EC	PROTO CIRCUITS	3398	P W BOARD	645675/A	F	08/28/98
89554	EC	IMI INC.	297	P W BOARD	11448-001 REV B	P	08/18/98
89553	EC	TYCO ENGINEERED	3198	P W BOARD	185342-1	P	08/15/98
89552	EC	TYCO ENGINEERED	3198	P W BOARD	185342-1	P	08/15/98
89551	EC	SIGMA CIRCUITS INC	2798	P W BOARD	8137-P5D REV D	P	08/15/98
89550	EC	UNKNOWN	9822	P W BOARD	DOR4	F	08/20/98
89549	EC	UNKNOWN	472	P W BOARD	CHAMP PCDU	F	08/19/98
89548	EC	ELECTRO PLATE	970706	P W BOARD	346011-1	P	08/15/98
89547	EC	CIRTECH INC	3098	P W BOARD	D448721-2	P	08/06/98
89546	EC	CIRTECH INC	3098	P W BOARD	D448731-2	P	08/06/98
89545	EC	TYCO ENGINEERED	3098	P W BOARD	184956-1 REV D	F	08/06/98
89544	EC	IMI INC.	2498	P W BOARD	F44909	F	08/13/98
89543	EC	IMI INC.	2498	P W BOARD	F44922	F	08/13/98
89542	EC	IMI INC.	2498	P W BOARD	F44899	P	08/13/98
89541	EC	IMI INC.	2498	P W BOARD	F44898	F	08/13/98
89540	EC	ARGOS SPACE	690/02	P W BOARD	65331-001	P	08/13/98
89539	EC	TYCO ENGINEERED	2298	P W BOARD	34111458-001 REV A	P	08/06/98
89539	EC	TYCO ENGINEERED	2298	P W BOARD	34111458-001 REV A	P	08/06/98
89538	EC	TYCO ENGINEERED	2298	P W BOARD	34111456-001 REV A	P	08/04/98
89536	EC	TYCO ENGINEERED	2198	P W BOARD	34113868-001	P	08/05/98
89535	EC	TYCO ENGINEERED	2298	P W BOARD	34113859-001	F	08/05/98
89534	EC	SIGMA INC	3098	P W BOARD	CHAMP-FAB LGR	P	08/03/98
89519	EC	CIMULEC	9820	P W BOARD	RBUS06SC/12	P	08/24/98

EC JOBS							
Job Number		Manufacturer	Date Code	Part Type	Part Number	Result	Date
88579	CA	DALE	9820	M83401	M8340109K1002JC	P	10/06/98
88574	CA	NATIONAL SEMICONDUCTOR	9605	JK137BYA	JM38510/11804BYA	P	10/20/98
88573	CA	NATIONAL SEMICONDUCTOR	9801	54ACTQ244DMQB	5962-9218601MRA	P	10/09/98
88572	CA	NATIONAL SEMICONDUCTOR	9821, 9823	54ABT245J-QML	5962-9214801QRA	F	10/27/98
88570	CA	ASI	9827	MICROCIRCUIT	AS58C1001SF-15	P	10/26/98
88569	CA	MICROPAC	9803	OPTO-COUPLER	JANTXV4N49	P	10/20/98
88561	CA	MICROSEMI CORPORATION	9633	1N4153-1	JANTXV1N4153-1	P	09/30/98
88558	CA	NATIONAL SEMICONDUCTOR	9722	54ACTQ245DMQB	5962-9218701MRA	P	10/08/98
88551	CA	NATIONAL SEMICONDUCTOR	9803	JL147BCA	JM38510/11906BCA	P	09/22/98
88547	CA	MICROSEMI CORPORATION	8608	1N4961	JANTXV1N4961	P	09/08/98
88546	CA	HEWLETT PACKARD	9825	HSSR-7111#200	5962-9314001HPA	P	09/11/98
88541	CA	ANALOG DEVICES	9814	OP400AY/883	5962-8777101MCA	P	09/15/98
88522	CA	INTERNATIONAL RECTIFIER	9818	2N7334	JANTXV2N7334	P	10/01/98
88517	CA	LINEAR TECHNOLOGY CORP.	9742	LT1021CMH-5/883B	5962-8876202GA	P	09/08/98
88517	CA	LINEAR TECHNOLOGY CORP.	9742	LT1021CMH-5/883B	5962-8876202GA	P	09/08/98
88514	CA	LINEAR TECHNOLOGY CORP.	9808	LT1010MH/883	5962-8856201XA	P	08/26/98
88513	CA	LINEAR TECHNOLOGY CORP.	9705	LT1009MH/883	5962-8961001XA	P	08/10/98
88512	CA	MICROSEMI CORPORATION	9749A	1N5940A	JANTXV1N5640A	P	08/19/98
88511	CA	SEMICON COMPONENTS	9803	1N5926A	JANTXV1N5629A	P	08/18/98
88510	CA	COMPENSATED DEVICES, INC.	9811	1N4106-1	JANTXV1N4106-1	P	08/10/98
88508	CA	MICROSEMI CORPORATION	9808	1N758A-1	JANTXV1N758A-1	P	08/06/98
88507	CA	BKC SEMICONDUCTORS	9719	1N3595-1	JANTXV1N3595-1	P	08/07/98
88503	CA	HARRIS SEMICONDUCTOR	9745	MICROCIRCUIT	M38510/19001BXA	P	08/13/98
88502	CA	BKC SEMICONDUCTORS	9808	1N5806	JANS1N5806	P	08/11/98
88258	CA	NATIONAL SEMICONDUCTOR	9802	54ACTQ08DMQB	5962-8954702CA	P	08/28/98