Upgrade of the Level-0 trigger system for BNL-E949

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***Abstract*— A new programmable trigger board and digital Mean-timer modules using CPLD have been introduced to the trigger system of the BNL-E949 experiment in order to reduce the online dead time. This article describes details of the upgrade.**

***Index Terms*— trigger, meantimer, CPLD, FPGA**

I. Introduction

THE BNL-E949 experiment[1], which is a successor to E787[2], aims to measure the branching ratio of the rare kaon decay $K^+ \to \pi^+\nu\bar{\nu}$ whose branching ratio is predicted to be 10^{-10}[3]. Several improvements, one of which is the upgrade of the Level-0 trigger system described here, were made to E787 in order for E949 to reach a sensitivity of 10^{-11} and observe 10 Standard Model events.

E949 observes kaons decaying at rest. Kaons are produced by 21.5GeV protons from the Alternating Gradient Synchrotron(AGS) incident on a 6cm Platinum production target. Particles produced at zero degree are transported to the E949 detector via the Low Energy Separated Beamline 3(LESB3)[4].

The E949 detector is shown in Fig. 1. The whole detector is situated in a 1 Tesla magnetic field parallel to the beam axis. An incident kaon comes to rest and decays in the target which is composed of a bundle of scintillating fibers. The momentum of charged decay products is measured with a cylindrical drift chamber[5] surrounding the target. The particles come to rest in the Range Stack(RS) consisting of 19 layers of plastic scintillator segmented into 24 azimuthal sectors. The pulse shapes of both ends of each RS counter are recorded by 500-MHz Transient Digitizers(TDs)[6] in order to observe $\pi^+ \to \mu^+ \to e^+$ decay chain. Photon detectors cover the full 4π solid angle: the central barrel region is covered by the Barrel Veto(BV) and Barrel Veto Liner(BVL), which are lead-scintillator sampling calorimeter, and the region along the beam axis is covered by endcaps of undoped-CsI(EC)[7]. The collar, microcollor, upstream photon veto, active degrader and downstream photon veto fill the remaining gaps near the beam axis.

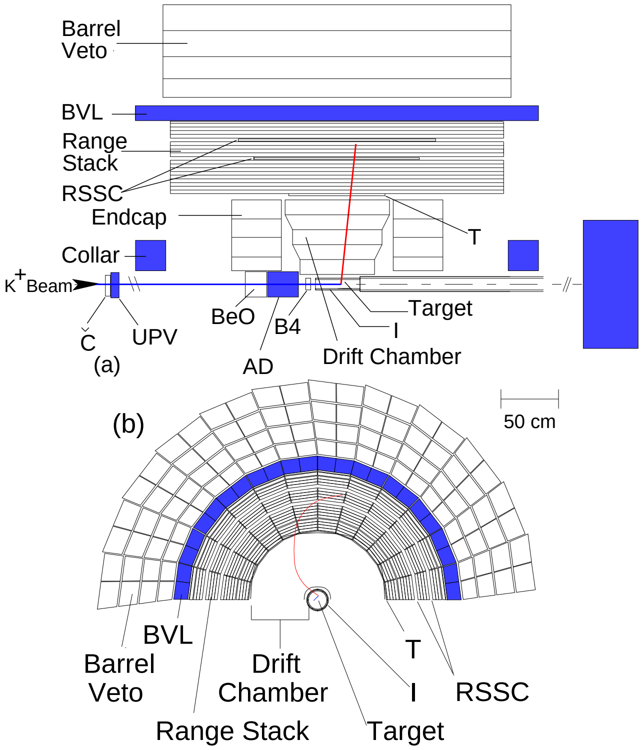

Fig. 1. Schematic sideview(top) and endview(bottom) of the upper half of E949 detector. Shaded part is the newly installed detector for E949.

A total of 3.5×10^6 kaons enter the E949 target in each 2.2 sec spill every 5.4 sec. In order to meet the data transfer speed(10MB/sec), the number of triggers per spill must be reduced. E949 trigger system consists of fast Level-0(L0) trigger, Level 1.1(L1.1) and Level 1.2(L1.2) triggers. They are entirely operated on ECL signals. A block diagram of the E949 L0 trigger system is shown in Fig. 2. The L0 trigger

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system is composed of several FASTBUS modules. The RZ board(RZ) and Trigger Transmitter(TT) put 65 L0 trigger bits to the Trigger Bus(T-Bus). The L0 trigger board makes a decision using the T-Bus bits. The L1.1 and L1.2 triggers involve processing of TD and ADC data with a longer decision time but at the lower rate of events that pass the L0 trigger.

The trigger condition for $K^+ \rightarrow \pi^+\nu\bar{\nu}$ is defined as follows:

$$\begin{aligned} \pi^+\nu\bar{\nu} \quad \equiv \quad & K_B \cdot DC \cdot (T \bullet 2) \cdot \\ & (6_{ct} + 7_{ct}) \cdot \overline{19_{ct}} \cdot RR \cdot \overline{L0\_zfrf} \cdot \\ & \overline{(BV + BVL + EC)} \cdot HEX \cdot \\ & L1.1 \cdot L1.2 \end{aligned}$$

where K_B requires that a K^+ in the beam enters the target, and DC is the online Delayed Coincidence bit which requires that the timing of the outgoing pion is at least 1.5nsec later than timing of the incoming kaon. The $T \bullet 2$ signal is a coincidence of the first and second layer of the RS in the same sector, which ensures the pion enters the RS. The trigger bit $6_{ct} + 7_{ct}$ requires the pion reaches the 6th or 7th layer of the RS and suppresses the $K^+ \rightarrow \pi^+\pi^+\pi^-$ or $K^+ \rightarrow \pi^+\pi^0\pi^0$ backgrounds. The $\overline{19_{ct}}$ signal requires the pion does not reach the 19th layer and suppresses $K^+ \rightarrow \mu^+\nu$(called $K_{\mu 2}$) background. The "*ct*" designates the RS sectors that are associated with a $T \bullet 2$($T \bullet 2$ sector plus the next two clockwise sectors; this is the direction that a positive particle moves in the magnetic field). The RR bit is a refined range of the charged track calculated from the online information which rejects events with long range such as μ^+ from the $K_{\mu 2}$ decay. $BV{+}BVL$, EC and HEX are online photon bits from the barrel region, Endcap region and RS, respectively, which remove events with photons such as $K^+ \rightarrow \pi^+\pi^0$(called $K_{\pi 2}$) or $K^+ \rightarrow \mu^+\nu\gamma$. $L0\_zfrf$ is a online fiducial cut for z-position of the charged track.

In addition to the $\pi^+\nu\bar{\nu}$ trigger, there are monitor triggers for the purpose of calibration and normalization, and triggers for other physics modes. All triggers can be prescaled, but the $\pi^+\nu\bar{\nu}$ trigger and sometimes other physics triggers are usually not prescaled. All trigger decisions, defined as combinational logic of L0 trigger bits, are performed by L0 trigger board. Note that all L0 trigger bits on T-Bus are latched by $T \bullet 2$ and every $T \bullet 2$ introduces a dead time of 40nsec. With a L0 pass and a subsequent L1.1 and L1.2 pass the start signal for readout of the data is issued.

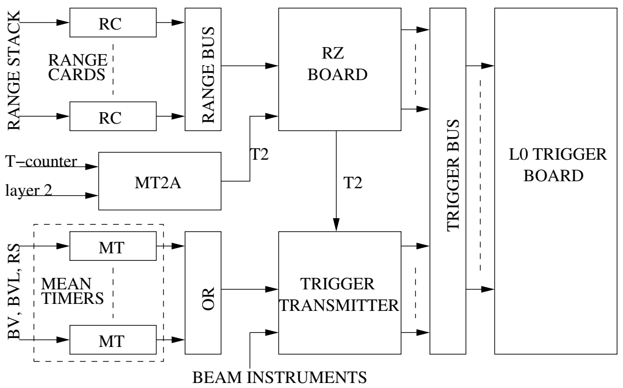

Fig. 2. A block diagram of the E949 L0 trigger system. All trigger decisions, defined as combinational logic of L0 trigger bits on the Trigger Bus, are performed by L0 trigger board. Note that the dashed line region at the bottom-left corner of the figure is newly installed Mean-timers described later.

The E949 experiment aims to accumulate more statistics with higher beam intensity than E787. The trigger system must work more flexibly and with less dead time. In E949, programmable L0 trigger board was installed instead of the E787 trigger board for the flexibility of the trigger. Digital Mean-timer modules were installed to reduce online dead time.

II. Level-0 Trigger Board

The L0 trigger board for E787 used wire-wrap ECL logic in a FASTBUS board; one had to re-wire the board to modify the trigger condition. In E949, trigger modifications were expected because of the detector upgrade, and we therefore developed a new programmable L0 trigger board. The board has Complex Programmable Logic Device (CPLD) chips (a product of ALTERA cooperation). Any trigger logic can be programmed using the Hardware Description Language (HDL). The CPLD has In System Program(ISP) capability. The trigger conditions can be modified through JTAG link without extracting the board from the crate. The specification of the new L0 trigger board is summarized in TableI; a picture of the board is shown in Fig. 3. For the trigger logic, two high-speed PLD chips(EPM7032-B-4) are used. In addition to the high-speed PLD, the board has a large-scale PLD chip (EPF10K100E-1) for various applications which will be described below.

TABLE I
Specification of the L0 trigger board

High-speed PLD	EPM7032B-4
Large-scale PLD	EPF10K100E-1
Board Size	FASTBUS
Input	65 ECL at back 16 ECL at front
Output	24 ECL(duplicated) 3 Or-ed(output) 16 ECL at front

The $T \bullet 2$ signal initiates the trigger process and creates a dead time of 40nsec. If a L0 condition is satisfied, the dead time must be extended for further trigger processing. This scheme is illustrated in Fig. 4. The OR-ed L0 decision signal is fed to the RZ board, which extends the $T \bullet 2$ signal via a one-shot to 100nsec. In order to realize this scheme, the propagation time of the new board is required to be less than 19nsec. We chose the SY100ELT24(25) for the TTL/ECL(ECL/TTL) converter chips. The high-speed CPLD and ECL/TTL converter chips meet the requirement (see TableII).

A. Prescaler

The number of L0 decision for monitor triggers should be prescaled at the L0 trigger board, because any L0 decision signal introduces 100nsec dead time as described in the above

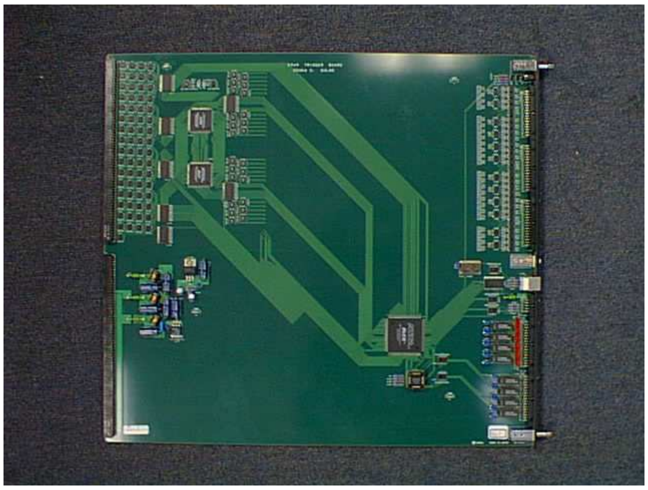

Fig. 3. A picture of the new L0 trigger board. Two high-speed PLD chips for trigger logic are located at top-left corner. A large-scale PLD for various applications is located at bottom-right corner.

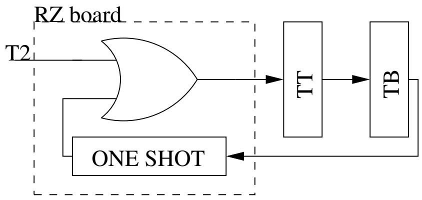

Fig. 4. A schematic view of extending the L0 dead time. Any L0 trigger decisions extend the $T \bullet 2$ width from 40nsec to 100nsec.

scheme. We therefore introduced an on-chip prescaler for monitor triggers in order to reduce the trigger dead time. A block diagram of the prescaler on the trigger board is shown in Fig. 5. The trigger decision signal of a monitor trigger is fed to the large-scale PLD, and the large-scale PLD counts the number of events. After reaching the number of prescaling factor, the large-scale PLD issues the enable signal to the high-speed PLD for the next event. The prescaling factor can be selected thorough ECL lines(at front panel) from a computer. Introducing the prescaler on the minimum-bias monitor trigger(requiring only $K_B \cdot DC \cdot T \bullet 2$), the L0 dead time was reduced from 4.0% to 1.7%.

B. Diagnostic system

In upgrading the trigger system, debugging time is desired to be as short as possible. We therefore introduced an on-chip diagnostic system in the large-scale PLD. A block diagram of the diagnostic system is shown in Fig. 6. The large-scale PLD counts the number of events(scaler) and monitors the

TABLE II

PROPAGATION TIME OF THE L0 TRIGGER BOARD

ECL/TTL + TTL/ECL conversion	2 nsec
EPM7032B-4	12 nsec
propagation on board	2 nsec
TOTAL	16 nsec

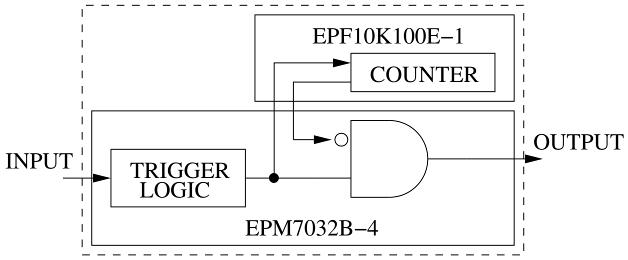

Fig. 5. A schematic view of the on-chip prescaler. After reaching the number of prescaling factor, the large-scale PLD issues the enable signal to the high-speed PLD for the next event.

hit pattern of input signals from the T-Bus(hit pattern finder). The on-chip scaler counts a trigger decision signal from both new and old trigger boards, and compares the number of events. No disagreement was observed at 10^{-6} level during the engineering run of E949. A hit pattern finder allowed for easy debugging when new triggers were introduced. The information is read through ECL lines(at front panel) from a computer.

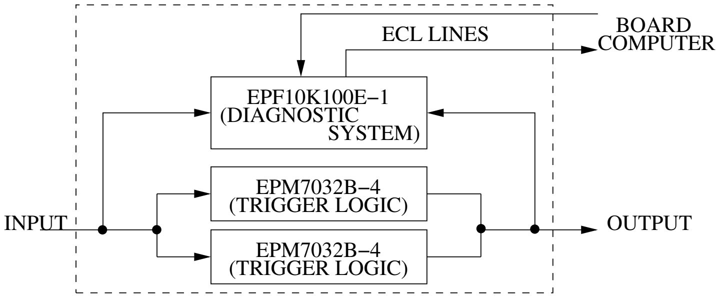

Fig. 6. A block diagram of the diagnostic system. On-chip scaler and hit pattern finder were introduced to the large-scale PLD. The information is read through ECL lines from a computer.

III. MEAN-TIMER

Digital Mean-timer modules were installed for the online photon veto of the E949 experiment. In the E787 experiment, analog sum signals of the single end of the RS and BV [1] counters were used for the photon veto signal, and the veto time width was large(typical 20nsec) to account for the timing variations due to the z-position of the photons. By using a Mean-timer module, the veto time width can be narrowed and accidental veto rate is therefore reduced. The signals of both ends of the RS, BV and BVL counters are mean-timed in the photon veto Mean-timer. The mean-timed signals are fed to the Trigger Transmitter and used as L0 photon veto signal.

A gate array has been used as a digital Mean-timer up to now. CPLDs are remarkably high-speed today and we therefore have developed a digital Mean-timer using CPLD. Fig. 7 shows the logic circuit of the digital Mean-timer described in HDL. The triangles in the figure represent a logic element which is the minimum component of the CPLD

[1]Note that the BVL is new to E949 and was not in the E787 detector.

device(called 'delay-cell'). The propagation time of the delay-cell is 1nsec[8]. The serial line of the delay-cells is called 'delay-line', and two delay-lines are used in the digital Mean-timer. The signal of both ends of the scintillator are fed to the delay-line. Fig. 8 shows the time progress of the signals in the scintillator and the delay-line. The left-right coincidence signals occurs at a fixed time regardless of the time difference between the left and right signals.

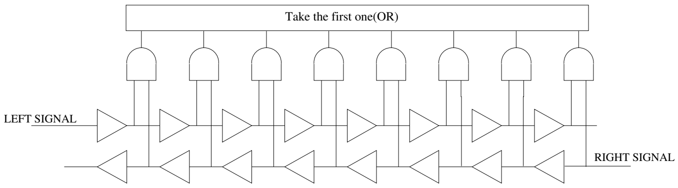

Fig. 7. Logic circuit of the digital Mean-timer described in HDL. The triangles represent a logic element which is the minimum component of the CPLD(called 'delay-cell').

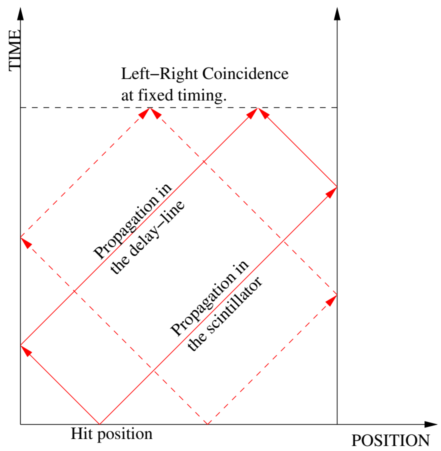

Fig. 8. Time progress of the signals in the scintillator and delay-line. Left-Right coincidence for any hit positions in the scintillator(e.g. solid line and dashed line) occurs at the fixed timing.

Due to space limitation in the electronics hut, the Mean-timer combined the functions of a discriminator and CPLD. Six Mean-timer blocks were implemented in a large scale PLD. A picture and block diagram of this module is shown in Fig. 9 and Fig. 10, respectively. The specification is shown in TableIII.

TABLE III
SPECIFICATION OF THE MEAN-TIMER MODULE

PLD	EPF10K50E-1
Board Size	CAMAC
Input	12 analog
Output	16 ECL at front

A. *Performance at test bench*

The performance of the Mean-timer was tested at a test bench. Two random signals from gate generators are input

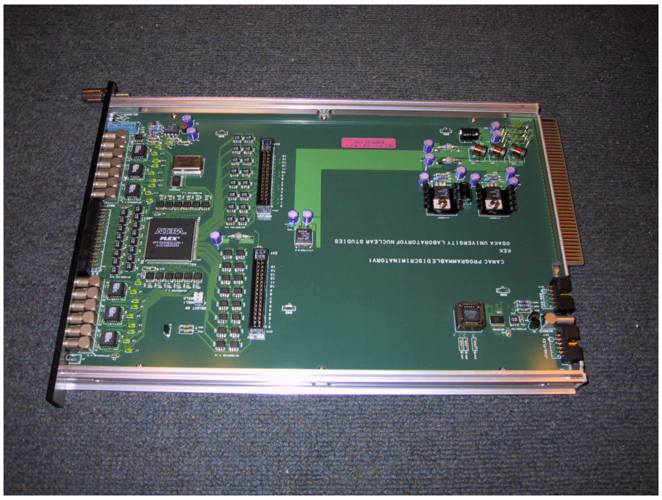

Fig. 9. A picture of the Mean-timer module. A large-scale PLD is located at Middle-left of the module.

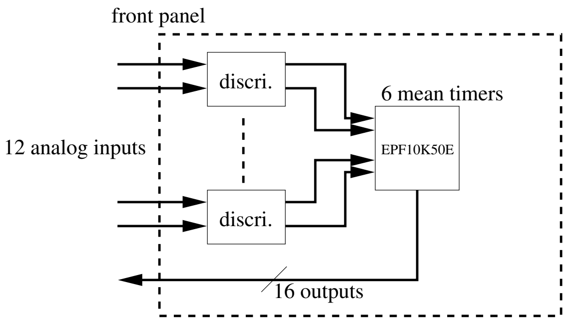

Fig. 10. A block diagram of the Mean-timer module. This module combined the function of a discriminator and CPLD.

to the Mean-timer module. The two input signals and the mean-timed signal are fed into a CAMAC TDC with 25psec resolution(see Fig. 11). The left plot of the Fig. 12 is the time distribution of the two inputs signals. Since the 12 delay-cells in a delay-line are used for this test, the range is 12nsec. The right plot of the Fig. 12 is the time distribution of the difference of the online and offline mean-timed signals. The sigma is 0.26nsec.

B. *Performance with beam*

The digital Mean-timers were installed to the E949 trigger system and the performance was checked. Fig. 13 shows time distribution of the online photon veto bit. Top-left(right) figure shows the distribution of BV(BVL) analog sum and bottom-left(right) figure shows the distribution of BV(BVL) Mean-timer. The hits at around t=0 due to electromagnetic shower in the detector were removed efficiently with half the acceptance loss of the previous system.

IV. CONCLUSION

We have developed the L0 trigger board and digital Mean-timer module for the BNL-E949 experiment. The L0 trigger board allowed us rapid and simple programming of the

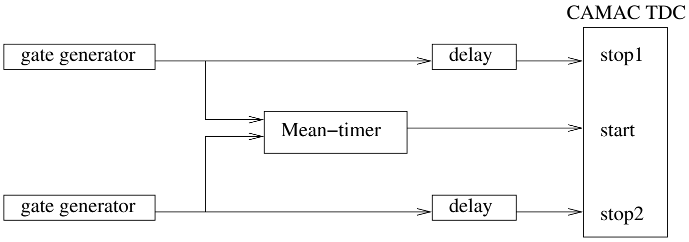

Fig. 11. A block diagram of setup for the Mean-timer performance test.

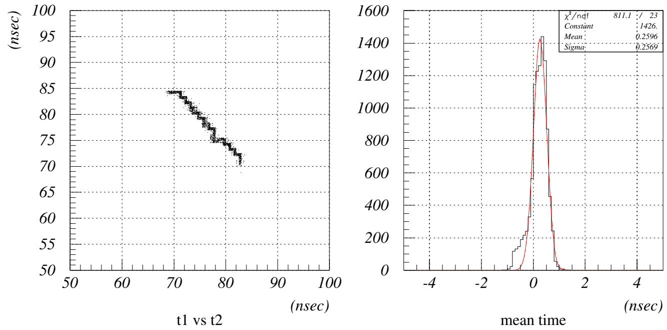

Fig. 12. Scatter plot of the two input signals(left) and difference of the online and offline mean timed signal(right). The sigma in the right plot is 0.26nsec. A dip at around t=78nsec in the left plot is due to the scheme of the CPLD.

triggers. In addition to the flexibility, the online dead time was reduced by an on-chip prescaler. A powerful diagnostic capability provided quick and easy debugging of new trigger logic. The digital Mean-timer modules were installed to reduce online dead time. Using these modules, a factor of two narrower veto width has been realized.

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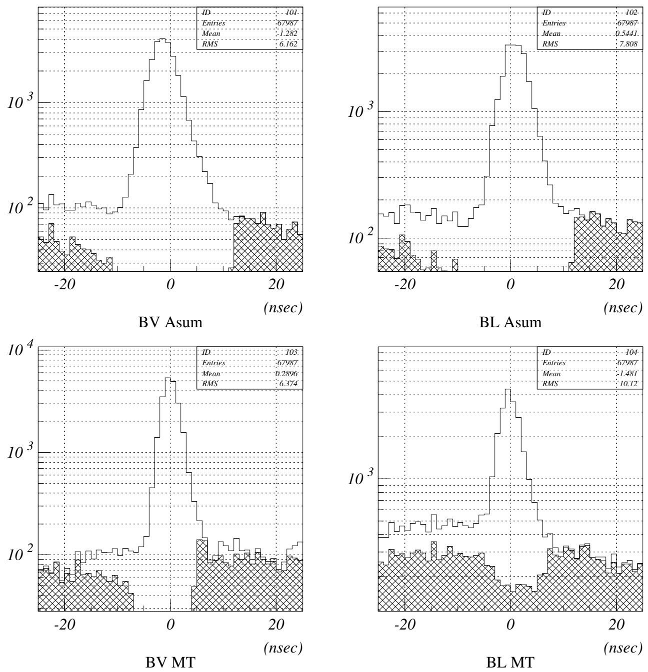

Fig. 13. Performance of the digital Mean-timer. Open histogram shows $K_{\pi 2}$ distribution of hit times in the photon veto systems when the bit is not set. Shaded histogram shows the time distribution for events with the bit set. In all cases the time distributions of the photon veto signals is shown relative to the time of the π^+ track.