Hybrid 5z66 Traveler

December 14, 1999

1 Connectivity

Repairs on shorts: Fe ClK low shorted to DVDD, fixed by cutting through a trace to isolate short and adding wire to bypass short. Also cut BE ClK high and had to add bypass wire to that too.

Made FE CLK lo opens on chips 4 and 5 while debugging short. Fixed opens by jumping from chip 3 to 4 to 5.

2 Chips

The following chips were assembled on this hybrid (in the order that the chips get read out):
Hybrid 5Z66 has die: 027-008 027-016 027-023 027-030 027-037

3 Data Analysis Summary

The following summarizes the findings of the Burn-in data analysis program. The first chip in the readout name is numbered 0.

```
% Hybrid 5z66 classification info. Created 14:10:42 12/13/99

Hybrid 5z66 quality: good
Chip classification: good good good good good
Bad channels: none
Bad cells: none
Random bad capacitors: none
Channels at pedestal needed for DCMS: 34.6 33.7 33.7 35.6 36.7
```

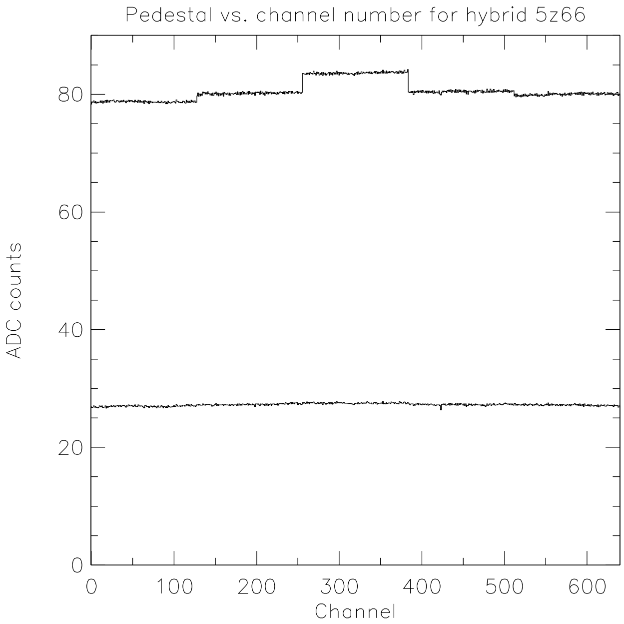
4 Comments

Has automatic Chip-to-Chip wirebonds.
HV Test.

5 Pedestal

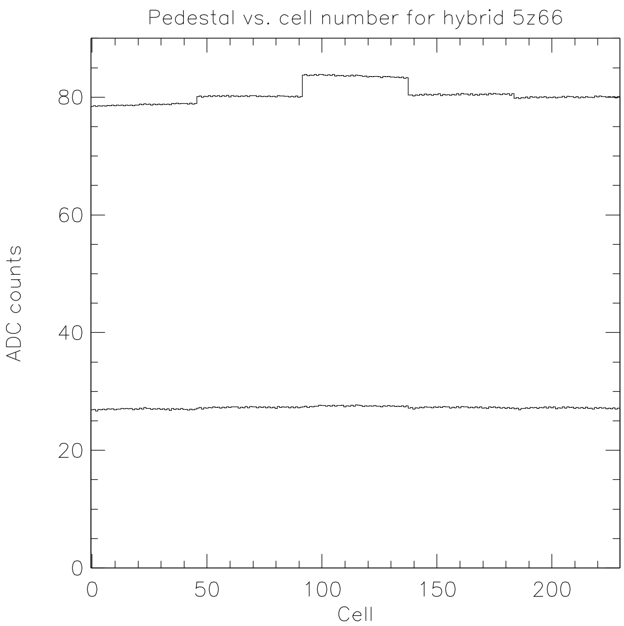
The following plot shows the pedestals vs. channel number with and without charge injection:

Pedestal for each Channel



The following plot shows the average pedestal vs. pipeline cell ID with and without charge injection. The x-axis is cell ID offset by 46 for each chip. Thus cell ID 5 for chip 1 is at x=5, chip 2 at x=51, chip 3 at x=97, etc.

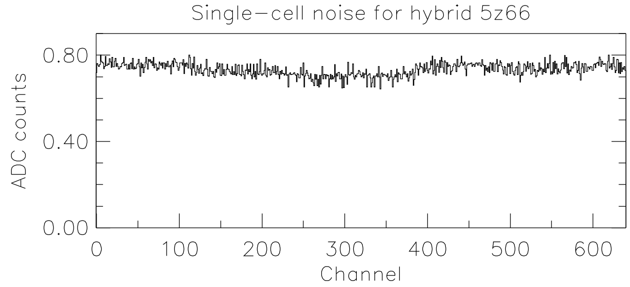
Pedestal vs. Pipeline Cell ID

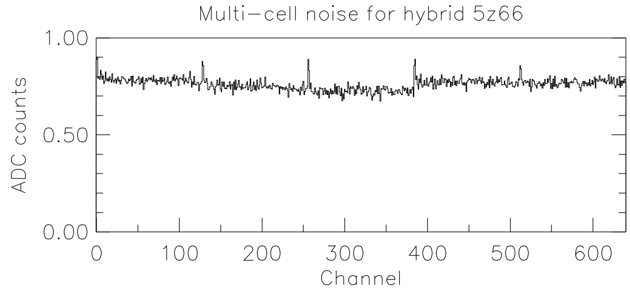


6 Noise

The following plots show the single-cell and multi-cell RMS noise:

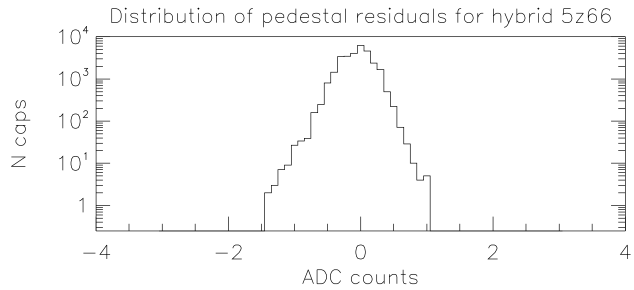
RMS Noise

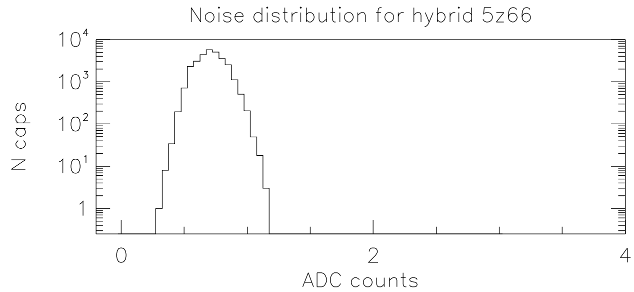




The following are histograms of the pedestal of each pipeline capacitor relative to the chip average (top); and the RMS noise of each capacitor (bottom):

Distribution of Pedestals and Noise





7 Currents

The following plots show the supply currents per chip as a function of measurment number. Currents are measured approximately every 10 minutes:

Supply Currents During Burn-in