PHENIX Central Arm Tracking Detectors

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The PHENIX tracking system consists of Drift Chambers (DC), Pad Chambers (PC) and the Time Expansion Chamber (TEC). PC1/DC and PC2/TEC/PC3 form the inner and outer tracking units, respectively. These units link the track segments that transverse the RICH and extend to the EMCal. The DC measures charged particle trajectories in the r-ϕ direction to determine p_T of the particles and the invariant mass of particle pairs. The PC's perform 3D spatial point measurements for pattern recognition and longitudinal momentum reconstruction and provide spatial resolution of a few mm in both r-ϕ and z. The TEC tracks particles passing through the region between the RICH and the EMCal. The design and operational parameters of the detectors are presented and running experience during the first year of data taking with PHENIX is discussed. The observed spatial and momentum resolution is given which imposes a limitation on the identification and characterization of charged particles in various momentum ranges.

1 Introduction

The PHENIX detector [1] at the Relativistic Heavy Ion Collider (RHIC) is designed to perform a broad study of A-A, p-A and p-p collisions to investigate nuclear matter under extreme conditions. The PHENIX tracking system, located in the two central arms of the detector, measures the momentum of charged particles from RHIC collisions, reconstructs invariant masses of electron and kaon pairs and contributes to particle identification. The three tracking subsystems are optimized for different functions. The low-mass multi-wire focussing Drift Chambers (DC) provide high resolution p_T measurements needed for determination of the invariant mass of particle pairs. The DC also participates in the pattern recognition at high particle track densities by providing position information that is used to link tracks through the various PHENIX detector sub-systems. Three Pad Chambers (PC) designated PC1, PC2 and PC3 provide three dimensional space points for the charged tracks and determine p_z/p_T. Both the DC and PC's provide position information for the LVL-2 trigger. A Time Expansion Chamber (TEC) identifies tracks originating from outside the fiducial volume and provides e/π separation in the momentum range from 250 MeV/c to 2.5 GeV/c using dE/dx information. Fig. 1 shows a schematic drawing of the PHENIX central arms indicating the positions of the DC's, PC's and TEC.

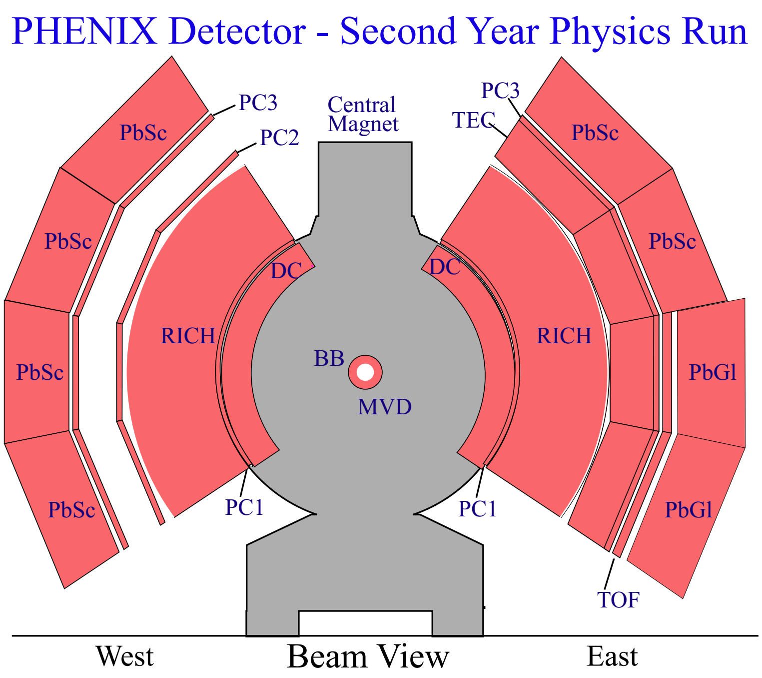

Fig. 1. The two central spectrometer arms, viewed in a cut through the collision vertex.

Central Au-Au collisions at RHIC produce charged particle multiplicities of dN_c/dy = 700 with a spectrum of soft particles peaking at 200-300 MeV/c.

The PHENIX tracking system is designed to track low-momentum particles where multiple scattering and particle decay make tracking difficult. The split in central-arm azimuthal coverage results in a large number of particles entering the detector's active regions without passing through the DC's. All three subsystems working together are needed to perform accurate tracking and pattern recognization in the high multiplicity RHIC environment. A detailed discussion of the three tracking subsystems follows.

2 The Drift Chambers

The PHENIX Drift Chambers (DC) are cylindrically shaped and located in the region from 2 to 2.4 m from the z axis and 2 m along the beam direction. This places them in a residual magnetic field with a maximum of 0.6 kG. The position of the DCs relative to the other detectors in the central spectrometer is shown in Fig. 1.

Each DC measures charged particle trajectories in the r-ϕ direction to determine p_T of each particle and ultimately, the invariant mass of particle pairs. The DC also participates in the pattern recognition at high particle track densities by providing position information that is used to link tracks through the various PHENIX detector sub-systems.

Simulations of ion-ion collisions at RHIC specified the requirements on p_T resolution and double track spatial resolution. The goal is to measure the $\phi \rightarrow e^+e^-$ mass with a resolution better than its natural width of 4.4 MeV and have good tracking efficiency for the highest multiplicities at RHIC. These considerations impose the following requirements on the DC:

– Single wire resolution better than 150 μm in r-ϕ .
– Single wire two track separation better than 1.5 mm.
– Single wire efficiency better than 99%.
– Spatial resolution in the z direction better than 2 mm.

2.1 Construction of the Drift Chambers

The DC system consists of two independent gas volumes located in the west and east arms, respectively. The east arm detector is the mirror image of the west arm. Each detector's volume is defined by a cylindrical titanium frame defining the azimuthal and beam-axis limits of the detector volume (Fig. 2). Five-mil Al-mylar windows define the limits of the gas volume radially. Each frame is filled with drift chamber modules and is divided in 20 equal sectors covering 4.5^o in ϕ. There are six types of wire modules stacked radially in each sector: X1, U1, V1, X2, U2 and V2. Each module contains 4 sense (anode) planes and 4 cathode planes forming cells with a 2-2.5 cm drift space in the ϕ direction.

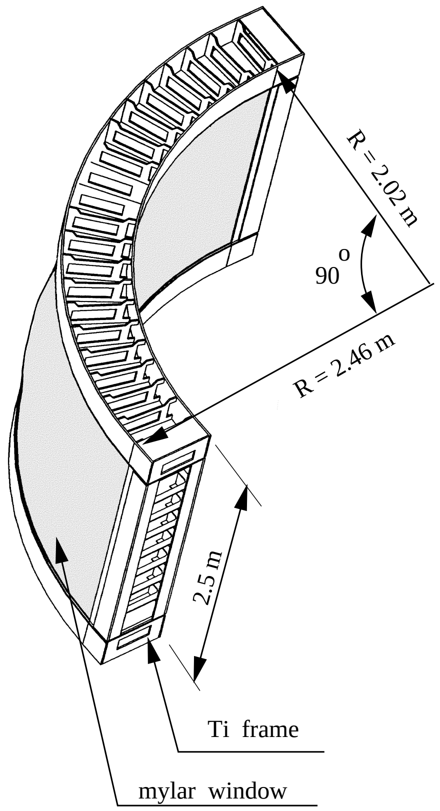

Fig. 2. Construction of DC frame.

The X1 and X2 wire cells run in parallel to the beam to perform precise track measurements in r-ϕ. These wire cells are followed by two sets of small angle U,V wire planes used in the pattern recognition. U1, V1, U2, and V2 wires have stereo angles of about 6° relative to the X wires and measure the z coordinate of the track. The stereo angle was selected to minimize track ambiguities by matching the z resolution of the pad chambers.

Each of the X- and U,V-stereo cells contain 12 and 4 anode (sense) wires, respectively. As a result, there are 40 drift cells in the DC located at different radii. The layout of wires within one DC sector is shown in Fig. 3. The stereo wires start in a sector on one side and end in a neighboring sector on the other side of the DC.

To satisfy the requirement of efficient track recognition for up to 500 tracks, each sense wire is separated in the center into two halves. Each half of a sense wire is then read out independently. To electrically isolate the two halves of

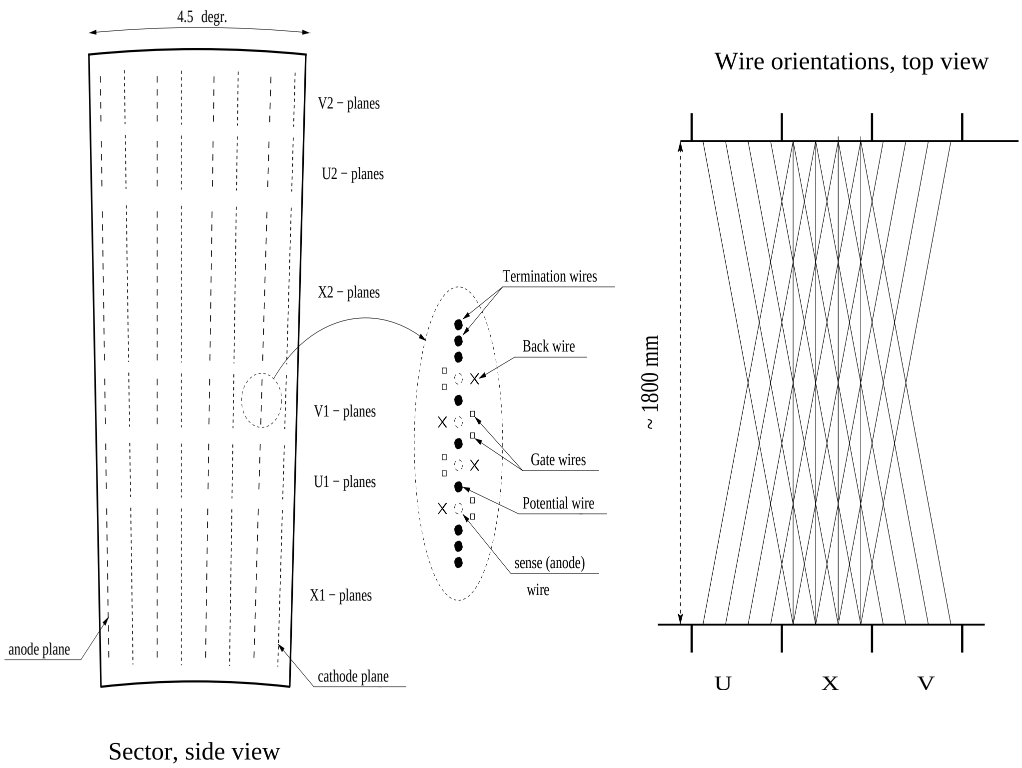

Fig. 3. The layout of wire position within one sector and inside the anode plane (left). A schematic diagram, top view, of the stereo wire orientation (right).

a single sense wire, the wire was attached to a low mass central support. The support was made with kapton of 100 μm thickness and introduces only very little additional mass in the fiducial volume of the chamber. Each wire plane in a cell has it's own kapton strip in the center to which the anode wires were attached and then cut in the middle. In total, the DC system contains roughly 6500 anode wires and thereby about 13,000 readout channels.

The wire configuration of the DC is similar to the controlled geometry drift chamber described in[2,3]. The focusing geometry eliminates the left-right ambiguity and reduces the number of potential tracks seen by each wire. At the same time it narrows the sampling length of primary electrons and improves two-track separation by decreasing the pulse width.

The anode wires are separated by Potential (P) wires and surrounded by Gate (G) and Back (B) wires. P wires form a strong electric field and separate sensitive regions of individual anode wires. G wires limit the track sample length to roughly 3 mm and terminate unwanted drift lines. This minimizes the time spread of drifting electrons from a single track and thereby decreases the pulse width. The B wire has a rather low potential and terminates most of the drift lines from it's side, essentially eliminating left-right ambiguity and decreasing the signal rate per electronics channel by a factor of two. There remains right-left ambiguity in the region ± 2 mm from the anode wire. Extensive numerical studies have been done to optimize the electric field configuration using the two-dimensional simulation code GARFIELD [4]. The cell potential configuration was optimized to achieve uniform gas gain within each cell, especially for the innermost and outermost wires in the U and V cells. Fig. 4 illustrates three calculations that helped define the optimum potential configuration.

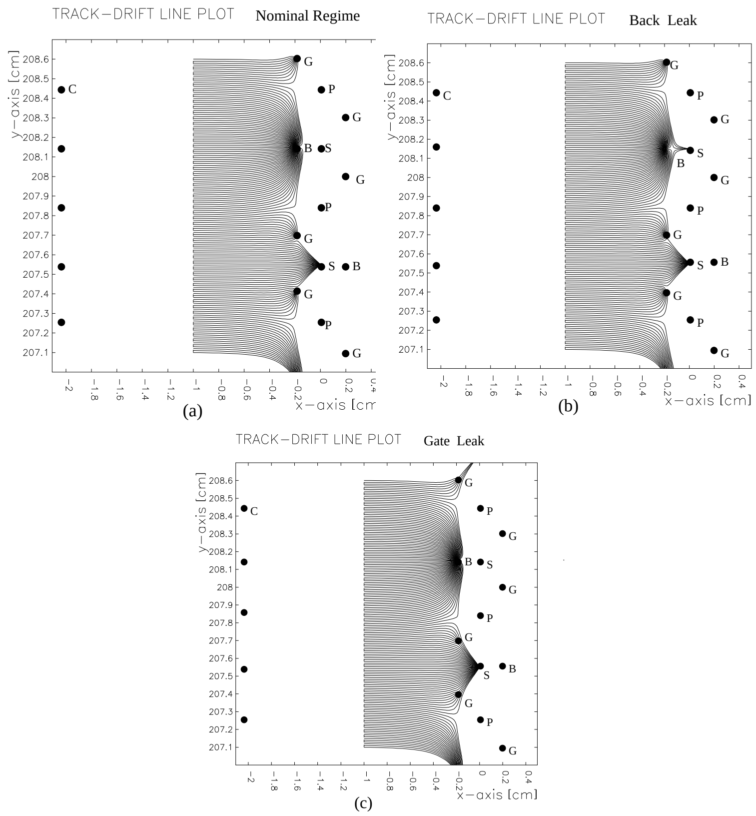

Fig. 4. Calculations of drift lines for three different types of electrostatic field configurations. Fig.(a) demonstrates the optimum regime. On Fig.(b) some of the drift lines penetrate behind the B wire and stop at the anode wire. This is a “leak” through the B side. On Fig.(c) the potential on the G wires is too high and some of the lines with longer drift length curve behind the G wires directly to the S wire. Different wire types are marked by letters: B - back, C - cathode, G - gate, P - potential, S - sense or anode wires.

The Ti frames and Al modules holding the FR4 cards with wire nets were fabricated at PNPI, Russia. The wire nets were wound partly in Russia and partly in the US. Each module was mounted into the chamber through open windows and supported by 3 bolts that penetrated holes in the Ti wall from each side.

To provide high voltage to each plane, separate wires (SIL-KOAT wires, WIREMAX P/N 1824) were routed through holes in the Ti frame and sealed with special ribbon plugs. For signal wires a Flex cable (Parlex Corp.) has been used. A plug with a slit was used for sealing the signal cable. The HV leads were connected to HV RC filters which were in turn connected directly to the signal ground of the amplifier. All elements of these filters were potted in resin (Cast-Coat inc., resin CC-301AD-FR-T) and showed no current leaks at the level of 10 nA at 6 kV. Each cell requires 4 different potentials : Potential, Gate, Back, and Cathode. The HV power system and HV monitoring allow one to independently feed each X module and each set of two UV modules. As a result there are 640 HV channels in 2 DC arms.

The total load to the Ti frame by all wire tensions is roughly 4.5 tons. To avoid significant bending of the frame an additional carboplastic strut 2 inches in diameter was installed in the middle. Before module installation the frame was loaded to full strength by a set of springs. The measured map of actual distortions was used to compensate the deflections by adding or removing additional thin washers between the frame wall and the modules.

After installation of the anode wire tensions were measured using electrostatic excitation. The deviations of the wire tension did not exceed 10% of the nominal value. The chambers were conditioned at high voltage in a dry nitrogen atmosphere. The corona discharge on the anode wires allows one to burn away possible dust and other impurities. Afterwards the chambers were filled with a working gas mixture of 50% Ar and 50% Ethane.

2.2 Drift Chamber Front-End Electronics

The DC signals are read out by custom electronic circuit cards that are mounted onto the detector in the twenty sectors on each side of the detector. Each sector houses 4 “ASD/TMC cards” and one “FEM” card. The ASD/TMC card contains 6 ASD8 chips and 10 TMC chips. It amplifies and digitizes signals from 40 anode wires. This card is named for the chips it uses at each stage of the signal conditioning. The FEM or Front End Module card controls the triggering and readout of the digitizers, formats the data, and allows for slow control access to parameters such as discriminator thresholds.

Signals from the wires are resistor-diode protected and then DC coupled into the differential inputs of the ASD8 chip. The ASD8 [5] chip contains 8 channels of pre**A**mplifier, a 6 nsec **S**haping amplifier, and an externally controlled **D**iscriminiator. Our implementation uses moated local grounds and independent low voltage regulators for each ASD8 chip. Our grounds are moated since each chip has a ground pad and local regulators inside the moat, and only a ”drawbridge” connecting it to its neighbors. An 8-channel DAC sets the threshold of the individual discriminators to typically 6 pC. This results in a hit probability well under 0.1% in our roughly 500 nsec digitization window.

The discriminator output signals are connected to Time Memory Cell (TMC) chips. We use the TMC-PHX1 version which is a VLSI implementation of the

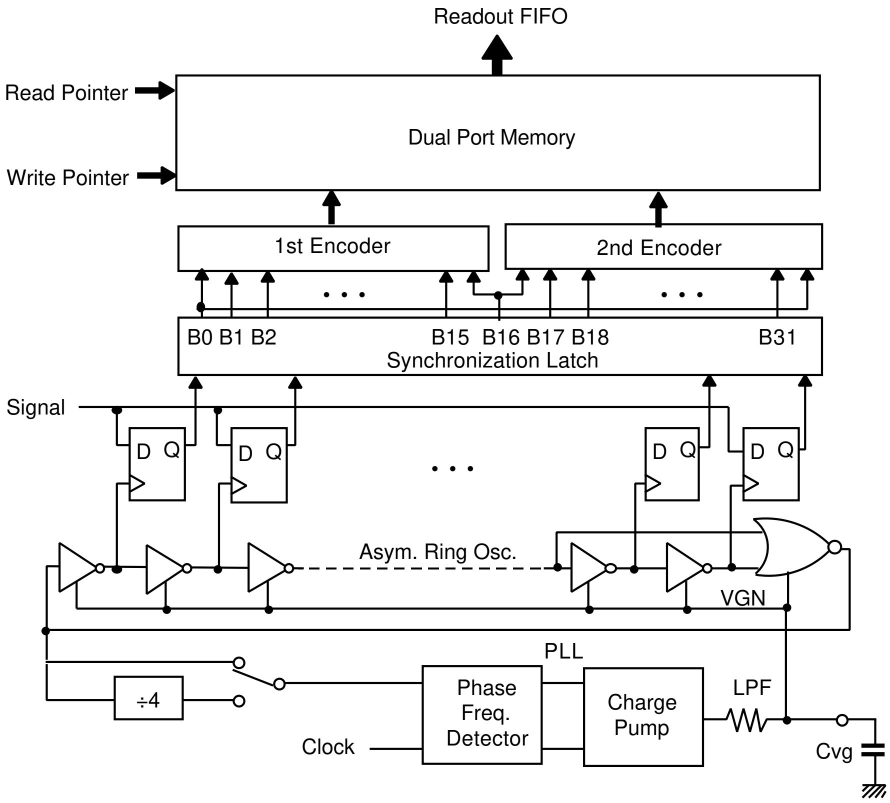

Fig. 5. Logic diagram for the input to a single TMC channel

TMC technology coupled with an on-board encoding and buffering scheme specific to the PHENIX drift chamber needs [6]. The logical diagram of a single channel of the TMC-PHX1 chip is shown in Fig. 5. The signal (logical 0 or 1) comes in from the lower left. This signal is latched on the series of D flip flops (FF) via a cascading clock signal. The cascading clock signal is tuned via a phase-lock loop (PLL) so that it completes the cascade sequence in one period of the external clock. Thus, the 32-bit word in the FF array is essentially a time history of the ASD's discriminator output in bins whose time interval is 1/32 of the clock period. By using 4 times the RHIC crossing clock rate as out reference we achieve a single bin resolution of roughly 0.8 nsec.

Due to limitations in memory space on board of the TMC-PHX1, we cannot store the raw 32-bit words from each clock cycle. Instead each 16-bit half of the word is encoded down to 5 bits by storing only a single edge (leading or trailing) from its time interval. At the end of each clock cycle a pair of 5 bit words is written into a 256 cell circular memory buffer. In this way, the TMC maintains a continual running history of all leading and almost all trailing edges spanning the previous 6 μsec, which is longer than PHENIX trigger time desition of 4 μsec.

Upon receipt of a trigger, the TMC copies a portion of the circular memory buffer to an output FIFO. Internal registers select the offset (how far in the past to look for the data) and the interval used for filling the output FIFO. The output FIFO is sized so that it can hold 5 PHENIX events allowing the triggers from one event to overlap with the readout of a previous one.

The FEM card acts as the controller for four ASD/TMC cards. It receives triggering and readout requests from the PHENIX DAQ [7] via a GLink optical fiber which transmits 20 bit words at 4X RHIC clock. Different bits in this word are used as triggers, readout requests and reset commands. A pair of Altera Flex8000 FPGA chips act as the Heap Manager (HM)[8]. The HM uses mode bits to control the operational state of the FEM's, formats the data into a packet and forwards it to the Data Collection Modules (DCM). The HM code is held in on-board EPROM's which are used at bootup and can also be reprogrammed via slow controls. The FPGA's are responsible to sort and format the data as well as construct header information with event and clock counters. Nominally the FEM has two GLink output streams, each operating at 40 MHz and 20 bits. For the initial implementation, all the data are sent through one output stream. Finally, the FEM card houses a PHENIX standard ARCNet card. This card provides slow communications for tasks such as setting the discriminator thresholds. The PHENIX design allows for the insertion of custom code into the ARCNet cards nonvolatile memory. Our implementation allows for single batch commands which execute cold start and multiple threshold settings in single commands. The power consumption per one sector is about 80 W and water cooling is used to remove the heat.

2.3 Adjustment and Performance of the Drift Chambers

The electrostatic field in the chamber needs fine adjustment to satisfy all required specifications. The single wire efficiency was adjusted to be 95-96%. This allowed us to keep the mean pulse width to near 35 nsec and therefore maintain double track resolution to better than 2 mm. We were also able to maintain the track-finding efficiency at better than 99%. The single wire resolution was found to be 165 μm.

To estimate the DC performance in left-right ambiguity rejection the "back wire efficiency" parameter was introduced which measures the probability of getting a hit on an anode wire when the track passed on the back or shielded side. After adustment of the B wire potential, the average B wire efficiency did not exceed 5%. A single track resolution of about 165 μm was determined as a residual of wire hits to the fitted tracks. This is very close to the design specification.

The Drift Chambers were installed, commissioned and operated in the two

PHENIX central arms. The DC design was proven under experimental conditions to provide single wire efficiency, single wire resolution, two track efficiency and back efficiency performance at or near the design specifications. The DC was used to collect large amounts of data during the year-1 and year-2 PHENIX runs.

3 The Pad Chamber System

The PHENIX Pad Chambers (PC) are multiwire proportional chambers that form three separate layers of the PHENIX central tracking system. Each detector contains a single plane of wires inside a gas volume bounded by two cathode planes. One cathode is finely segmented into an array of pixels. The charge induced on a number of pixels when a charged particle starts an avalanche on an anode wire, is read out through specially designed readout electronics.

The PC system determines space points along the straight line particle trajectories outside the magnetic field. Fig. 1 shows the radial location of the PC's in the central tracking arms. The innermost pad chamber plane, called PC1, is located between the DC and the Ring Imaging Cherenkov Counter (RICH)[9] on both East and West arms. Also on both arms, PC3 is mounted just in front of the Electromagnetic Calorimeter (EMCal)[10] while the PC2 layer behind the RICH is present in the West arm only. The PCs are the only non-projective detectors in the central tracking system and thus are critical elements of the pattern recognition. PC1 is also essential for determining the three-dimensional momentum vector by providing the z coordinate at the exit of the DC.

PC information is also essential for particle identification, particularly for critical electron identification which has to have a hadron rejection factor of 10^4. The DC and PC1 information gives direction vectors through the RICH, while PC2 and PC3 are needed to resolve ambiguities in the outer detectors where about 30% of the particles striking the EMCal are produced by either secondary interactions and particle decays outside the aperture of the DC and PC1 or low-momentum primary tracks that curve around PC1 in the magnetic field and strike PC2 and PC3. The recognition of three points on a straight line track through the whole spectrometer ensures that the response from the electron identifying detectors (RICH, TEC and EMCal) and the momentum from the DC are correctly correlated for particle identification.

3.1 Pad Chamber Design

Several performance and spatial constraints drove the design of the PC's. A low occupancy, in spite of the expected high charged particle multiplicity, dictated the pixel granularity of the cathode plane. The size of the pixels was governed by the need for good position resolution in the z direction, while for the purpose of pattern recognition, position resolution was not the main issue, but rather high efficiency and reliable hit information. This was accomplished by a readout design where the cathode is segmented in small cells which have a size similar to the required position resolution. Reading out the information with the simplest possible digitization and comparing the measured signal with a discriminator threshold is sufficient to achieve the required position resolution.

A special pad design was invented, where each cell contains three pixels and an avalanche must be sensed by all three pixels to form a valid hit in the cell. By the triple coincidence requirement, electronic noise is unlikely to produce a false hit, which is a known problem of discriminator readout. However, this arrangement is costly in terms of electronic channels. Thus, the interleaved pixels were ganged together (Fig. 6), nine by nine and connected to a common readout channel, such that the three pixels in a cell are always connected to different but neighbouring channels and each cell is defined by its unique channel triplet. So, the information can be broken down to the cell level, by identifying the triplets.

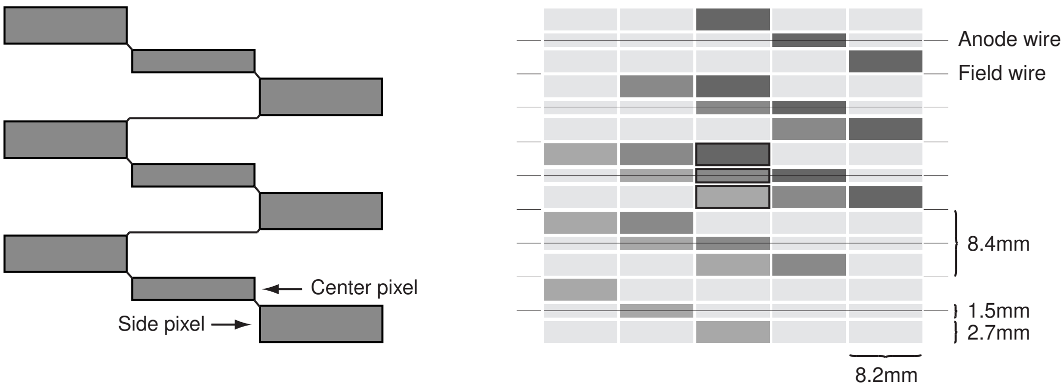

Fig. 6. The pad and pixel geometry (left). A cell defined by three pixels is at the center of the right picture

This solution saves a factor of nine in readout channels compared to readout of every pixel and a factor of three compared to a readout pad geometry where a cell is the actual electrode connected to an electronics channel. The design goals for the position resolution were $\pm 4mm$. This motivated an anode wire spacing of about 8 mm. For geometrical reasons, a spacing of 8.4 mm was chosen. Desiring a square cell geometry, a cell area of $8.4 \times 8.4 mm^2$ was adopted. In the z direction this resulted in a position resolution of $\pm 1.7mm$ which was substantially better than the design goals. At the positions of PC2 and PC3 it is sufficient to maintain the same angular resolution as on PC1. Thus the cells on PC3 have 4 times the area of PC1 cells since PC3 is at twice the distance from the crossing beams as compared to PC1.

3.2 Pad Chamber Construction

Each detector consists of a single plane of anode and field wires lying in a gas volume between two cathode planes (Fig. 7). One cathode is segmented into pixels and the other is solid copper. Signals from the pixels are routed outside the gas volume where they are amplified and discriminated by the Readout Cards (ROC's) which populate the motherboard forming the outer face of the detector. The Front End Modules (FEM's), located at the outside edge of the detectors handle the power for the communications with and the control of the ROC's via bus traces on the motherboard.

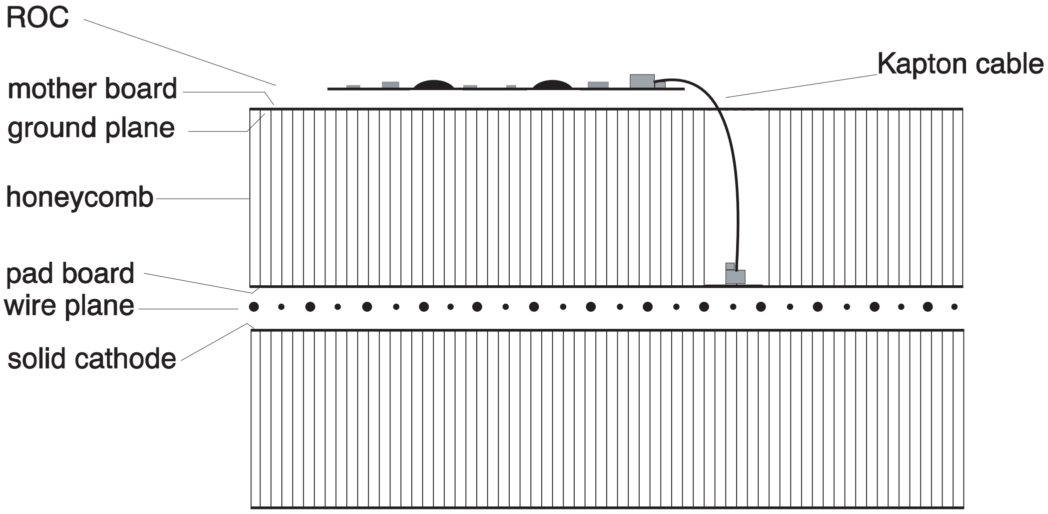

Fig. 7. Vertical cut through a chamber.

The basic construction unit of a chamber is the cathode panel, either plain or pixel type. Each panel is fabricated as an FR4-honeycomb-FR4 sandwich where the FR4 facesheets are clad with copper if they are part of the electronic system of the chamber. The sandwich structure, being extremely stiff, provides the mechanical strength of the chamber and no frame construction is needed on PC1. The wires are strung between terminal boards at each end of the pixel cathode panel. This makes PC1 extremely light and very little material is placed in the fiducial volume of the spectrometer arms. The lack of frames makes it neccessary to close the gas volume by gluing the two panels together. This construction allows the 8 separate PC1 chambers (each being about $0.5{\times}2\ \mathrm{m}^2$ in size) of an arm to be mounted side by side leaving only 0.7% of insensitive area. The radiation thickness of PC1 is only 1.2% of a radiation length (including the readout electronics).

PC2 and PC3 chambers, which are much larger than PC1, have less critical constraints on material thickness. Therefore, construction with the two cathode sandwich panels supported around the edge by a fiberglass (S2) frame could be used. This allows the gas volume to be sealed by an O-ring when the two panels are bolted together along the frame.

The pixel cathode panel is the most challenging of the two panels. The very large circuit boards ($0.5{\times}2\ \mathrm{m}^2$ on PC1 and $1{\times}2\ \mathrm{m}^2$ on PC3) forming the skins of the sandwich have etched patterns with trace width and trace spacings of 0.150 mm, a pitch that is a challenge even on miniature boards. The pixel board has in addition approximately 4500 copper plated holes bringing the signals from the pixels to microconnectors soldered on the opposite side of the pixel board. Extensive testing was needed by a semiautomatic custom made test system, with spring loaded needles providing electrical contact, to assure the quality of etching and hole plating. Microconnectors were soldered to the pixel board and flexible, flat Kapton cables were inserted in the connectors before the board was glued together with the honeycomb (which had slits cut out to allow the Kapton cables through). Thereafter, the top board (the motherboard) was added to the sandwich. The motherboard carries the traces for the readout electronics on the outer surface and a continuous groundplane (for shielding and ground distribution) on the inner surface.

The mechanical strength of the sandwich relies on the FR4 boards being as flat and parallel as possible. Gluing was done on flat granite tables using a vacuum bag to press the pieces together. The PC2 and PC3 chambers were too large for the pixel board (and motherboard) to be etched in one sheet. Two pixel boards ($1{\times}2\ \mathrm{m}^2$) had to be patched together to fit the $2{\times}2\ \mathrm{m}^2$ chamber size (approximate PC3 chamber area). Similarly two motherboards must be glued together. An S2-glass tube with rectangular cross section, with the side equal to the honeycomb thickness, served as a joint piece at the seams for both the two pixelboards and the two motherboards. The honeycomb fills the volume of the sandwich. All frames are manufactured from long bars of S2 fiberglass and glued onto the panels.

Wires were wound onto the pixel panels in winding machines. The wires were mechanically fixed to the terminal boards by gluing and the electrical contact to the high voltage was made by soldering. With the wires in place, the chambers were closed and tested for HV performance and gas tightness. Thereafter, the chambers were ready for electronics mounting.

3.3 Pad Chamber Readout Electronics

The total PC system comprises 172,800 electronic channels. All amplifying and digitizing electronics were implemented in custom made integrated circuits[8]. The cost per channel could be kept low due to the simple nature of the information (1 bit per channel). This also resulted in advantageous properties in terms of data volume, power dissipation and simplicity of design, operation and maintenance. The extremely large channel density (4320 channels on a chamber) makes it necessary to use the flat chamber surface for mounting that part of the readout electronics where all channels are treated in parallel.

Two integrated circuits were developed. The TGLD[11] chip contains 16 parallel channels of charge amplifier plus discriminator. Thresholds can be set as low as an equivalent of 1.5 fC input charge. Many operational characteristics of the chip are remotely programmable via serial communication. Most important are the discriminator threshold and amplitude of the internal test charge injection. A memory chip, the DMU, stores all results from three TGLD chips, while waiting for a potential level-one event trigger. The 48 bits of data, corresponding to a valid trigger are stored until being read out. Up to five events can be stored in the DMU pending readout.

To place the readout electronics in the fiducial volume of the spectrometer, where the material thickness had to be kept to a minimum, required using modern miniature assembly techniques. The readout card (ROC) (Fig. 8) houses three TGLD chips and one DMU chip, i.e. it handles 48 channels. The ROC can be regarded as a multichip module where the assembly is done by the Chip-On-Board technique on a 100 μm thick Kapton circuit board. In this technique, the bare silicon brick is glued to the board and the electrical connections are made by ultrasonic wirebonding directly between the chip and circuit board. A ROC is $4 \times 6 \ \ \mathrm{cm}^2$ large and it connects to the cathode pads by Kapton cables through the honeycomb. Ten rows of nine ROCs in each row, communicate to the side of the detector (outside the fiducial volume) via traces on the motherboard. The signals and DC supply to and from the ROCs in a row are bussed throughout the row. Only the serial DMU output goes individually from each ROC. All digital signals are communicated as differential RS485 standard. The differential signals are translated to CMOS standard by translator chips placed on the connector cards which are soldererd to the traces on the motherboard. The connector card carries a miniature connector into which one side of the ROC, shaped as a flat cable end, is inserted. The total weight of a ROC, a connector card, Kapton cables and the associated connectors is 4.8 grams. On PC1, where the channel density is the highest, this corresponds to a radiation thickness of 0.2% of a radiation length.

At the side of the detector the FEM card handles the communication to and

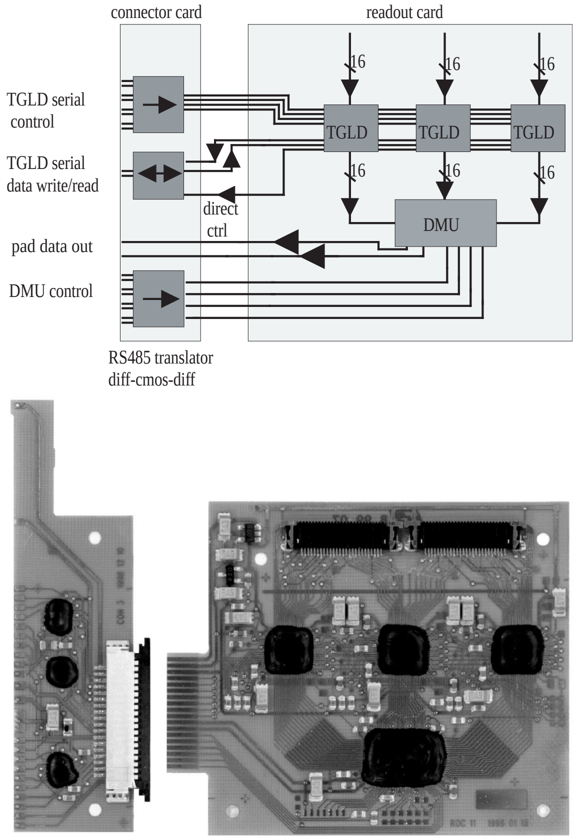

Fig. 8. Block scheme of the connector and readout card (top), photograph showing how it looks in reality (bottom).

from five ROC rows. Data are serially read from each DMU for all ROC's in parallel. At the FEM, the data is formatted for suitable transmission on one optical fiber, away from the detector to the counting house where the DCM's interface the data to the event builder. This architecture is the same for all subsystems in PHENIX and it is described in another contribution in this volume [7].

3.4 Pad Chamber Performance

During the past year, the PC system showed a performance easily reaching the design goals both during real data taking at high multiplicity and in extensive studies with cosmic rays. 99.5% efficiency is routinely obtained at a setting which has a margin of at least a factor 2 in chamber gain and discriminator threshold. Fig. 9 shows the achieved efficiency as a function of the applied anode voltage at the nominal threshold setting (at which the electronics are totally free of noise). All three chamber types show plateau efficiencies of 99.5% or better. The filled circles represent the results when a detected particle is required to have resulted in at least three neighboring fired pads (the normal operating condition). Relaxing this to accept only two neighboring fired pads as a valid hit, allows the plateau efficiency to be reached at slightly lower gain (open squares).

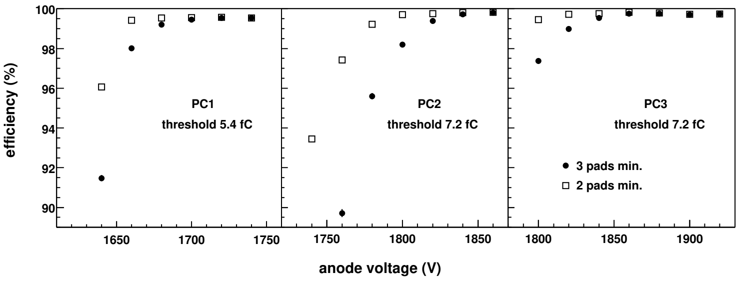

Fig. 9. Efficiency curves for PC1/2/3 with varying high voltage at fixed thresholds.

The position resolution was measured to be ± 1.7 mm for PC1 along the wire (the z direction) in good agreement with the simulated performance. Perpendicular to the wires this readout provides the same resolution as normal wire readout (where drift time information is neglected), i.e. one can determine on which wire the avalanche was situated. In case one particle starts an avalanche on two wires (due to an inclined track) the reconstructed hit position will be right between the two wires.

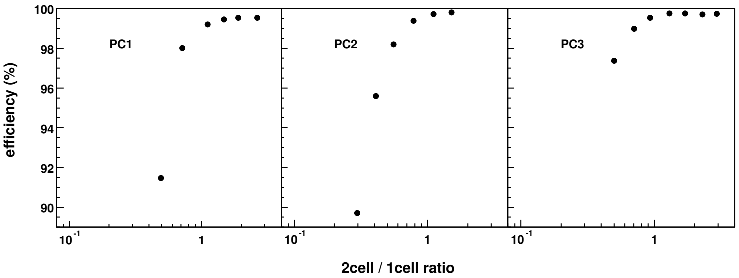

Fig. 10. Efficiency vs. two-cell/one-cell ratio.

An avalanche will most often give rise to a cluster of fired cells. Simulations have shown that the fraction of 2-cell clusters compared to 1-cell clusters is a sensitive measure of the detection efficiency. In Fig. 10 this has been expressed for the cosmic data as the ratio between the fraction of 2-cell clusters and 1-cell clusters. When plotted against the efficiency we can conclude that monitoring this ratio to be larger than 1 will ensure the operation at maximum plateau efficiency. Thus the PC system can be kept at the optimal gain-threshold operating point without any additional quantitative gain information.

The PC system, is now fully installed with 172,800 electronic readout channels distributed over PC1 and PC3 chamber planes in both arms and a PC2 plane in the West arm only. The system has reached all design goals by an ample margin, resulting in particularly simple commissioning and operation. The data produced by the system has proven to be easy to understand and the hit reconstruction software, based on simulations and tests with small chambers, has produced fast and reliable results. The data has played an important role both in the first physics analyses and in detector performance studies of other systems in the tracking spectrometers. Due to the proven reliability of the hit information available after a few hundred microseconds, the PC's will be essential for more selective Level-2 triggers in the high luminosity runs coming in the future.

4 The Time Expansion Chamber

The Time Expansion Chamber (TEC) is composed of a set of 24 large multi-wire tracking chambers arranged in four, six-chamber sectors which reside in one of the PHENIX Central Spectrometer (CS) arms. The TEC performs a number of functions for the experiment[12]. It measures all charged particles passing through its active area, providing direction vectors that are matched to additional track information from the DC's and PC's also located in the CS. The tracking information is used to solve the complex pattern recognition problems associated with the high particle multiplicities in relativistic heavy ion physics. It aides in background rejection for particles passing into the EM-Cal [10] and TOF [9] wall. The detector system allows for systematic studies of tracking efficiency and background rejection versus multiplicity in coordination with the DC. The TEC also enhances the momentum resolution of the CS at $p_T \geq 4GeV/c$ by combining with the DC to provide a long lever arm for improved track-angle resolution. In addition the TEC measures ionization energy losses (dE/dx) of charged tracks which enables particle identification, particularly electron/pion separation, over a momentum range important to the physics goals of the experiment. Finally, the TEC has been designed with features allowing for an eventual upgrade to a Tracking-TRD[13]. The future upgrade will significantly extend the momentum range of electron identification out to tens of GeV/c.

4.1 Time Expansion Chamber Description

The TEC resides in the PHENIX East Spectrometer (ES) arm. Its four sectors match the ES arm's acceptance, covering $\pi/2$ in azimuth and ± 0.35 in η (Fig. 1). Each sector subtends $\pi/8$ in azimuth and is located between inscribed circles of radius 4.23 m and 4.88 m where the origin is the beam-collision point. The subsystem has a total of 20,480 readout channels and contains 63,080 wires.

The TEC is composed of individual chambers, with six chambers stacked together to form a wedge-shaped sector (Fig. 11). Each chamber is indepen-

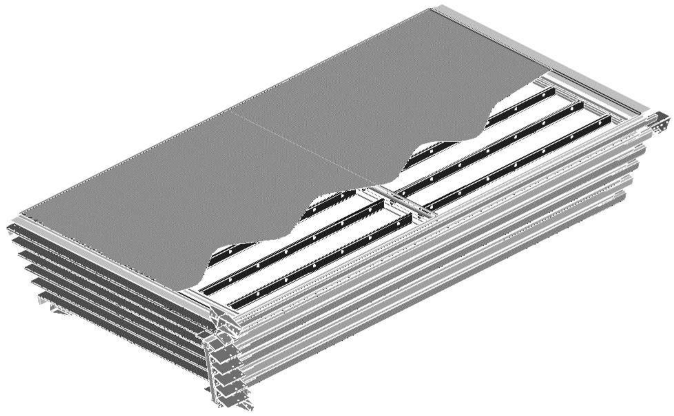

Fig. 11. TEC six-plane sector.

dent and self-supporting, made from a combination of machined graphite-composite, S2-glass and FR-4 components all epoxied together. Individual chambers have active areas varying from 3.1m x 1.7m for the smallest to 3.5m x 1.9 m for the largest TEC plane. The material in the detector's active area was minimized by using a box beam wire divider located at z=0 and widely spaced I-beam window supports all made of thin FR-4. The open design results in 98% of the TEC's fiducial area being active.

Each chamber is built in two layers: a lower layer containing structural elements for window support and space for inclusion of TRD radiator foils, and an upper layer containing the active elements of the wire chamber. The upper layer is filled with P-10 gas and is composed of a Cu-mylar cathode window, 3 cm drift space, three wire planes (field, anode, field) oriented parallel to the z axis of the detector, and a final Cu-mylar cathode window (fig. 12). The anode wires are spaced on average 4 mm from each other (specifically 4.05 mm and 4.15 mm depending on the sector plane) and 3.0 mm from both cathode wire planes. The Cu-coated mylar windows have multiple functions. They are biased to establish the proper field shaping inside the detector, serve as the gas barrier and provide an RF shield. The wire planes are divided in half at z=0 both for ease of construction and to decrease the average multiplicity per wire by a factor of two. The anode wires were 25 μm Au-coated W-Re and the field wires were 50 μm Au-coated Cu-Be.

4.2 Time Expansion Chamber Electronics

Every anode wire of the TEC was instrumented with the electronics chain described in Fig. 13. The 32-channel analog printed circuit boards (TEC-PS) were mounted on each chamber and contained 4x8-channel preamp/shaping amplifier ASIC's, calibration circuitry and opamps to drive the signal over the $\sim$8 m of twisted pair cable to the carriage racks containing the TEC FEM's.

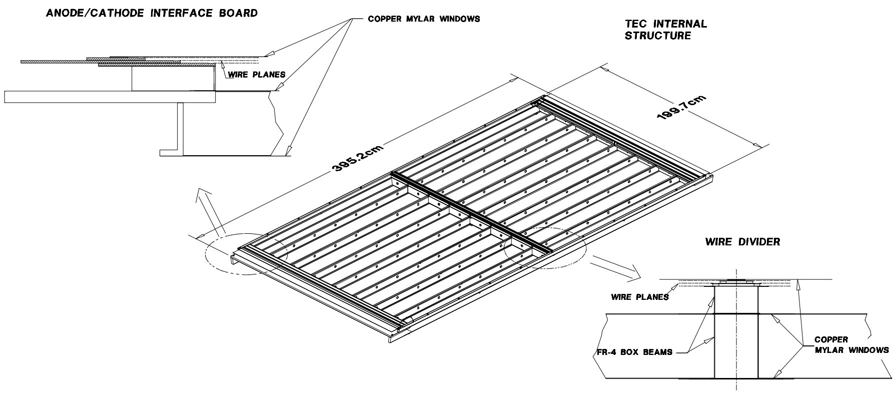

Fig. 12. Mechanical structure of single TEC chamber. The frame skeleton, anode-cathode interface board and central wire divider are shown.

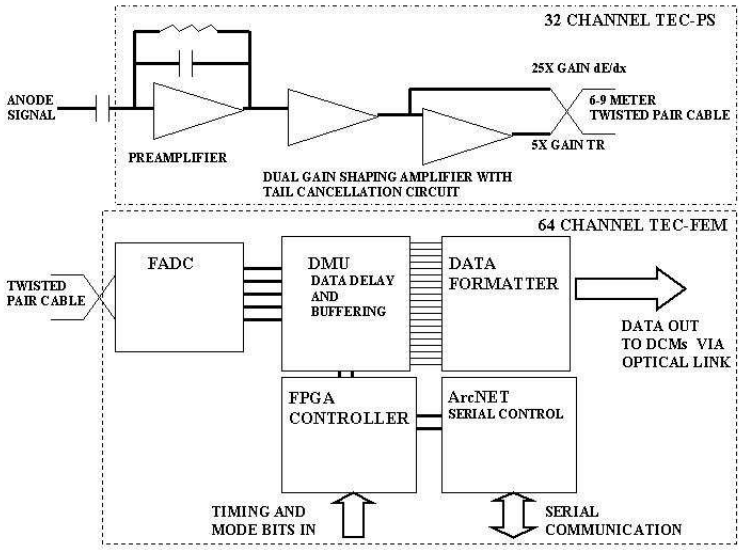

Fig. 13. TEC electronics chain block diagram. The 32-channel TEC-PS boards are mounted directly on the chamber. Signal cables connect the TEC-PS boards to electronic crates containing TEC FEMs.

The 64-channel TEC FEM's receive the analog signals from the TEC-PS , digitize and format the data and send their output over fiber-optic lines to the PHENIX Counting House. There are currently 440 TEC-PS boards and 216 TEC FEM's operating on the PHENIX TEC.

The preamp/shaping amplifier ASIC's (TEC-PS chip) has an average 95 ns shaping time, unipolar output and tail cancellation circuitry [14]. The chip has dual gain output of 5X and 25X to increase the dynamic range of the electronics, enabling it to be sensitive both to the dE/dx energy deposit of the minimum ionizing particles and the x-rays produced through transition radiation. The shaping time, gain and pole-zero of each channel on the ASIC are adjustable through digital down-load. The feature allows each analog electronics channel to be adjusted remotely or to be completely disabled. In addition, each TEC-PS board contains a remotely programmable DAC along with a pulser circuit that is used for electronic calibration and debugging. This is combined with the individual channel enable/disable feature to allow one to send calibration pulses to any combination of channels on the detector which is used as a major diagnostic tool for the TEC.

The TEC FEM digitizes the analog signal using a Flash ADC (FADC) ASIC. The digitized signal is then buffered with a custom Digital Memory Unit (DMU) and formatted with a combination of buffers, registers and programmable gate-arrays (FGPA's). The custom FADC is non-linear with 5-bit encoding and 9-bit dynamic range. The range and pedestal of the FADC can be adjusted remotely. The chip runs at 37.7 MHz, or 4X the frequency of the collider-beam crossing. The DMU is also an ASIC. It is programmed for the proper latency associated with the experiment's Level-1 trigger decision and also contains a 5 event data-driven buffer. The TEC FEM's digital parameters and programming can be down-loaded through an ARCNet link on each board. The formatted data on the FEM is transmitted to the PHENIX Counting House via a 1 GHz Glink optical fiber link.

The electronic noise associated with the detector was carefully studied. Individual chambers in a quiet lab environment were able to obtain noise values of 0.3 fC/channel RMS at the output of the TEC-PS board which is close to the equivalent input noise charge (ENC) of the preamp/shaper itself. The electronic noise with the full system operating on the PHENIX carriage has an average noise/channel between 1 and 2 fC RMS, which is dominated by coherent noise. This is within the system design specifications.

4.3 Time Expansion Chamber Operation and Performance

The TEC wire chamber contains a combination of metalized-mylar cathode planes and wire planes which are biased to shape the electric field and set the gas gain. A charged track passing through the TEC ionizes the gas and the resulting electron clusters drift in the radial direction into the amplification region where the signal is collected by the anode wires (Fig. 14). With P-10 gas in the TEC the maximum electron cluster drift time is 1.3 μsec. The TEC is typically operated with an effective gas-gain range of 2000 to 5000. The FADC readout combines with the radial drift to give an electronic image of each track. On average there are 50 time slice samples for each track passing through a TEC plane. Each time slice provides both a position measurement in r and ϕ, and a dE/dx measurement. The position measurements are translated into direction vectors for each track to be used in both the pattern recognition and momentum determination. The dE/dx can be used for particle identification, especially for separating electrons from pions in the range 200 MeV/c to 2.5

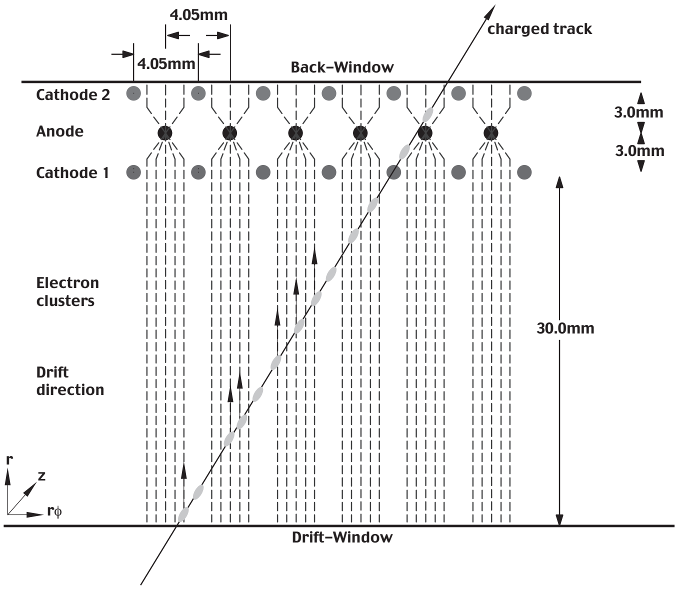

Fig. 14. Schematic detailing operation of the TEC. The anode-cathode configuration is shown together with the $\vec{E}$-field lines. A charged track traversing the TEC leaves electron clusters in the gas volume which drift to the anode wires where the multiplication avalanche occurs. Signals from the anodes are read out through the TEC electronics chain.

GeV/c.

The position resolution of the TEC was measured using real data events. After selecting low multiplicity data to assure a clean sample the same track was reconstructed using either planes 0 and 2 of the TEC or planes 1 and 3. Comparison of the track coordinates in the two cases gives the TEC space resolution multiplied by $\sqrt{2}$ since the resolution is included twice in this comparison (Fig. 15). The measured 2-plane resolution of 770 μm is larger than the resolution of 500 μm which was predicted. Additional studies have determined the degraded resolution is because the TEC was operated at an effective gas gain range of 2000-2500 for this data set rather than the designed gas gain of 5000. Once the correct gas gain was established the TEC simulation [15] was used to determine the 4-plane resolution for the data (Fig. 16). The TEC 4-plane resolution for the year 2000 data set was 380 μm which can be improved to 260 μm by increasing the chamber gas gain, which will be done for subsequent runs.

Track reconstruction with the TEC is done using a combinatorial Hough transform. In this method a space is defined with coordinates ϕ and α. The polar angle at the intersection of a track with a reference radius near the radial midpoint of the TEC is ϕ and the inclination of the track at that point is α. The α angle is inversely proportional to the p_T of the particle. All TEC hits in 4-planes are mapped pairwise into the ϕ-α space. The mapping typically results in peaks in the pairwise plot that corresponds to real tracks. The overall TEC

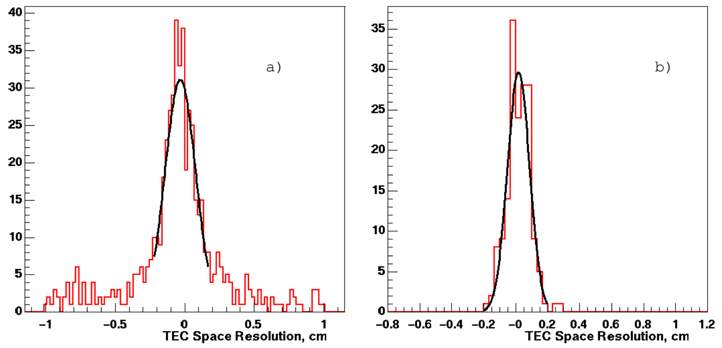

Fig. 15. TEC 2-plane position resolution. a) Position residual of real tracks reconstructed using TEC planes 0,2 vs plane 1,3 where plane 0 is the one nearest the interaction point. Two-plane resolution from real data 770 μm RMS. b) Two-plane resolution calculated from simulated TEC data 500 μm RMS assuming a gas gain of 10^4.

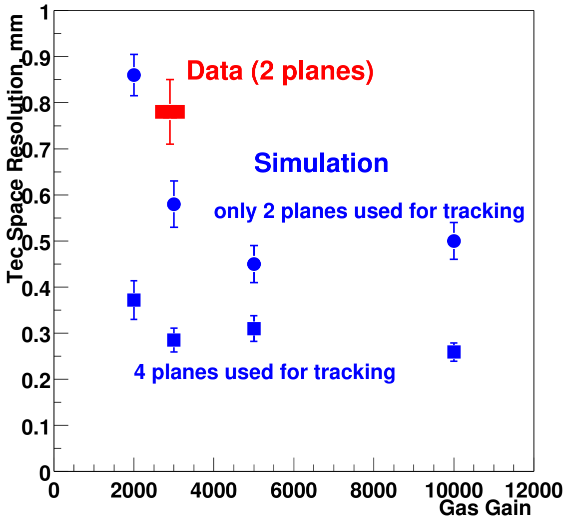

Fig. 16. Simulation results of TEC 2-plane and 4-plane resolution vs. gas gain. The 2-plane simulation results are compared with a data point at a gas gain of between 2500 and 3000 (one data point with wide rectangle). Combining data measurements and simulation yields TEC 4-plane position resolution of 380 μm RMS for typical gas gain (between 2000 and 3000) during data taking.

tracking efficiency versus multiplicity and momentum was calculated using the track insertion method. For the multiplicity dependence a track from real data was inserted into a real event with known multiplicity and the efficiency for finding that track was determined (Fig. 17). Similarly, the momentum dependence of the tracking efficiency was determined by inserting a simulated track with a known momentum into real data. From these plots one concludes that the TEC efficiency is strongly dependent of track multiplicity but has little dependence on momentum except below 400 MeV/c.

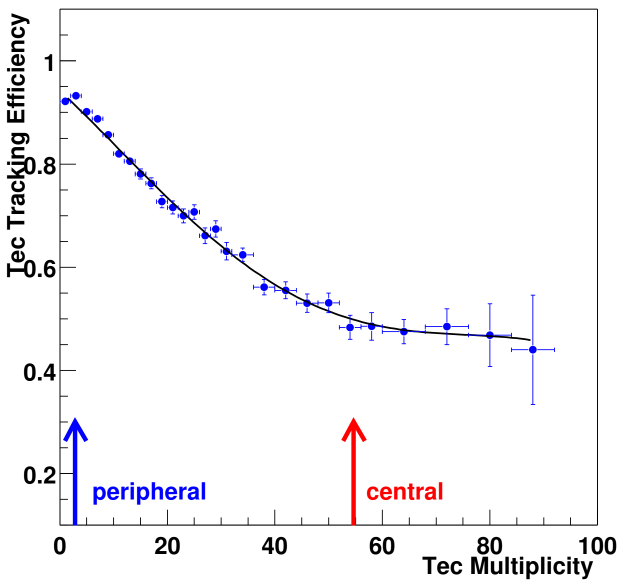

Fig. 17. Efficiency of TEC track reconstruction vs event multiplicity determined by inserting single tracks into real data and calculating reconstruction efficiency for those tracks.

In a thin medium such as a gas a particle's dE/dx behaves approximately as $1/\beta^2$ when it is non-relativistic and then slowly rises as a function of β until it plateaus at large γ. Since the TEC measures both a particles momentum and energy loss one can use the TEC to identify particle species over a certain momentum range. Energy loss distributions in a thin medium have a large high-side tail which requires employing a truncated mean technique on the TEC dE/dx data. TEC prototype studies in a test beam indicated that truncation levels of 50-60% allowed for clear separations of electrons and pions at 0.5 GeV/c (Fig. 18)[16]. A similar analysis was performed on the year-1 RHIC data using the TEC.

4.4 Time Expansion Chamber Summary

The PHENIX TEC, a set of large multi-wire tracking chambers, has been installed, commissioned and operated in the PHENIX Central Arm Spectrometer during the first RHIC data run. The detector has been used for pattern recognition and momentum reconstruction on our current data set. The custom electronics work to specification with an average noise per channel under 2 fC, when the full system is operated. A combination of data and simulations has been used to measure both the TEC position resolution and its tracking efficiency versus multiplicity and momentum. The TEC position resolution is 380 μm which should be improved by increasing the chamber gain. The TEC

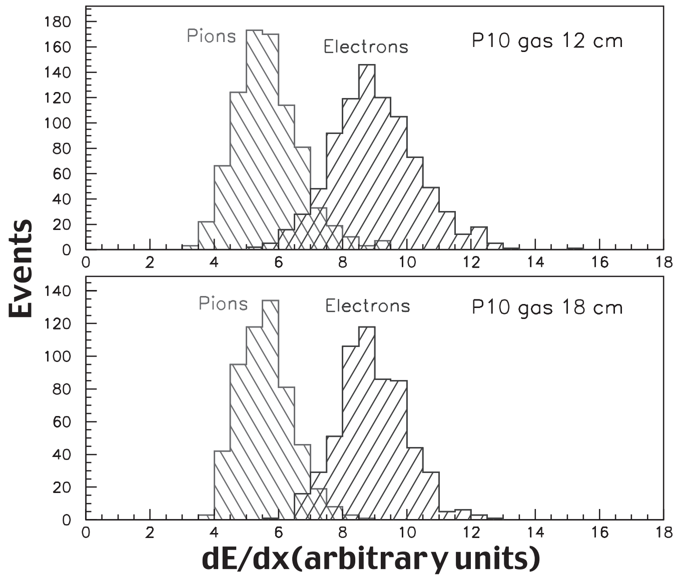

Fig. 18. TEC truncated mean charge distributions for electrons and pions measured with test beam data. Electron/pion separation for both 4-planes(12 cm) and 6-planes(18 cm) of the TEC are shown.

tracking efficiency has a strong dependence with track multiplicity, and is flat with respect to p_T above 400 MeV/c.

5 Acknowledgements

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