Current Status of the SVD DAQ System

Y. Tsujita
Institute of Applied Physics,
University of Tsukuba

1 Overview of the SVD DAQ System

For the BELLE silicon vertex detector (SVD) system, a basic unit is four double sided silicon detectors which are connected in daisy-chain. At each side of the unit, a hybrid board, which contains five VA1 preamplifier chips, is attached for the readout. We must manage 82,000 readout channels in the whole SVD system.

We have 128 hybrids. They are eventually connected to flash ADC (FADC) modules (See [1].). We will install FADCs in total four crates, each of which is called FADC crate. One FADC crate accepts input from 32 hybrids. Because an FADC module has four readout channels, number of the FADCs per one crate is eight (32/4).

We use SHARC VME modules (WS2126) [2] supplied from Wiese, Germany, for the VME master in each FADC crate. SHARC [3] is a DSP supplied from Analog Devices.

Besides the SHARC module, A MVME-162 modules with VxWorks real-time OS is used in each crate for run control [4]. With NSMLIB developed by CDAQ people, we can manage run control within an FADC crate.

2 Buffer Manager

To average data transfer rate between FADC modules and central DAQ interface board (CEBTX), we develop a buffer manager program on WS2126 and MVME162 with VxWorks.

In buffer manager program, two processes, *producer* and *consumer* run concurrently with semaphore method. Tasks of each process are as follows.

producer Gathers data from FADC modules and stores them in heap memory region.

consumer Data in the heap region are transfered to another region which CDAQ can read.

Buffer manager program must run under a rate of 500 Hz or more. Design of buffer manager program is as follows.

- Ring buffer system is used for heap memory region.
- Semaphore method is used to protect the heap region. Overwriting of data in heap region will be restricted by this method.

3 Data Size Estimation

The average transfer rate was estimated by Monte-Carlo simulation. In the BELLE SVD system, we have 64 double sided hybrids. An input of each side of a hybrid is connected to one channel of an FADC module. In convenience, we may name one side of hybrid "one side". Thus we have 128 sides of hybrids. Total strip number is 640 $\times$ 128 $\simeq$ 82,000.

Number of sides of hybrids in one FADC crate is 128/4 = 32, where 4 is the number of FADC crates which we use. As one FADC module has four channels, number of FADC modules is 32/4 = 8.

One side of hybrid has 640 readout strips, then strip number per FADC module is 4 $\times$ 640 = 2,560. One FADC crate has 8 FADC modules, then strip number per FADC crate is 8 $\times$ 2,560 = 20,480.

According to Monte-Carlo simulation [5], occupancy of the SVD is as follows. In this estimation, It is assumed that one hit cluster includes data from the hit strip and four neighboring strips.

Case 0. : Nominal case	
Event rate	500 Hz
Occupancy	2.4 %
Case 1. : $B\overline{B}$ + beam background + electric noise	
Event rate	100 Hz
Occupancy	2.4 %
Case 2. : beam background triggered beam background + electric noise	
Event rate	400 Hz
Occupancy	6.2 %

In case 0 (nominal case), hit strip number per one FADC crate is as follows.

$$20,480 \times 0.024 \simeq 492$$

If we assume that data size per strip is 3 Bytes, then data size per FADC crate is

$$492 \times 3 = 1.476 \text{ KBytes.}$$

Event rate is 500 Hz, then transfer rate per one FADC crate is

$$1.476 \times 500 \text{ (Hz)} = 0.738 \text{ MBytes/s.}$$

In case 1 and case 2, data transfer rate is calculated as follows.

$$0.738 \times \left\{ \begin{array}{l} 100 \text{ (Hz)}/500 \text{ (Hz)} \times 2.4 \text{ (\%)}/2.4 \text{ (\%)} \\ 400 \text{ (Hz)}/500 \text{ (Hz)} \times 6.2 \text{ (\%)}/2.4 \text{ (\%)} \end{array} \right\} \simeq \left\{ \begin{array}{ll} 0.148 & \text{(case 1)} \\ 1.525 & \text{(case 2)} \end{array} \right\} \text{Mbytes/s}$$

4 Summary

- We are designing and developing buffer manager program for WS2126 and MVME-162 with VxWorks.

- Semaphore method would be an important method for buffer manager program.
- Download program for SHARC DSPs is being developed now.
- DMA control on SHARC DSP is a powerful method for data handling in global run mode.
- We can expect that this DSP will run in more than 500 Hz data transfer rate.
- Run control program with VxWorks and NSMLIB is under construction.

References

[1] J. S. Lange, *"New SVD Backend Electronics"*, Proceedings for '97 BELLE Trigger/DAQ Workshop.

[2] Wiese Signalverarbeitung GmbH, *"WS2126 VME SHARC Cluster"*, Version 1.1 (1997).

[3] Analog Devices, *"ADSP-2106x SHARC User's Manual"*, First Edition (1995).

[4] C. Fukunaga, *"New SVD Run Control"*, Proceedings for '97 BELLE Trigger/DAQ Workshop.

[5] A. Bozek, SVD video conference 97/10/27.