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In this issue:

Beginning Oct. 1, 1999 the EEE Links will be published by the NASA Electronic Parts and Packaging (NEPP) Program. Look for more details about the NEPP Program in the next issue of EEE Links.

Different Approaches for Ensuring Performance/Reliability of Plastic Encapsulated Microcircuits (PEMs) in Space Applications June 17, 1999

Editor: **Robert Humphrey, (301) 731-8625**
rhumphre@pop300.gsfc.nasa.gov
Mailing List Information and Article Submissions: (301) 731-8625
Desk Top Publisher: **Esther Bailey**
Published by the NASA/GSFC Electrical Systems Center
Component Technologies and Radiation Effects Branch, Code 562
Branch Head: **Darryl Lakins**

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Letter from the Editor

Robert Humphrey
Editor of EEE Links
(301) 731-8625
rhumphre@pop300.gsfc.nasa.gov

Welcome to the October issue of EEE Links. Keeping up with the latest technology advances has always been an extraordinary challenge. Remember EEE Links is your vehicle for sharing practical experiences and discoveries.

Please keep us informed with your questions and needs so we can continue to improve the upcoming issues to meet your needs.

Different Approaches for Ensuring Performance/Reliability of Plastic Encapsulated Microcircuits (PEMs) in Space Applications June 17, 1999

R. David Gerke, Mike Sandor, Shri Agarwal
California Institute of Technology
Jet Propulsion Laboratory (JPL)
Pasadena, CA
Andrew F. Moor, Kim A. Cooper
The Johns Hopkins University
Applied Physics Laboratory (APL)
Laurel, MD

ABSTRACT

Engineers within the commercial and aerospace industries are using trade-off and risk analysis to aid in reducing spacecraft system cost while increasing performance and maintaining high reliability. In many cases, Commercial Off-The-Shelf (COTS) components, which include Plastic Encapsulated Microcircuits (PEMs), are candidate packaging technologies for spacecrafts due to their lower cost, lower weight and enhanced functionality. Establishing and implementing a parts program that effectively and reliably makes use of these potentially less reliable, but state-of-the-art devices, has become a significant portion of the job for the parts engineer.

Assembling a reliable high performance electronic system, which includes COTS components, requires that the end user assume a risk. To minimize the risk involved, companies have developed methodologies by which they use accelerated stress testing to assess the product and reduce the risk involved to the total system. Currently, there are no industry standard procedures for accomplishing this risk mitigation. This paper will present the approaches for reducing the risk of using PEMs devices in space flight systems as developed by two independent Laboratories. The JPL procedure primarily involves a tailored screening with accelerated stress philosophy while the APL procedure is primarily a lot qualification procedure. Both Laboratories successfully have reduced the risk of using the particular devices for their respective systems and mission requirements.

For a copy of the entire paper please contact by Email: michael.a.sandor@jpl.nasa.gov

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Military Qualifications Working Group – First Meeting

Michael Sampson
NASA Goddard Space Flight Center
Michael.J.Sampson.1@gsfc.nasa.gov
(301) 286-8838

The first meeting of the Qualifications Working Group was held on August 24, 1999 in the offices of the Logistics Management Institute in McLean, Virginia. The Group consists of around 20 people representing the military services and other branches of the Department of Defense. NASA was the only non-military entity represented. The Group's Charter, as defined by Gregory Saunders, Director of the Defense Logistics Support Command, Logistics Management and the Group's sponsor, is to consider the process of qualification to supply products to the US military from a completely clean slate. The objective is to define a process that will provide the military (and NASA) the material to meet their needs far into the next century. To meet this objective it will be necessary to create an environment that is attractive both to the commercial supplier and the government customer in a world of rapid change and a fiscal conservatism. Perhaps it will be sufficient to "tweak" the existing system, removing some unnecessary elements or providing additional options to reduce time delays and eliminate inefficiencies. Or it could be that qualification is seen to have outlived its usefulness and the Group could recommend eliminating qualification as an element in government procurement. Or any option in between, whatever makes the best sense

for the future. The Group is due to deliver its report in six months.

The first meeting was for introductions of Group members and basic concepts. The Group includes a wide array of viewpoints in addition to electronics and encompasses most of the breadth of military procurement. This is about qualifying products ranging from metal sheets and hydraulic valves to complex microcircuits. There were two presentations at this meeting; others representing a spectrum of viewpoints on the subject are planned for the future. The second objective is to understand current processes and to explore other models drawn from as many sources as can be identified, will agree to participate and can be accommodated by the Group.

The initial presentations were by the Defense Supply Center Columbus (DSCC) and the Defense Supply Center Philadelphia (DSCP). The DSCC representative, Darryl Hill provided an excellent overview of the familiar Qualified Manufacturer's List (QML) and Qualified Products List (QPL) concepts. The emphasis of the DSCC presentation was on the qualification of electronic parts. The QPL process was the first method of qualification and is still the most widely used. QML is a recent development that is currently only applied to discrete semiconductors (MIL-PRF-19500) microcircuits (MIL-PRF-38535) and hybrids (MIL-PRF-38534). The QPL lists the characteristics of the product for which a manufacturer is qualified; in QML it is the manufacturer's ability to dependably produce products in a defined technological capability range that is qualified. The DSCP representatives Gene Maisano and Al Capiella, explained the Qualified Sources List (QSL) concept that is currently only employed for products procured through this location. These products are primarily metal sheeting and mechanical fasteners. This is another innovative approach to cope with a broad range of products, and has general features that are similar to QML. A major difference between QML and QSL is that QSL does not include specific technical performance requirements, the technical requirements are provided by separate specifications, some of which may have their own QPL's. To be granted listing on a QSL, the manufacturer must pass an audit of their basic manufacturing, quality assurance and process control methodologies, with an emphasis on the effective use of statistics. It is not clear if this concept could be effectively applied to other types of commodities, especially electronic parts.

It was clear from the discussions that the QPL / QML situation for electronic parts is much better than for many other commodities. In these commodities, QPL's are not being revised and in some cases, all the sources listed on a QPL may have dropped their qualification or gone out of business years ago.

Presentations for future meetings are planned to include third party qualification representatives, prime contractors and commodity manufacturers. Other parties will be included as required to meet the needs of the Working Group.

Call for Papers
2nd Annual Microelectronics Reliability and Qualification Workshop
October 26-27, 1999
Pasadena Convention Center
Pasadena, California

Sponsored By:
Jet Propulsion Laboratory
Sandia National Laboratory
Applied Physics Laboratory
Aerospace Corporation
Air Force Research Laboratory
Components, Packaging, and
Manufacturing Society of IEEE

The 2nd annual Microelectronics Reliability and Qualification Workshop will be held October 26-27, 1999 in the Pasadena Convention Center in Pasadena, California. The purpose of the workshop is to provide a forum for open discussion in all areas of microelectronics reliability and qualification for high reliability and commercial applications in the form of oral presentations and panel discussions. Papers presenting the latest results in microelectronics device reliability and qualification methodologies or work in progress are solicited. General topics of interest include (but are not limited to):

- Accelerated Testing
- ASICS
- Compound Semiconductors
- COTS
- Design of Experiment

- Environmental Studies
- Failure Mechanisms
- Test and Verification
- Low Temperature Applications
- Low Power Applications
- Materials Issues
- Memories
- MEMS Structures
- Microprocessors
- Mixed Signal Devices
- Optoelectronics
- Passive Components
- Power Converters
- Process Verification
- Production and Yield Enhancement
- Qualification
- Reliability Assurance Practices
- Radiation Effects
- Reliability Modeling
- Thermal & Dynamic Analysis
- Up-screening

PAPER SUBMISSION:

Prospective authors are requested to submit an abstract of approximately 100 words. The abstract must include the author's name, affiliation, complete address, telephone and FAX number, and be suitable for a 20-minute presentation. The abstract must state: (1) the purpose of the work and what problems and questions are being addressed, (2) the results or conclusion of the work, and (3) how the work advances the knowledge of microelectronics reliability or qualification. Authors are responsible for obtaining all required company and government clearances prior to submission. Entries must be received by **August 27, 1999**.

REGISTRATION:

Registration fee is $120 ($160 after Oct. 11), which includes dinner reception and workshop proceedings.

For paper submission, registration and further information, contact:

Jing Yuan, Publicity and Registration Chair
Tel: (818) 354-5787 Fax(818) 393-4559
Email: jing.yuan@jpl.nasa.gov
http://parts.jpl.nasa.gov/workshop/home.htm

1999 MAPLD International Conference

September 28-30, 1999
Kossiakoff Conference Center
JHU Applied Physics Laboratory
Laurel, Maryland

The 2nd annual Military and Aerospace Applications of Programmable Devices and Technologies International Conference will address devices, technologies, usage, reliability, fault tolerance, radiation susceptibility, and applications of programmable devices and adaptive computing systems in military and aerospace systems. The program will consist of approximately 60 oral and poster technical presentations and close to 20 industrial exhibits. This international conference is open to US and foreign participation and is unclassified. There will be one classified session at the secret level, for U.S. citizens only. For additional conference information, please see the Programmable Technologies Web Site (http://rk.gsfc.nasa.gov).

MAPLD '99 PROGRAM

WELCOME

Rich Katz - NASA Goddard Space Flight Center
Stamatios Krimigis - JHU/Applied Physics Lab

TECHNICAL SESSIONS:

A. Military & Aerospace Applications
Session Chair: Marty Fraeman - JHU/APL
Invited Speaker: Dr. Ralph McNutt - JHU/APL
Space Exploration Beyond 2020

B. Devices, Elements, and Technologies
Session Chair: Rich Katz - NASA GSFC
Invited Speaker: John McCollum - Actel Corp.
Programmable Elements and Their Impact on FPGA Architecture, Performance and Radiation Hardness

C. Radiation Environments and Effects
Session Chair: Ken LaBel - NASA GSFC
Invited Speaker: Rich Katz - NASA GSFC
FPGAs in Space Environment and Design Techniques

D. SoC, Synthesis, and IP
Session Chair: Hans Tiggeler - University of Surrey
Invited Speaker: Sandi Habinc - ESA
Designing Space Applications Using Synthesizable Cores

E. Adaptive Computing

Session Chair: John McHenry - NSA
Invited Speaker: Brad Hutchings - BYU
Configurable Computing: Past, Present, and Future

F. Classified Session

Session Chair: Al Hunsberger - NSA
Invited Speaker: Mark Dunham - DOE/LANL
Gigasample Image and Signal Processing via Reconfigurable Computing

P. Poster Session

Session Chair: Christina Gorsky - SGT, Inc.

Dinner Speaker (Tuesday Evening)

Dr. Don DeVoe, University of Maryland
Micro Electro Mechanical Systems (MEMS)

Panel Session: (Wednesday Evening)

Architecture, Technologies and Design Methodologies for 2005 and Beyond
Panel Moderator: Ann Garrison Darrin - JHU/APL

THE CONFERENCE IS SPONSORED BY:

NASA Goddard Space Flight Center
JHU/Applied Physics Laboratory
National Security Agency
NASA Radiation Effects Program
Military & Aerospace Programmable Logic Users Group
American Institute of Aeronautics and Astronautics

For more information about the conference or submission of late news papers see http://rk.gsfc.nasa.gov or contact:

Richard Katz
NASA
rich.katz@gsfc.nasa.gov
Tel: (301) 286-9705

Alan W. Hunsberger
NSA
awhunsb@afterlife.ncsc.mil
Tel: (301) 688-0245

Ann Garrison Darrin
JHU/APL
ann.darrin@jhuapl.edu
Tel: (240) 228-4952

Programmable Logic Application Notes

Richard Katz
Microelectronics and Signal Processing Branch
NASA Goddard Space Flight Center
301-286-9705
rich.katz@gsfc.nasa.gov

This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter the focus is on some experimental data on low voltage drop out regulators to support mixed 5 and 3.3 volt systems. A discussion of the Small Explorer WIRE spacecraft will also be given. Lastly, we take a first look at robust state machines in VHDL and their use in critical systems. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or e-mail.

1999 MAPLD Conference

September 28-30, 1999
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Laurel, Maryland

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1999 IEEE NSREC and RADECS Papers

A number of papers were given on programmable devices at the July 1999 IEEE Nuclear and Space Radiation Effects Conference (NSREC). Other programmable-related papers will be given at the 1999 RADECS conference during September 1999. This section will list the titles and first author infor-

mation for each of these articles. E-mail addresses for NSREC first-authors may be found at:

http://www.nsrec.com/email.htm

Single Event Upset Immunity of Strontium Bismuth Tantalate Ferroelectric Memories, J.M. Benedetto.

The Impact of Software and CAE Tools on SEU in Field Programmable Gate Arrays, R.B. Katz.

Design Guidelines for COTS in Military and Space Systems, P.S. Winokur.

Reprogrammable FPGA for Space Applications, J-J. Wang.

*The Effects of Architecture and Process on the Hardness of Programmable Technol*ogies, R.B. Katz.

Radiation Effects on Advanced Flash Memories, D.N. Nguyen.

SEU and Microdose Measurement Based on FAMOS Transistors, P.J. McNulty.

Total Ionizing Dose Effects in SRAM-Based FPGAs, B.G. Henson.

Total Dose and Dose-rate Effects on Start-up Current in Antifuse FPGA, J. J. Wang. (RADECS)

Total Ionizing Effects in a SRAM-based FPGA, D.M. Gingrich (RADECS).

WHAT'S NEW?

A large amount of data, reports, papers, application notes, and conference information is being stored on our companion Programmables Technology www site, http://rk.gsfc.nasa.gov. In order to make it easier to keep readers up to date, all new additions to the site are being listed in chronological order on our "What's New" page. This can be found at: http://rk.gsfc.nasa.gov/What's_New.htm

The site has some new areas including conference information, low voltage dropout regulators, and ferroelectric memories (FRAMs) on the memories page.

Wide Field Infrared Explorer (WIRE)

WIRE was a Small Explorer (SMEX) spacecraft which unfortunately had a failure after launch which prevented the spacecraft from meeting any of its science objectives. A programmable device was at the center of this mishap and has been the subject of much discussion. We will present here the failure review board's Executive summary along with some technical discussion about the failure. The main section of the Board's report is at: http://rk.gsfc.nasa.gov/richcontent/Reports/wiremishap.htm. Appendix F, which provides the analysis of the failure mechanism, is on-line at: http://rk.gsfc.nasa.gov/richcontent/Reports/WIRE_Report.PDF.

Executive Summary

The Wide-Field Infrared Explorer Mission objective was to conduct a deep infrared, extra galactic science survey. The Wide-Field Infrared Explorer was launched on March 4, 1999, and was observed to be initially tumbling at a rate higher than expected during its initial pass over the Poker Flat, Alaska, ground station. After significant recovery efforts, WIRE was declared a loss on March 8, 1999.

The WIRE Mishap Review Board has determined that the telescope instrument cover was ejected earlier than planned and at approximately the time the WIRE pyro electronics box was first powered on. The instrument's solid hydrogen cryogen supply started to sublimate faster than planned, causing the spacecraft to spin up to a rate of sixty revolutions per minute over the twelve hours following the opening of the secondary cryogen vent. Without any solid hydrogen remaining, the instrument could not perform its observations.

The root cause of the WIRE mission loss is a digital logic design error in the instrument pyro electronics box. The transient performance of components was not adequately considered in the box design. The failure was caused by two distinct mechanisms that, either singly or in concert, result in inadvertent pyrotechnic device firing during the initial pyro electronics box power-up. The control logic design utilized a synchronous reset to force the logic into a safe state. However, the start-up time of the Vectron crystal clock oscillator was not taken into consideration, leaving the circuit in a non-deterministic state for a time sufficient for pyrotechnic actuation. Likewise, the startup characteristics of the Actel A1020 FPGA were not considered. These devices are not guaranteed to follow their "truth table" until an internal charge pump "starts" the part. These uncontrolled outputs

were not blocked from the pyrotechnic devices' driver circuitry. There has been no evidence or indication of any component failure although component failures were considered in the investigation.

A significant contributing cause of the anomaly was the failure to identify, understand, and correct the electronic design of the pyro electronics box. Design errors in the circuitry, which controlled pyro functions, were not identified. The pyro electronics box design was not peer reviewed, and other system reviews conducted by the instrument design organization did not focus on the electronics box. At the time the Systems Design Review was conducted for WIRE the design of the pyro electronics box was not completed. It is the assessment of the WIRE Mishap Investigation Board that a peer review held during the design process, by people with knowledge of and expertise regarding pyro circuit design would have identified the turn-on characteristics that led to failure.

A large number of failure scenarios were evaluated during the investigation to determine the cause of the cover ejection. These included; pre-launch, launch, powered flight, separation, software, operations, design and component reliability faults. Based on comprehensive, systematic review of data, it was determined the cover was most likely ejected at the time the WIRE pyro electronics box was turned on due to a transient condition that exists in the pyro electronics during startup. This transient condition is the direct result of the non-deterministic initialization of a Field-Programmable Gate Array (FPGA) that controls both the arming and firing circuits in the pyro electronics.

Although some design attention was given to the startup behavior of the FPGA, the design contained unidentified idiosyncrasies that triggered the cover ejection. The system design did not contain sufficient start-up lockout protection or independent provisions to prevent the FPGA startup operation from propagating to the firing circuits.

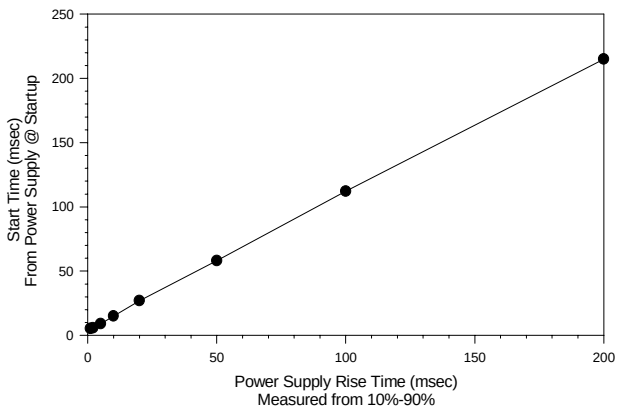
The anomalous characteristics of the pyro electronics unit were not detected during subsystem or system functional testing due to the limited fidelity and detection capabilities of the electrical ground support equipment. Post-flight circuit analyses conducted as part of the failure investigation have predicted the existence of the anomaly and it has been reproduced confidently using engineering model hardware.

Some Technical Details

This section will cover some of the key factors surrounding this failure and discuss the principles behind them. These issues are relatively common, some of which have been discussed here previously. As a result of this investigation, a new application note has been written along with a NASA Parts Advisory. These may be found at the following url's: http://rk.gsfc.nasa.gov/richcontent/General_Application_Notes/StartupNote.pdf and http://rk.gsfc.nasa.gov/maplug/Notices/NASA_Advisory_046_ActelStartup.pdf

The design implemented in the FPGA utilized a synchronous reset circuit. If one would assume a random state of all flip-flops during the power-on period, then the circuitry would have a 1 of 4 chance of failing catastrophically, in the WIRE configuration. This idealized model applies here since the synchronous reset relies on a rising clock edge to put the FPGA's circuits into the reset condition. However, real crystal clock oscillators do not start instantaneously and have a startup delay that can last for tens of milliseconds or more, depending on the oscillator design, the frequency of the crystal, and other factors. One key "other" factor in the WIRE mishap was the rise time of the power supply. The figure below shows the start time characteristic of a WIRE flight spare oscillator as a function of power supply rise time. For these tests I used a linear ramp for the power supply.

Summary of start time characteristics of a flight spare oscillator at 10°C. Start time is a linear function of power supply rise time using a ramp generator as the power supply.



Note the linear relationship between oscillator startup time and power supply rise time. The time measured here is from the power supply startup until the first edge output from the oscillator. It took additional time for the oscillator to stabilize. These 200 kHz oscillators would either put out pulses of incorrect width or drop pulses until the device stabilized. Clearly, care must be taken in any logic design with respect to the reset topology. Normally an asynchronous clear would be applied with a synchronous removal; this would ensure a quick reset function with synchronous removal to prevent metastable states in sequencers.

Using the idealized model mentioned above of a random flip-flop power-on state, we could then hope to see some evidence of failure if the circuit was tested enough times. This does not necessarily apply and the philosophy of "testing in reliability" is again shown to be false. The power-on state of flip-flops, which are not guaranteed to be in any particular state, were shown to be clearly not random.

In particular, it was shown that in repeated power-on trials, flip-flops in the FPGAs (A1020, A1020B) would consistently power-up in the same state, for stable "conditions." This was demonstrated both on the lab bench and indirectly shown on the WIRE Pyro box engineering model in an effort to replicate the failure. Bench testing showed that the flip-flop's initial state was also a function of power supply rise time. The mechanism here is the circuit design inside of the FPGA, the effect of asymmetrical load capacitances, and other uncontrolled parameters. After numerous (> 30) trials getting identical results with a power supply rise time of about 1 µs, a very slow rise time was used and the flip-flops powered on in the opposite state.

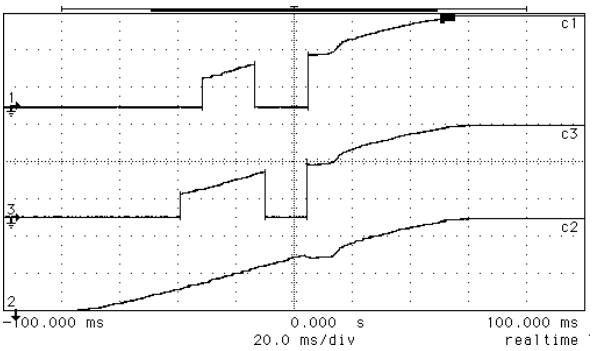
Another factor involved in FPGA flip-flop initial state determination for WIRE was the amount of time the flip-flop has been powered off. In this part of the study it was shown, as mentioned above, that repeated trials yielded unchanging results. However, after letting the circuit sit unbiased for an extended period of time, hours, the flip-flops would many times power up in the "opposite" state for just one power-on cycle.

A related case was engineering model testing of GLAS instrument electronics. Here a "working circuit" suddenly ceased to function when the +5V power supply was changed. In this case A14100A devices were used. Analysis showed that the change in the power supply's startup condition changed the power-on state of flip-flops. Based on the symptoms of the failure, it was suspected that the flip-flops which perform the "control function" of the FPGA were not being properly cleared. The MODE pin was tied to +5VDC and the change of the power supply resulted in a change of the power-on state of the flip-flops. This is a good reminder for users of Act 1,2,3,XL, and DX technology parts to always verify that the MODE pin is properly biased to ground during startup. If the Actionprobe is used, it will drive MODE high at the appropriate time. For SX devices which have IEEE 1149.1 test circuits, "Revision 0" parts must have an independent clock drive TCLK with TMS high. For revision 1 parts the TRST* pin should be biased at ground.

Another characteristic of the A1020 FPGA used in the WIRE Pyro Box circuitry was that the outputs of the device were direct inputs to the relay and FET drivers. There was no circuitry utilized to block the outputs of the FPGA during the power-on interval. While not inherently the case, many programmable devices, not just Actels or A1020's, have outputs that are not controlled while the device is powering up or initializing. Each device must be analyzed on a case by case basis. It is noted that some future SX devices, currently in design, will have outputs that are "power-up friendly." The drivers will come up in a tri-state condition and resistors, programmed in either a pull-up or pull-down configuration, will hold the output pin at the appropriate logic level until the device is powered up and stabilized.

Again, testing has shown that a device can not easily be "characterized" for start-up transient performance. Like flip-flop power-on state, the size of the transient, including whether one is seen at all, is a factor of the power supply rise time and the amount of time the device has been powered off. According to Actel documentation, it is also a factor of device temperature. For design/analysis purposes, it should be assumed that an unpredictable transient will occur and that the device powers up with uncontrolled I/O's (except for devices especially designed for safe power-on). As a result, logic that blocks the outputs

of the programmable device should be used, in conjunction with a power-on-reset circuit, to ensure that critical signals are under control. Similarly, it should be assumed that device inputs may behave temporarily as outputs. This effects circuits such as power-on-reset circuits where an input may source current during the transient, affecting the amount of time that the reset is active for. The figure below shows the transient response of a flight spare A1020 from the Small Explorer WIRE project.



Output transient on start-up of WIRE flight spare S/N 001 A1020 FPGA observed after 24 hours powered off. The bottom trace is V_{CC} while the top two traces are the ARM and FIRE signals. All signals are at 2 volts/division. Attempts to immediately repeat the transient failed, with both critical outputs, Cover and Arm, maintaining logic low output levels with no glitches detected. The probability of a transient is a function of the rise time of the power supply and the amount of time the device has been off, as a result of a "memory effect". The duration of the transient is also a function of the rise time of the power supply. Results on flight spare S/N 002 as well as 3 non-flight A1020B's and another A1020 were similar. Vertical scale is 2V per division. Horizontal scale is 20 ms per division. Note that under these conditions, both outputs were latched in the logic '1' state.

Low Voltage Dropout (LVDO) Regulators

With the move to mixed-voltage systems, the need for low voltage dropout regulators is increasing. The two devices selected for initial test offer the capability of powering small (LM2931CT) or moderate (LM1117T-3.3) loads. Commercial samples were obtained with both models procured in plastic packages. The devices were subjected to TID testing in a Cobalt-60 cell, proton testing at UC Davis, and for the LM1117T-3.3 only, heavy ion tests. The LM2931CT was not tested for heavy ion SEE because of trouble decapping the samples.

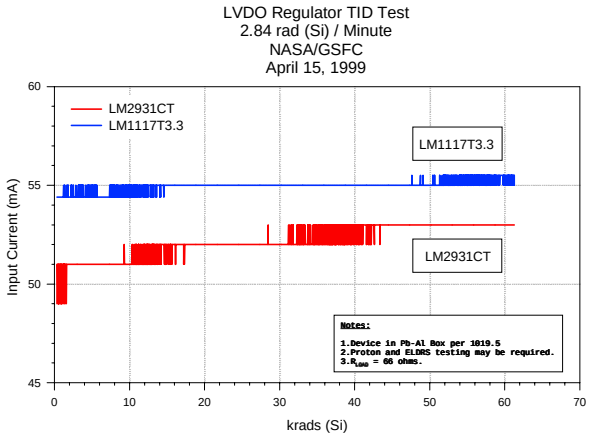
The bias and load circuits for these devices are not reproduced here. They are available for download from the internet in .pdf format from: http://rk.gsfc.nasa.gov/richcontent/LVDO_Regulators/Run1_LM2931_LM1117/regulator_3volt.PDF

Cobalt-60 Test

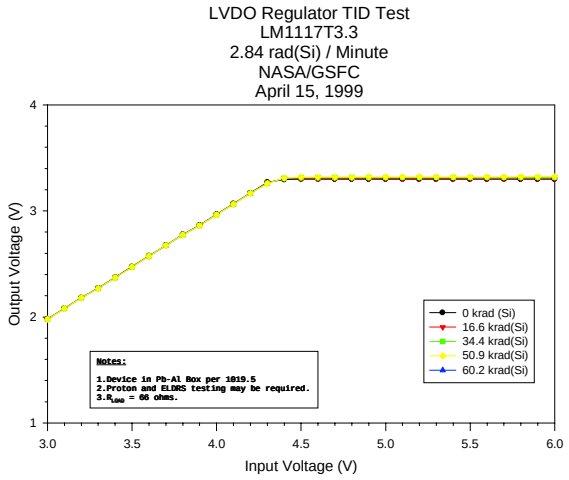
One device of each type was irradiated at 2.84 rad(Si)/sec. In situ monitoring of the current was performed and each device was biased with a 66 Ω load resistor. Additionally, at periodic intervals, the input voltage was swept and the outputs measured. This permits determination of the device's transfer function and dropout voltage without disturbing the devices under test.

Testing of the devices continued until just over 60 krad(Si) was reached with only minimal changes in the devices' parameters and no failures observed. The test was terminated because of facility availability limitations. Future testing will be done at a higher dose rate.

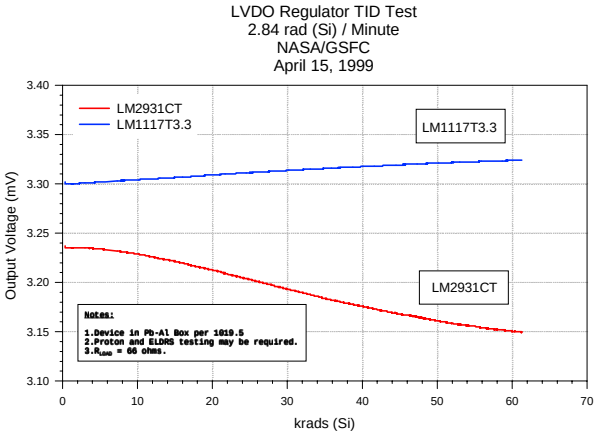
The figure below shows the change in input current over the course of the testing. As can be seen, only small changes were observed. Approximately 50 mA of the current displayed on the graph is from the load on the regulators' 3.3 VDC output.

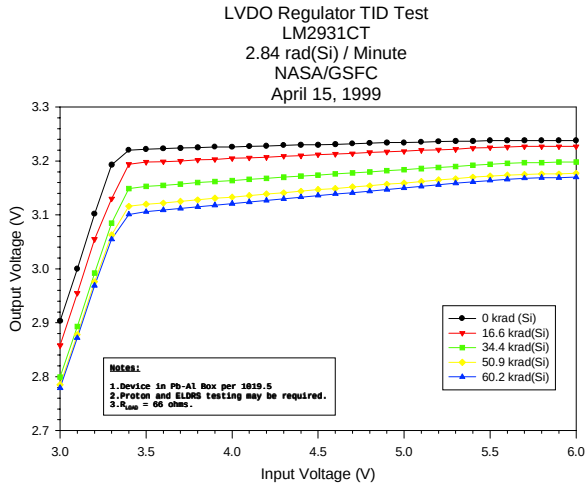


Similarly, only small changes in output voltage were recorded for each of the devices. In this case, the LM1117T-3.3 did considerably better, showing significantly less than a 50 mV change over the 60+ krad(Si) exposure.



As described earlier, in situ transfer functions were obtained during the irradiation. The data shows that adequate margin exists for this room temperature evaluation for regulation at 3.3 VDC.





Proton Test

The LM1117T-3.3 and the LM2931CT were subjected to proton tests. Two LM1117T and three LM2931CT devices were irradiated with 63 MeV protons. The input voltage for all runs was 5V and output voltages were approximately 3.3 VDC. The initial output voltage of the LM2931CT is adjustable and is set by trim resistors; the LM1117-3.3 comes trimmed to 3.3 VDC. All tests were done at room temperature and annealing effects were not measured.

The chart below summarizes the proton test data (courtesy of Dr. Robert Reed, NASA Goddard Space Flight Center). No significant radiation effects were observed. The following notation is used for the chart:

I_0 Initial input current
I_F Input current after irradiation
OUT_0 Initial output voltage
OUT_F Output voltage after irradiation

Device	S/N	I_0* mA	I_F* mA	Out_0 V	Out_F V	Dose krad Si
LM1117T	1	55	55	3.31	3.32	150k
LM1117T	2	55	55	3.31	3.31	150k
LM2931CT	1	49	50	3.18	3.19	50k
LM2931CT	2	49	51	3.18	3.20	100k
LM2931CT	3	50	51	3.21	3.17	150k

* Current includes driving a DC load of 66 Ω.

Heavy Ion SEE Test

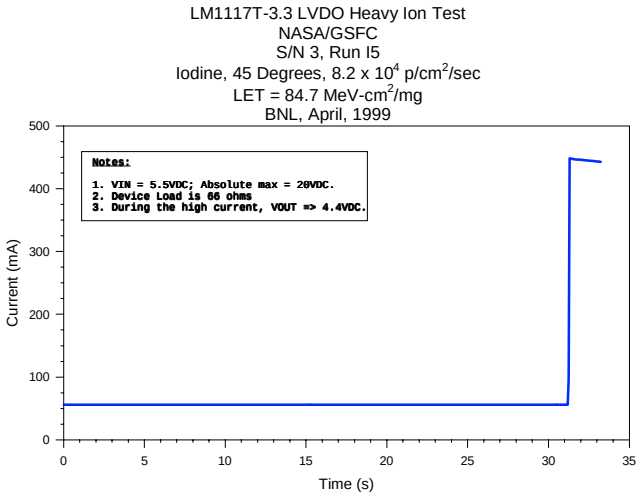
Three LM1117T-3.3 low-voltage dropout (LVDO) linear regulators were tested with heavy ions at Brookhaven National Labs in April, 1999. The units were procured as commercial parts in plastic packages. This device has a dropout voltage of 1.2V @ I=800 mA, making it suitable for producing a 3.3VDC supply from a "standard" 5V logic supply. Most runs were made with a worst-case max logic supply of Vin = 5.5VDC, although the device, as specified on the data sheet is capable of tolerating higher input voltages. Some runs were made with a worst-case min logic supply of Vin = 4.5VDC.

The devices all showed fluctuations in regulated output voltages during the runs. Start and end values are listed in the table on our www site. It is noted that the

changes are small and negligible for standard logic circuits.

All three devices passed at Vin = 5.5VDC with Iodine, normal incidence; this is an LET of 59.9 MeV-cm^2/mg. All three devices went into a "latchup-like" state at either 30 degrees (LET of 69.1 MeV-cm^2/mg) or at 45 degrees (LET of 84.7 MeV-cm^2/mg). In this mode, the input current increased by about 400 mA and the output went from 3.3 VDC to approximately 4.4 VDC, until power was removed. S/N LV1 was destroyed.

A typical strip chart of current during a heavy ion irradiation, when the device enters its high current mode is shown in the figure below.



Detailed test heavy ion SEE data can be viewed on-line at:
http://rk.gsfc.nasa.gov/richcontent/LVDO_Regulators/BNL0499/LM1117T-3.3_BNL0499.htm

NASA Lessons Learned

The Lessons Learned Information System (LLIS) is a NASA-wide lessons learned repository. The LLIS offers search capabilities to permit various searches (e.g., NASA Center, date, Project, search string, etc.). Additional categorization capability is under evaluation for future implementation by the LLIS Steering Committee. The NASA Lessons Learned url link, http://llis.nasa.gov/, will take you directly to the LLIS Home Page. The Recently Submitted Lessons url link, http://llis.nasa.gov/llis/new_lessons.html, will take you directly to a list of LLIS lessons in time descending order allowing easy access to view the most recently approved lessons.

Is It Safe?

This section will discuss some of the issues involved with designing robust finite state machines (FSMs) in VHDL and some recent developments in a VHDL synthesizer. Additional information can be found in *The Impact of Software and CAE Tools on SEU in Field Programmable Gate Arrays*, to be published in the IEEE Transactions on Nuclear Science, December 1999. Example input and synthesized outputs will be given along with a discussion of the results in the next edition. Time limitations prevent this from being completed here with the proper checking and verification.

Sequencer design can be broken down into several stages. There is the logical design that results in a finite state machine (FSM) which implements the desired function. At this stage logical names are used for each state. In a VHDL implementation, a separate enumerated type is often used, making the code very readable and easily maintainable. A structure of the state machine is then selected. VHDL synthesizers often provide, independent of the HDL code, several options. There are many forms, but a simple register with feedback is commonly used, with the combinational logic providing the next state signals to the state register. The sequence of states is encoded using one of several methods such as a sequential or a gray code. Another popular structure for FSMs is a "one-hot" implementation. The one-hot structure uses one flip-flop per state with exactly one flip-flop in the state register set at any time. The implementation is straightforward and is essentially a shift register initialized such that exactly one of the flip-flops is a 1. This configuration makes decoding of a state trivial and frequently results in a high-performance implementation. The one-hot structure is often used for FPGA designs that are in general register rich; designs implemented in CPLD architectures often use one of the encoded forms.

Independent of the state machine structure, a high-reliability system must not contain any lockup states. These are unused states that cannot sequence into a valid state; the state machine is literally locked up. A correctly designed system should never enter one of these unused states. However, a Single Event Upset or other electrical transient or power supply disturbance may cause a soft error and result in an unused

state being entered. Since one-hot implementations are often used in FPGAs they will be discussed here in detail. Sequential or gray coded state machines are also a concern, with a detailed discussion of those types of machines discussed in the reference mentioned above.

A simple two-phase, non-overlapping clock generator is used for this example. This machine has four states and can logically be represented in VHDL code by by an enumerated type such as:

```
Type StateT Is (Ph1, Ph2, Ph3, Ph4);
```

Using the one-hot encoding, a state assignment is selected by the synthesizer and the states represented in four flip-flops can legally be:

0001
0010
0100
1000

However, there are 16 possible states of this four flip-flop state vector. Four are used in legal states and 12 are unused. The state machine can transition into any one of 5 illegal states from an SEU; any of the 12 illegal states can occur from a disruption to the power bus or other disturbance or malfunction. The one-hot implementation makes *any* SEU a transition into an illegal state. Since the implementation is essentially a shift register, the fault will never be cleared until the system applies a reset. For example, if the state register, as a result of an SEU goes into state **0101**, then we will see the following sequence of states:

0101
1010
0101
1010

with no hope of recovery. Similarly, if one of the "hot" flip-flops is cleared by an SEU, then the machine will never leave the **0000** state.

There are other structures which help in making a modified one-hot state machine implementation robust. As an example, when a "one-hot" implementation in Actmap is selected, only n-1 flip-flops are used and the all 0's state is a valid state in their implementation. This eliminates the problem of clearing a state bit; the all 0's case is legal and valid. Additionally, a NOR function of all flip-flops' outputs is performed and is input into the D-input of the first flip-flop in the shift register. This tends to clear situations where multiple flip-flops are set by holding off the input of a '1' to the first stage of the shift register. As an example, assume that we have entered, because of an SEU, the state 011 and that the rest of the state machine is well designed. The FSM will transition through the following sequence and then recover:

011
001
000
100

Similarly, if a state bit is cleared, the NOR function will force the next state to be **100**, a valid state.

FSMs using sequential state assignments are also at risk. If the number of used states is not an integral power of 2, then there will be unused states with undefined transitions. Note that use of the VHDL "Others" clause, for any state encoding, will not provide transitions from the unused physical states to a valid logical state. The Others clause operates only on the states defined in the enumeration; it does not operate on physical hardware states. This is disconnect between the abstracted VHDL language and real hardware. There is no mechanism to directly talk about a physical implementation at this level of abstraction; obviously, it can be done using structural coding which eliminates the benefits of the synthesizer and schematics can be used, often a more appropriate tool. Additionally, depending on the tool being used, it's settings, and perhaps even it's revision level, unused states in the state machine that are included in the enumeration may be eliminated by an optimizer that determines that the states are either unreachable or that have no effect on the output.

There is a technique that has been developed, which obviously does not apply to one-hot implementations but can be used, if care is applied, to FSMs using either a sequential or gray code state assignment. This is described in greater detail in the reference but a robust state machine can be coded in VHDL by ensuring that all possible physical states are in the enumeration and that the optimizer can not eliminate them. The preservation of the states and transitions may be pos-

sible via synthesizer directives and attributes. In the VHDL domain, a solution would be to force the number of states in the enumeration to be an integral power of two via the introduction of dummy states. Then an "extra" input should force the state machine into a sequence through these states with a dummy output. This will force the states to be reachable and significant.

The problems with robust state machines have been discussed with various vendors. One has added a "safe" mode option to the FSM encodings, since the hardware is not easily and efficiently controlled at the VHDL level, as shown briefly above. This safe encoding feature is controlled via attributes placed into the HDL code.

The synthesizer's algorithm in this mode will add extra overhead since circuitry is needed for the detection of an illegal state and recovery. For this study, I have used Synplify Lite version 5.1.5a. An overview of their algorithms and effects will be given here. Detailed examples of input at the VHDL level and output at the netlist level in the form of a schematic will be in the next edition, as the EEE Links production deadline is now here. The examples, used here as a framework for the discussion, was a two-phase, non-overlapping clock generator targetted to SX technology. In SX, an "R-Cell" is used as the flip-flop element.

It is obvious that there will be extra combinational logic to detect entry into an illegal state that will assert an error signal. In the implementation examined here, there are two additional R-Cells in the "safe" implementation. These are used for forcing the state machine back into a legal state when an illegal state is detected. The two R-Cells form a simple shift register, with the first R-Cell clocked on the same edge as the

FSM and the second R-Cell clocked on the opposite edge. The recovery of this circuit uses the first R-Cell to latch in the signal indicating an error. This is passed to the second R-Cell in the pair, clocked on the opposite edge. This second R-Cell drives the asynchronous inputs to the other R-Cells through 1 stage (in the simple test case used) of combinational logic.

There are two impacts to this implementation. The first, obviously, as that the flip-flop count has increased which will slightly increase the SEU cross-section of the design, since an error in the recovery flip-flops will force the system to change it's state erroneously.

The second impact of this recovery mechanism is for timing analysis and margin. When analyzing this circuit, which at the VHDL code level appears to only use the rising edge of the clock, the designer / analyst must also analyze the path from the negative edge-triggered flip-flop to the other devices clocked on the positive edge. This signal must be removed in a half clock cycle. Of course, the worst-case half cycle time period will be less than one-half of the clock period as a result of asymmetry in the clock signal at the R-Cell's inputs. This may be the critical timing path in the design.

Jet Propulsion Laboratory Parts Analyses

Joan Westgate
NASA / JPL
818-354-9529
joan.c.westgate@jpl.nasa.gov

Failure analyses (FA), destructive physical analyses DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

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FAILURE ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
8065	DATEL	9834	DC / DC Converter	BHR-15 / 670-D12
8071	Micronetics	9812	Noise Diode	5065
8101	Harris Semiconductor	None	Radiation Hardened Octal Inverting Tri-state Buffer	HCTS240
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
8087	Chip Express	9811	QYH530 Gate Array ASIC	-
8097	Actel	9536	Field Programmable Gate Array	A1020A
8135	Burr-Brown	9831	250 mA High Speed Buffer (Commercial Quality)	BUF634
8136	Burr-Brown	9826	Low Power 12 Bit Sampling CMOS ADC (Commercial Quality)	ADS7806U
8137	Burr-Brown	9852	16 Bit 10 uS Sampling CMOS ADC (Commercial Quality)	ADS7805U
8138	Analog Devices, Inc.	9829	CMOS Complete Direct Digital Synthesizer (Commercial Quality)	AD9832
8157	Xilink	9837	Radiation Hardened Field Programmable Gate Array	XQR4036XL
PART CONSTRUCTION ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
8088	Lockheed Martin	9746	Power Actuation and Switching Module	20066280
8114	Samsung Electronics	850	16M x 8 Bit NAND Flash Memory	KM29U128T

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

CA JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
88180	UNKNOWN	9715, 9719, 9725	CAPACITOR	CDR31BX103AKWS	P	03/20/98
88190	MICROSEMI CORPORATION	8835	1N4944	JANTXV1N4944	P	03/25/98
88191	MICROSEMI CORPORATION	9713	1N5611	JANTX1N5611	P	03/26/98
88194	LINFINITY	9712	5962-01-239-4123	M38510/11703BXA	P	03/28/98
88197	MICROSEMI CORPORATION	9025	1N4970	JANTXV1N4970	F	04/03/98
88197	MICROSEMI CORPORATION	9025	1N4970	JANTX1N4970	F	04/03/98
88198	NATIONAL SEMICONDUCTOR	9745A	54ACTQ244FMQB	5962-9218601MSA	P	04/15/98
88225	NATIONAL SEMICONDUCTOR	9439	JM54AC174BEA	M38510/75307BEA	P	04/15/98
88227	HARRIS SEMICONDUCTOR	9633	HS1-302RH-Q	5922R9581201VCC	P	04/26/98
88269	BALL AEROSPACE	UNKN	FLEX CABLE	CCD FLEX CABLES	P	07/29/98
96407	HARRIS SEMICONDUCTOR	9827	TRANSISTOR	JANTXV2N7225	P	05/25/99
96417	SEMICOA	9825	TRANSISTOR	JANTXV2N4261	P	05/21/99
99558	INTERPOINT	9705	MSA2815S/ES	MSA2815S/ES	P	03/09/99
99565	MICROSEMI CORPORATION	9626	DIODE	JANTXV1N4104UR-1	F	04/01/99
99568	MAXWELL	9844	M28861/6-002-S-B	M28861/6-002-S-B	F	03/15/99
99571	OPTEK	9810	TRANSISTOR	JANTXV2N2907A	P	05/17/99
99577	COMPENSATED DEVICES	9746	DIODE	JANTXV1N4625-1	F	04/02/99
99580	MICROSEMI	9849	DIODE	JANTXV1N4148-1	F	04/05/99
99581	MICROPAC INDUSTRIES	9629	DIODE	JANTXV1N6092	P	04/09/99
99585	SENSITRON SEMICONDUCTOR	9810	DIODE	JANTXV1N5418	F	04/27/99
99588	MICROSEMI	9735	DIODE	JANTXV1N4245	P	04/15/99
99589	MICROSEMI CORPORATION	9518	DIODE	JANTXV1N5611	P	04/27/99
99598	SATCOM TECH CORP	9810	TRANSISTOR	JANTXV2N2222	P	05/24/99
99599	MICROSEMI CORPORATION	9622	DIODE	JANTXV1N5611	P	05/13/99
99602	BKC SEMICONDUCTORS	UNKN	DIODE	JANS1N6642U	P	05/10/99
99728	OPTEK	9823	2N5796U	JANTXV2N5796U	P	03/08/99
99747	HARRIS SEMICONDUCTOR	9849	MOSFET	FRF9150R3	P	05/27/99
99749	HARRIS SEMICONDUCTOR	9627	MICROCIRCUIT	5962R9581303	P	04/27/99
99753	MICROSEMI CORPORATION	8844	DIODE	JANTXV1N4463	P	04/16/99
99759	MICROSEMI CORPORATION	8914B	DIODE	JANS1N4148-1	P	04/19/99
99765	STATE OF THE ART	9803	RESISTOR	D55342E07B150DR	P	05/17/99
EV JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
80626	HARRIS SEMICONDUCTOR	9435, 9422	MICROCIRCUIT	HS926C31RH-Q	P	03/25/98

FA JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
80779	DIALIGHT	UNKN	LED	521-9186	F	04/09/98
80792	NATIONAL SEMICONDUCTOR	9521	LF411	JM38510/11904	P	04/14/98
88213	TEXAS INSTRUMENT	8040	DS7830	679-9111	P	05/06/98
99266	UTMC	9703	MICROCIRCUIT	5962R9654201QXA	F	02/12/99
99271	AEROJET	UNKN	MIXER ASSEMBLY	13350 19-4, SNF05	F	02/25/99
99272	UNKNOWN	UNKN	CONNECTOR ASSEMBLY	UNKNOWN	F	02/16/99
99299	AMPTEK	9734	HYBRID	A111A	F	04/21/99
99325	SSDI	9333	TRANSISTOR	SFT1192/5TVX	F	05/25/99
99594	ANALOG DEVICES	9608	MICROCIRCUIT	ADG508FTQ	F	05/26/99
99697	BKC SEMICONDUCTORS	9734	DIODE	JANTXV1N6468	F	04/12/99
99699	ANALOG DEVICES	9616	LM108	M38510/10104BGA	F	03/08/99
99765	STATE OF THE ART	9803	RESISTOR	D55342E07B150DR	P	05/17/99
EC JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
89324	YOUNG ELECTRONICS	9728	P W BOARD	8167642-1 REV A	P	04/01/98
89325	YOUNG ELECTRONICS	9728	P W BOARD	8148458-1 REV A	P	04/01/98
89326	YOUNG ELECTRONICS	9728	P W BOARD	8147416-1 REV G	P	04/01/98
89327	YOUNG ELECTRONICS	9727	P W BOARD	8148331-1 REV E	P	04/01/98
89328	YOUNG ELECTRONICS	9727	P W BOARD	8148326-1 REV F	P	04/01/98
89336	SPEEDY CIRCUITS	UNKN	P W BOARD	80895534 REV B	P	04/03/98
89337	SPEEDY CIRCUITS	UNKN	P W BOARD	80895536 REV A	P	04/03/98
89338	SPEEDY CIRCUITS	UNKN	P W BOARD	80895537 REV A	P	04/03/98
89339	SPEEDY CIRCUITS	UNKN	P W BOARD	80895538 REV A	P	04/03/98
89341	SPEEDY CIRCUITS	UNKN	P W BOARD	80895540 REV A	P	04/06/98
89342	SPEEDY CIRCUITS	UNKN	P W BOARD	80895541 REV A	P	04/06/98
89343	SPEEDY CIRCUITS	UNKN	P W BOARD	80895542 REV A	P	04/06/98
89344	SPEEDY CIRCUITS	UNKN	P W BOARD	80895543 REV A	P	04/06/98
89345	CIRTECH INC	1198	P W BOARD	858014-1-900 REV A1	P	04/07/98
89346	ADVANCED QUICK	0598	P W BOARD	IM-AC-5051	P	04/07/98
89347	ADVANCED QUICK	0598	P W BOARD	IM-AC-5071	P	04/07/98
89348	NORTH TEXAS CIRCUIT	05798	P W BOARD	3050710-001 REV F	F	04/08/98
89349	YOUNG ELECTRONICS	9725	P W BOARD	8156978-1 REV A	P	04/10/98
89350	YOUNG ELECTRONICS	9724	P W BOARD	8152182-1 REV B	P	04/09/98
89351	YOUNG ELECTRONICS	9720	P W BOARD	8158801-1	P	04/10/98
89352	YOUNG ELECTRONICS	9619	P W BOARD	8167570-1 REV B	P	04/09/98
89353	YOUNG ELECTRONICS	9610	P W BOARD	8156981-1 REV A	P	04/10/98
89354	YOUNG ELECTRONICS	9608	P W BOARD	8158697-1	P	04/10/98
89355	YOUNG ELECTRONICS	9537	P W BOARD	8148703-1 REV D	P	04/10/98
89940	SPEEDY CIRCUITS	UNKN	P W BOARD	80895539 REV A	P	04/03/98
90850	YOUNG ELECTRONICS	9728	PWBOARD	8147531-1 REV E	P	01/04/99
90854	YOUNG ELECTRONICS	9728	PWBOARD	8148366-1 REV F	P	01/04/99
90857	YOUNG ELECTRONICS	9720	PWBOARD	8158766-1	P	01/05/99
90860	YOUNG ELECTRONICS	9729	PWBOARD	8165944-1	P	01/04/99
90861	YOUNG ELECTRONICS	9730	PWBOARD	8148601-1 REV D	P	01/06/99

EC JOBS *(continued)*						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
90862	YOUNG ELECTRONICS	9730	PWBOARD	8148723-1 REV G	P	01/05/99
90863	YOUNG ELECTRONICS	9731	PWBOARD	8148281-1 REV D	P	01/05/99
90864	YOUNG ELECTRONICS	9731	PWBOARD	8148648-1 REV F	P	01/06/99
90865	YOUNG ELECTRONICS	9731	PWBOARD	8148643-1 REV D	P	01/06/99
90866	YOUNG ELECTRONICS	9733	PWBOARD	8170463-1	P	01/12/99
90867	YOUNG ELECTRONICS	9734	PWBOARD	8165944-1	P	01/07/99
90868	YOUNG ELECTRONICS	9747	PWBOARD	8177130-1	P	01/08/99
90869	AMBITECH INC	9802	PWBOARD	8170482-1	P	01/08/99
90874	ALLIED SIGNAL	9846	PWBOARD	3050710-001 REV G	P	01/11/99
90875	CIRTECH INC	3298	PWBOARD	3050814-001 REV A	P	01/07/99
90876	SAS CIRCUITS, INC.	5098	P W BOARD	WB548596-001 REV B	P	01/07/99
90877	BF GOODRICH	658	PWBOARD	PB605710403-01 REV B	F	01/08/99
90878	ALLIED SIGNAL	9852	PWBOARD	3050786-001 REV C	P	01/20/99
90879	ACTION COMPUTER	9842	PWBOARD	731-000215-1	P	01/20/99
90880	ACTION COMPUTER	9842	PWBOARD	LCD11006046 REV F	P	01/20/99
90881	ACTION COMPUTER	9839	PWBOARD	731-000218-1 REV A	P	01/22/99
90882	ADVANCED QUICK	5198	PWBOARD	GC2035088-1	F	01/22/99
90883	ADVANCED QUICK	5198	PWBOARD	GC2035089-1	P	01/15/99
90884	SIERRA CIRCUITS	5298	PWBOARD	12083-001 REV A2	F	01/14/99
90885	RIGIFLEX TECHNOLOGY	4498	PWBOARD	IM-EP-5208-1	P	01/25/99
90886	ACTION COMPUTER	9841	PWBOARD	LCD11006412-1 REV 4	P	01/25/99
90887	ACTION COMPUTER	9819	PWBOARD	731-001149-1 REV A	p	01/25/99
90888	ACTION COMPUTER	9850	PWBOARD	731-000203-1 REV B	P	01/25/99
90889	RIGIFLEX TECHNOLOGY	3198	PWBOARD	1309193	F	01/19/99
91008	SPEEDY CIRCUITS	9910	PWBOARD	LVPS REV C	P	04/01/99
91009	TYCO ENGINEERED	9838	PWBOARD	868561-1	P	04/06/99
91010	LOCKHEED MARTIN	999	PWBOARD	226A851-1	P	04/06/99
91011	CIRTECH INC	1199	PWBOARD	3050790 REV C	P	04/07/99
91012	CIRTECH INC	1199	PWBOARD	3050784-001 REV C	P	04/07/99
91013	ELECTRO PLATE	90318	PWBOARD	2A06534-101	P	04/09/99
91016	ELECTRO PLATE	90329	PWBOARD	A33828P01 REV B	P	04/12/99
91017	ALLIED SIGNAL	9850	PWBOARD	868693-1	P	04/15/99
91019	TYCO ENGINEERED	1499	PWBOARD	856657	F	04/14/99
91020	SUN CIRCUITS	1399	PWBOARD	2A06608-101	P	04/16/99
91021	RIGIFLEX TECHNOLOGY	999	PWBOARD	IM-OR-7506-1	F	04/16/99
91022	COLONIAL CIRCUITS	9913	PWBOARD	9271-201 REV B/B	P	04/20/99
91023	SAS CIRCUITS, INC.	999	PWBOARD	BE03995305	P	04/23/99
91024	SAS CIRCUITS, INC.	1199	PWBOARD	WB538606-001 REV B	F	04/23/99
91025	SAS CIRCUITS, INC.	1099	PWBOARD	WB538602-001	P	04/26/99
91026	ADVANCED QUICK	1099	PWBOARD	GD2028913 REV A	P	04/29/99
91027	SPEEDY CIRCUITS	9914	PWBOARD	8089-3810	P	04/19/99
91028	SPEEDY CIRCUITS	9914	PWBOARD	8089-3830	P	04/19/99
91029	ADVANCED INTERCONNECTION	70207	PWBOARD	PD10085-2 (TRW 49)	P	04/28/99
91030	COLONIAL CIRCUITS	9914	PWBOARD	040-126	F	04/28/99

EC JOBS *(continued)*						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
91031	SUN CIRCUITS	1599	PWBOARD	2A06605-101	P	04/29/99
91032	ADVANCED QUICK	1599	PWBOARD	GD2027363	P	04/22/99
91033	ADVANCED QUICK	1599	PWBOARD	GD2027393	F	04/23/99
91034	ADVANCED QUICK	9915	PWBOARD	GD2038626-1	P	04/26/99
91049	ADVANCED QUICK	1799	PWBOARD	GC2035088-1	P	05/06/99
91115	SPECTRA INC	9835	PWBOARD	442438	F	06/17/99
91116	SPECTRA INC	9809	PWBOARD	440618	P	06/22/99
91117	ELECTRO PLATE	9904	PWBOARD	040-115	F	06/07/99
91118	ADVANCED QUICK	2199	PWBOARD	GC2038629-1	F	06/05/99
91119	ADVANCED QUICK	2199	PWBOARD	GC2038628-1	F	06/05/99
91120	ADVANCED QUICK	2199	PWBOARD	GD2027353	P	06/05/99
91121	ELECTRO PLATE	9905	PWBOARD	040-140	P	06/15/99
91122	RJR CIRCUITS INC	9918	PWBOARD	WB540829-001	F	06/16/99
91123	SAS CIRCUITS, INC.	1199	PWBOARD	WB540664-001	P	06/09/99
91124	SAS CIRCUITS, INC.	1199	PWBOARD	WB540665-001	P	06/09/99
91125	ADVANCED QUICK	1899	PWBOARD	IM-RC-5121-1	P	06/17/99
91126	ADVANCED QUICK	2199	PWBOARD	GD2027353	P	06/09/99
91127	COLONIAL CIRCUITS	2298	PWBOARD	040-141	F	06/18/99
91128	CIRTECH INC	2099	PWBOARD	856639-1 REV A1	P	06/21/99
91129	ELECTRO PLATE	9905	PWBOARD	2A06541-101	P	06/22/99
91130	RIGIFLEX TECHNOLOGY	299	PWBOARD	IM-RC-5211-1	P	06/24/99
91131	ADVANCED QUICK	2099	PWBOARD	IM-OR-7513-1	P	06/25/99
91132	ELECTRO PLATE	9906	PWBOARD	2A06538-101	P	06/25/99
91133	ELECTRO PLATE	9922	PWBOARD	GD2023583	P	06/23/99
91134	ELECTRO PLATE	9905	PWBOARD	1A27889-501	P	06/21/99
91135	ADVANCED INTERCONNECTION	50302	PWBOARD	PD10095-1 (TRW 51)	P	06/28/99
91136	ADVANCED INTERCONNECTION	70213	PWBOARD	PD10085-2 (TRW 49)	P	06/28/99
91137	ADVANCED INTERCONNECTION	70214	PWBOARD	PD10085-1 (TRW 49)	P	06/28/99
91138	SPECTRA INC	9922	PWBOARD	IM-RC-5111-1	P	06/25/99
91139	ELECTRO PLATE	9906	PWBOARD	2A06541-101	P	06/30/99
91140	YOUNG ELECTRONICS	9901	PWBOARD	8167570-1	F	07/01/99
91141	YOUNG ELECTRONICS	9909	PWBOARD	8148256-1	P	06/29/99
91142	SPEEDY CIRCUITS	9923	PWBOARD	100MHZ A/D REV A	P	07/01/99
91143	SPEEDY CIRCUITS	9923	PWBOARD	LVPS REV D	F	07/01/99
91144	BF GOODRICH	206	PWBOARD	PB60571-104-01	P	06/24/99
91145	ELECTRO PLATE	9906	PWBOARD	346011-1	P	07/02/99
91146	RJR CIRCUITS INC	9923	PWBOARD	WB544848-001	P	07/02/99
91147	ADVANCED QUICK	2499	PWBOARD	20082634P1 REV B	F	07/08/99
91148	CIRTECH INC	2499	PWBOARD	3050830-001 REV A	F	07/08/99
91149	PROTO CIRCUITS	2299	PWBOARD	NISTAR	P	07/07/99