ROD Simulation Results

Wisconsin SCT/pixel ROD Group:

K. Dao

D. Fasching

R. Jared

J. Joseph

M. Nagel

L. Stromburg

L. Tomasek

December 17, 1999

Simulation General Information

- The C simulation is a flexible card driven model which allows
  - testing the expected behavior of the ROD under a wide variety of conditions
  - evaluating the impact of proposed algorithm changes on the ROD behavior
  - cross checking the VHDL code with large data samples
  - debugging/commissioning RODs in conjunction with the test stand

- The main simulation loop represents one cycle of the LHC 40 MHz clock which drives all detector mounted and off-detector electronics and which is synchronous with proton bunch crossings.

- Within each clock loop, triggers and data generation are simulated along with the data path, from pipelines and buffers on the detector mounted electronics to the output of the ROD. At each step, all data which would be alive in the actual system are alive in the simulation. Dead ABCs are also included.
- The simulation of the detector mounted electronics includes pipelining and buffering of hits for the duration of the level 1 trigger latency, buffer overflows and errors, event formatting and transmission to the ROD.
- The transmission model includes the transmission delay and bit errors.

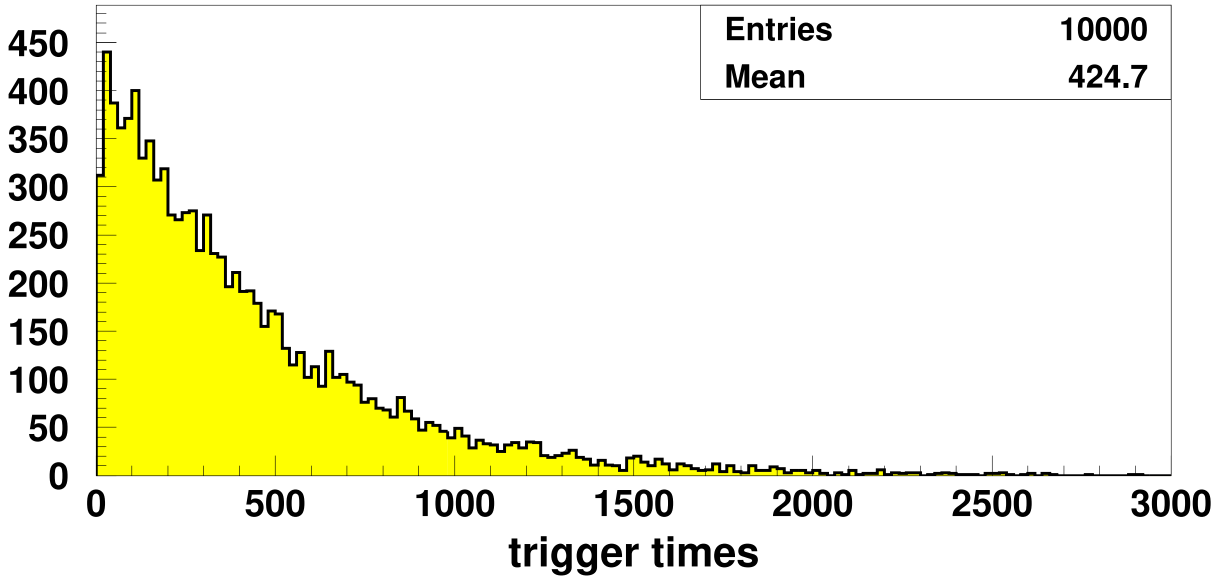
- The ROD model which has been described is fully simulated, starting with the bit-driven per-link formatter state machines and proceeding through each logical block of the FPGAs. The interfaces between the FPGAs have the same data paths and bit assignments as in the VHDL model.
- The generated input bitstreams can be written to a file which can be used as test data for the VHDL model. The data at the output as well as at several intermediate points on the board can be dumped to a file for comparison with correspoding outputs of the VHDL model.

- The ROD simulation includes all features which affect the data flow, e.g.
  - header-only mode in the link formatters
  - ROD_BUSY
  - XON/XOFF
  - variable detector occupancies
  - variable output bandwidth
  - variable buffer sizes

Trigger Generation

Level 1 accepts are generated according to a Poisson distribution around 100 KHz (400 clock cycle separation) Triggers are vetoed according to two ATLAS level 1 deadtime algorithms:

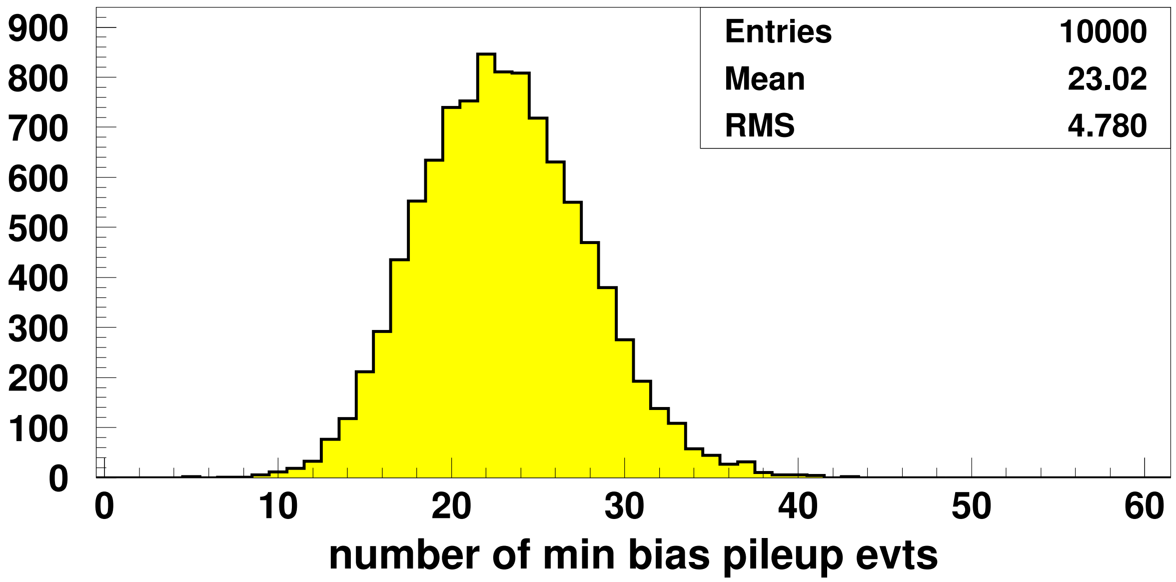
- Triggers separated by $\geq$ 4 bunch crossings
- $Q_{Q\geq 0} = (N_{L1A} \times 400) - n_{BC} \leq 3200$



Mean level 1 accept rate = 95 KHz after deadtime algorithms.

Data Generation

- For each level 1 accept choose the number of minimum bias events in from a Poisson distribution with a mean of 23



- For each column-pair (pixels) or half-module (SCT) choose the number of hits for the triggered bunch crossing from an occupancy distribution corresponding to the chosen number of minimum bias events. These occupancy histograms are derived from the ATLAS Monte Carlo.
- Include jets and clustering.
- Apply a scale factor if desired.

Simulation Runs

Several factors influence the mapping of data links into RODs

- ATLAS trigger architecture
- detector geometry
- data link modularity
- back of crate card real estate
- backplane pin count
- modularity of ROD components
- buffer sizes
- dataflow / data loss
- cost

The current link to ROD mapping is

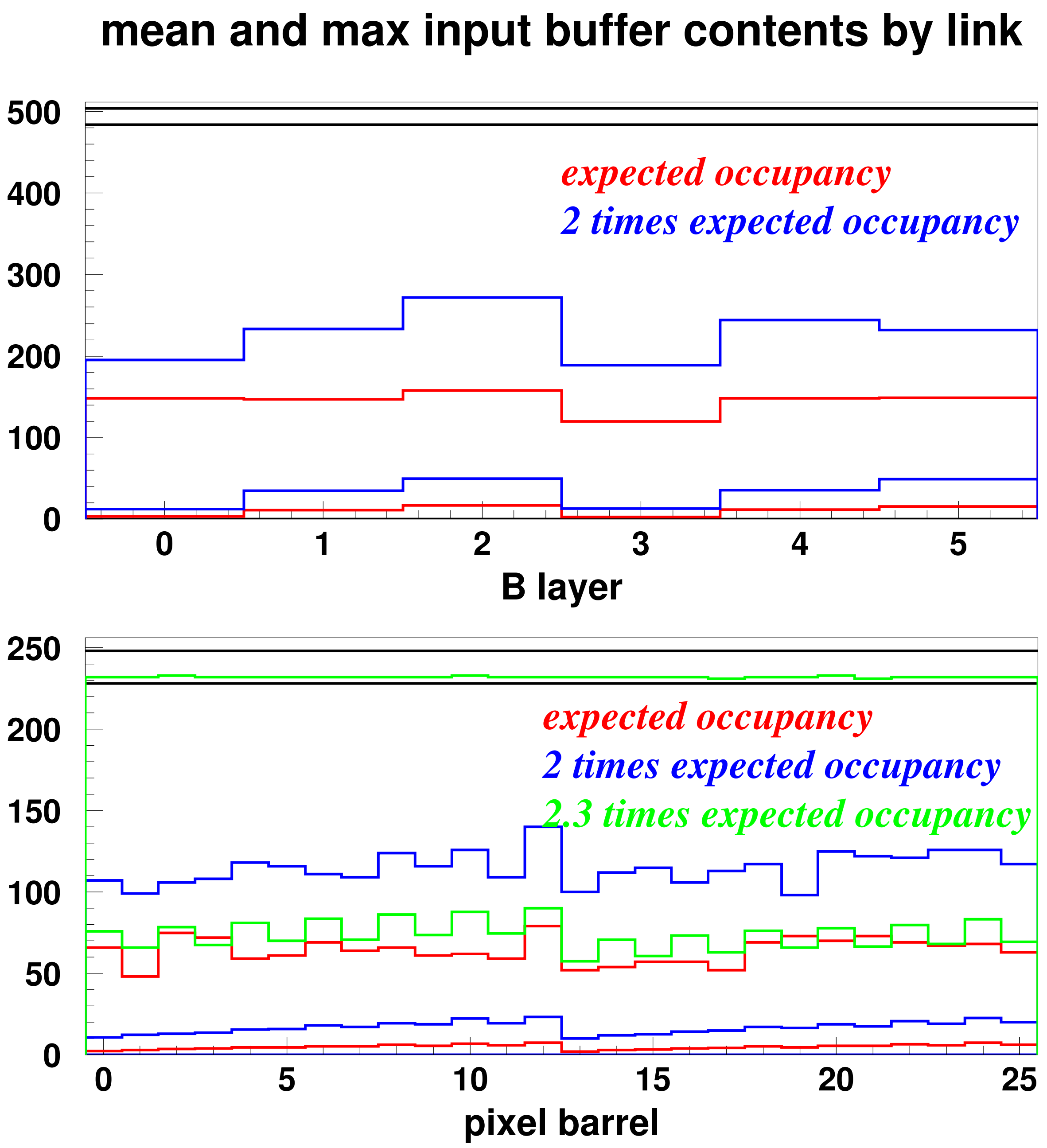
- 6 links per B layer ROD distributed in η
- 26 links per pixel barrel ROD; either 1 stave from each of the layer or 2 staves from barrel 2

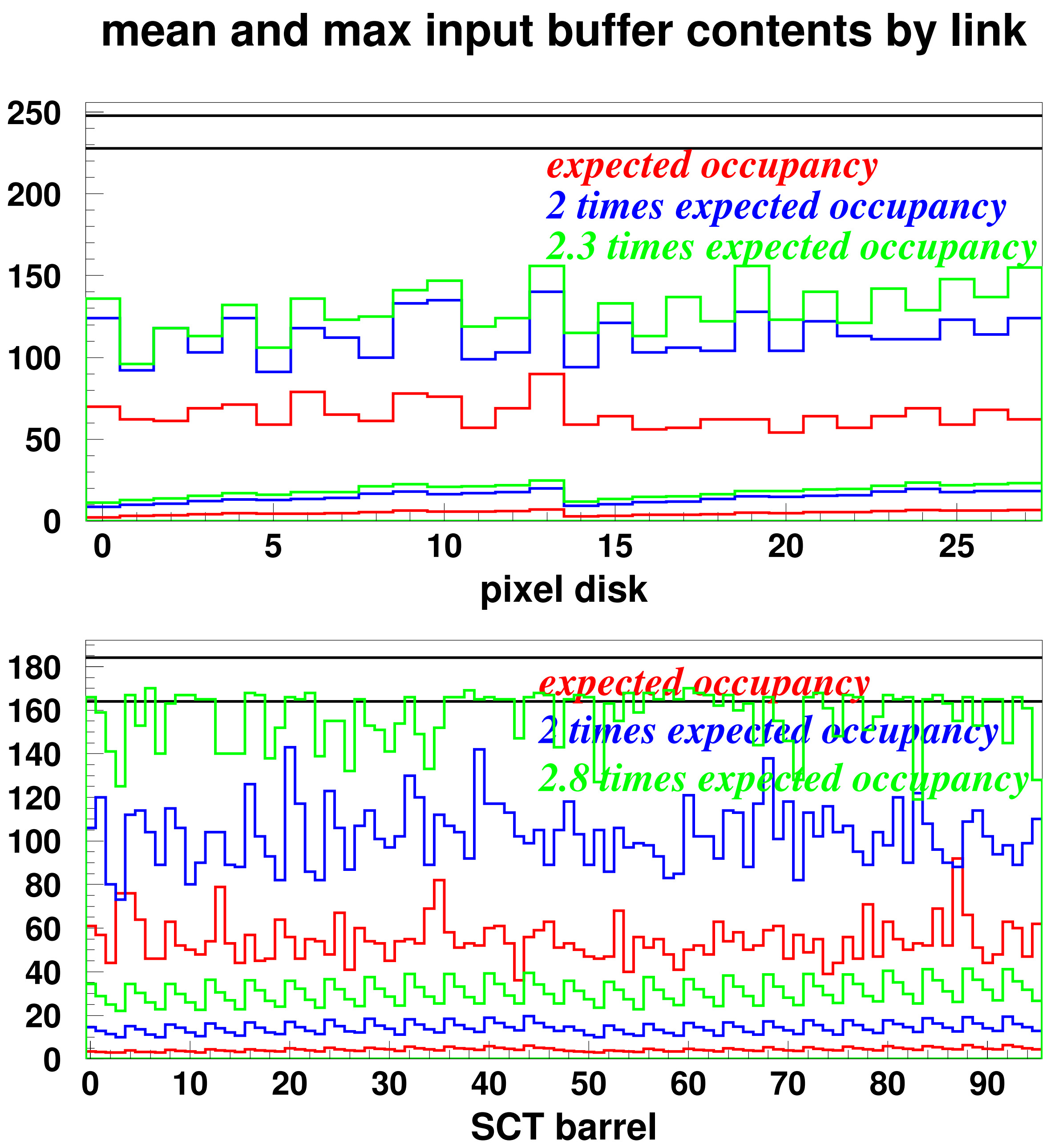
- 28 links per pixel endcap ROD; 18 from disks 1-3 and 10 from disks 4-5
- 96 links per SCT barrel ROD with 24 links from each layer
- 96 - a_few (due to cableing) per SCT endcap ROD

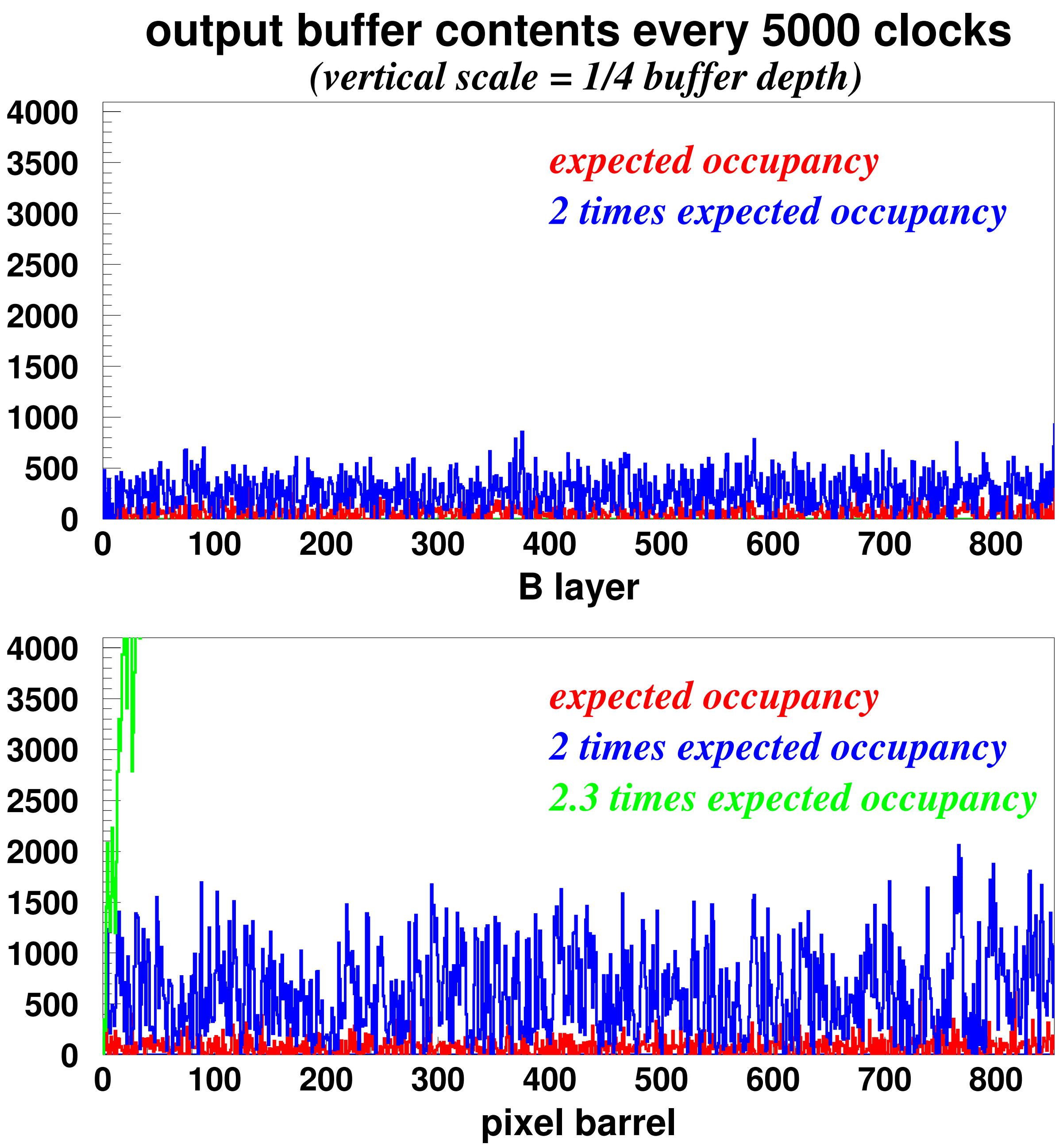
For the current best mapping runs were performed with 10,000 events under the following conditions

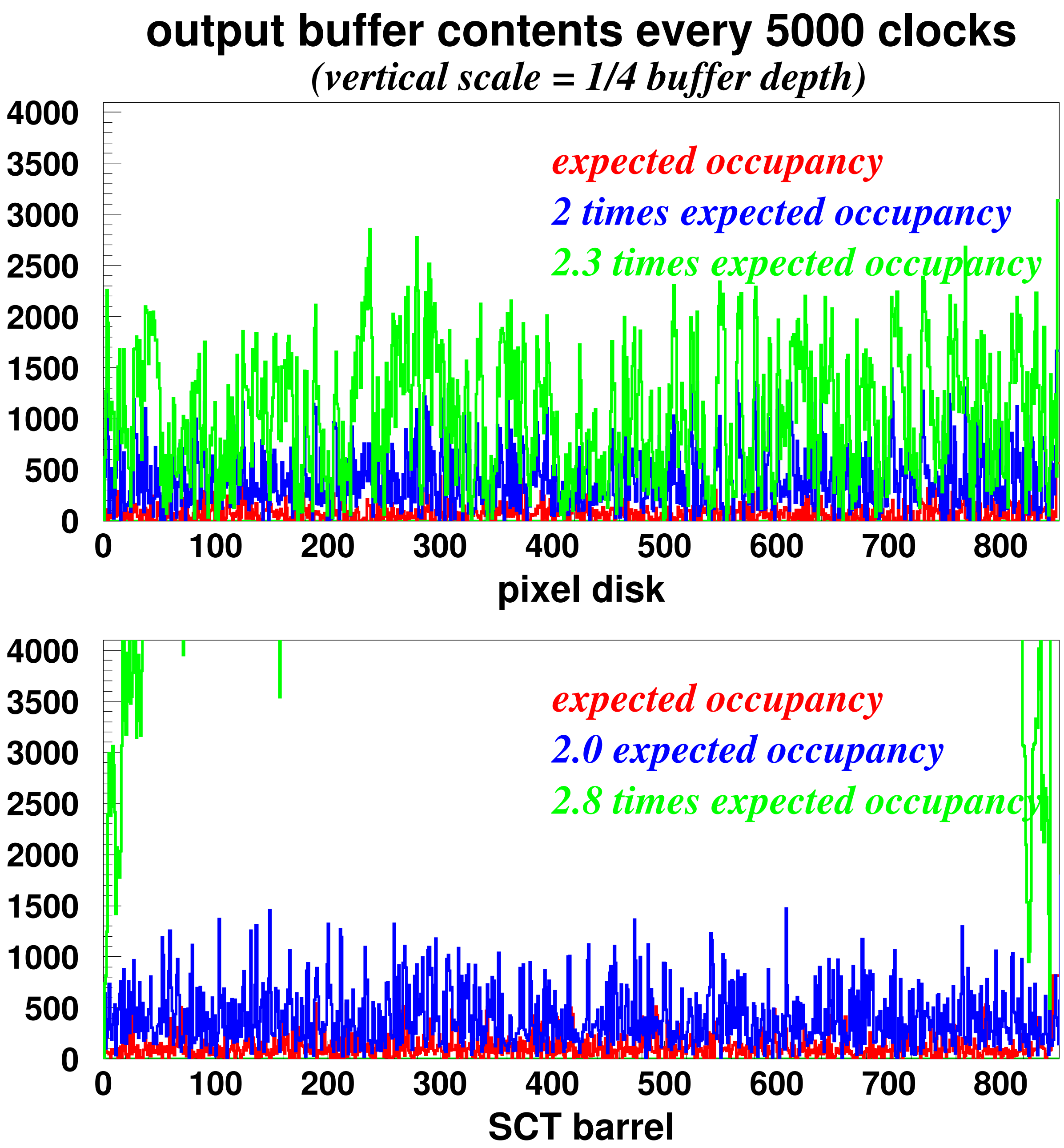
- nominal occupancy and 2 times nominal occupancy
- occupancy at the limit of the data flow off the ROD
- conditions which tested the bandwidth limit of the ROD through the event fragment builder

Data loss, used output bandwidth and ROD behavior were monitored.

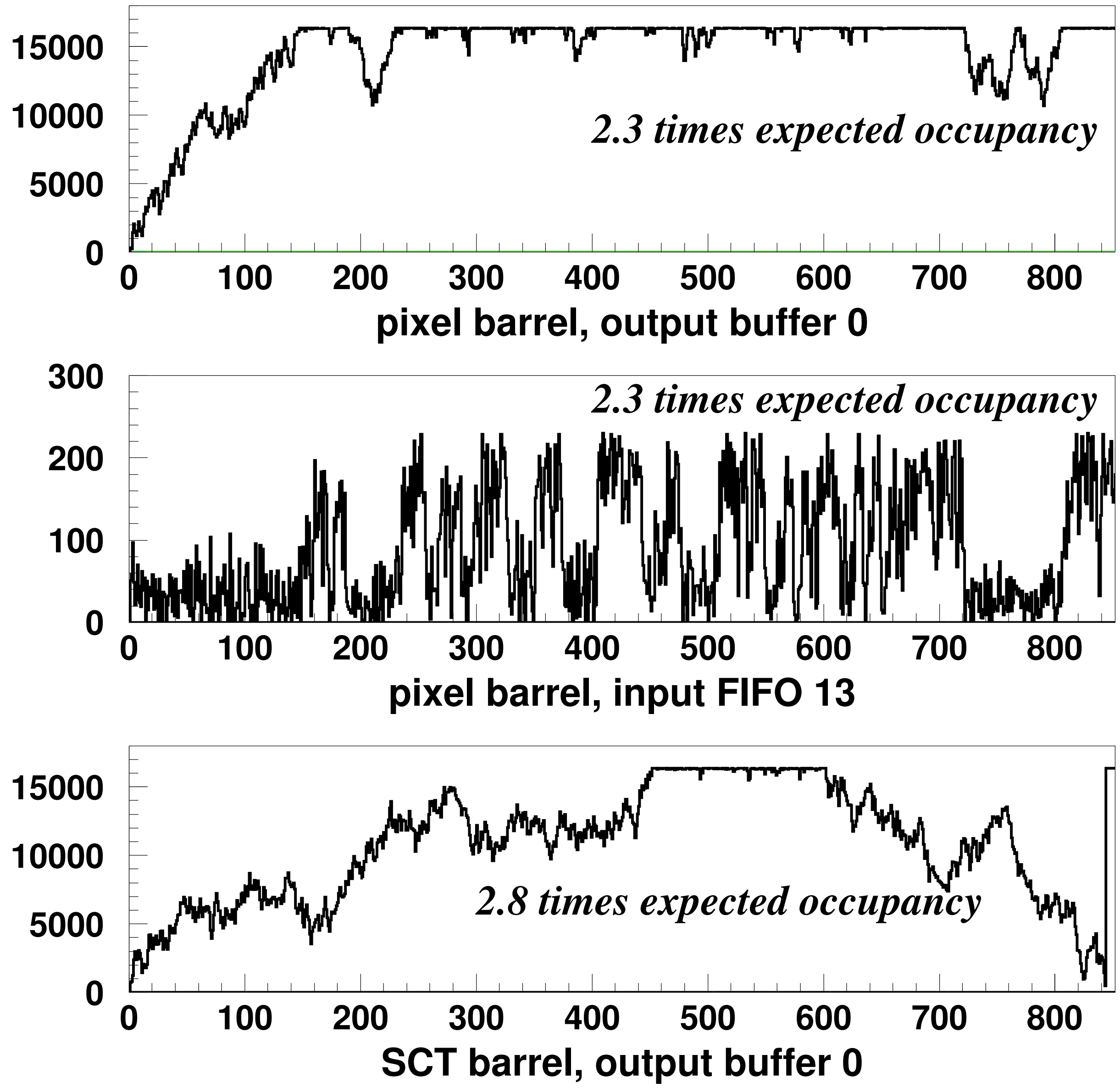

mean and max input buffer contents by link
500
400
300
200
100
0
0
1
2
3
4
5
B layer
expected occupancy
2 times expected occupancy
250
200
150
100
50
0
0
5
10
15
20
25
pixel barrel
expected occupancy
2 times expected occupancy
2.3 times expected occupancy


mean and max input buffer contents by link
250
200
150
100
50
0
0
5
10
15
20
25
pixel disk
expected occupancy
2 times expected occupancy
2.3 times expected occupancy
180
160
140
120
100
80
60
40
20
0
0
10
20
30
40
50
60
70
80
90
SCT barrel
expected occupancy
2 times expected occupancy
2.8 times expected occupancy


output buffer contents every 5000 clocks
(vertical scale = 1/4 buffer depth)
expected occupancy
2 times expected occupancy
4000
3500
3000
2500
2000
1500
1000
500
0
0
100
200
300
400
500
600
700
800
B layer
expected occupancy
2 times expected occupancy
2.3 times expected occupancy
4000
3500
3000
2500
2000
1500
1000
500
0
0
100
200
300
400
500
600
700
800
pixel barrel

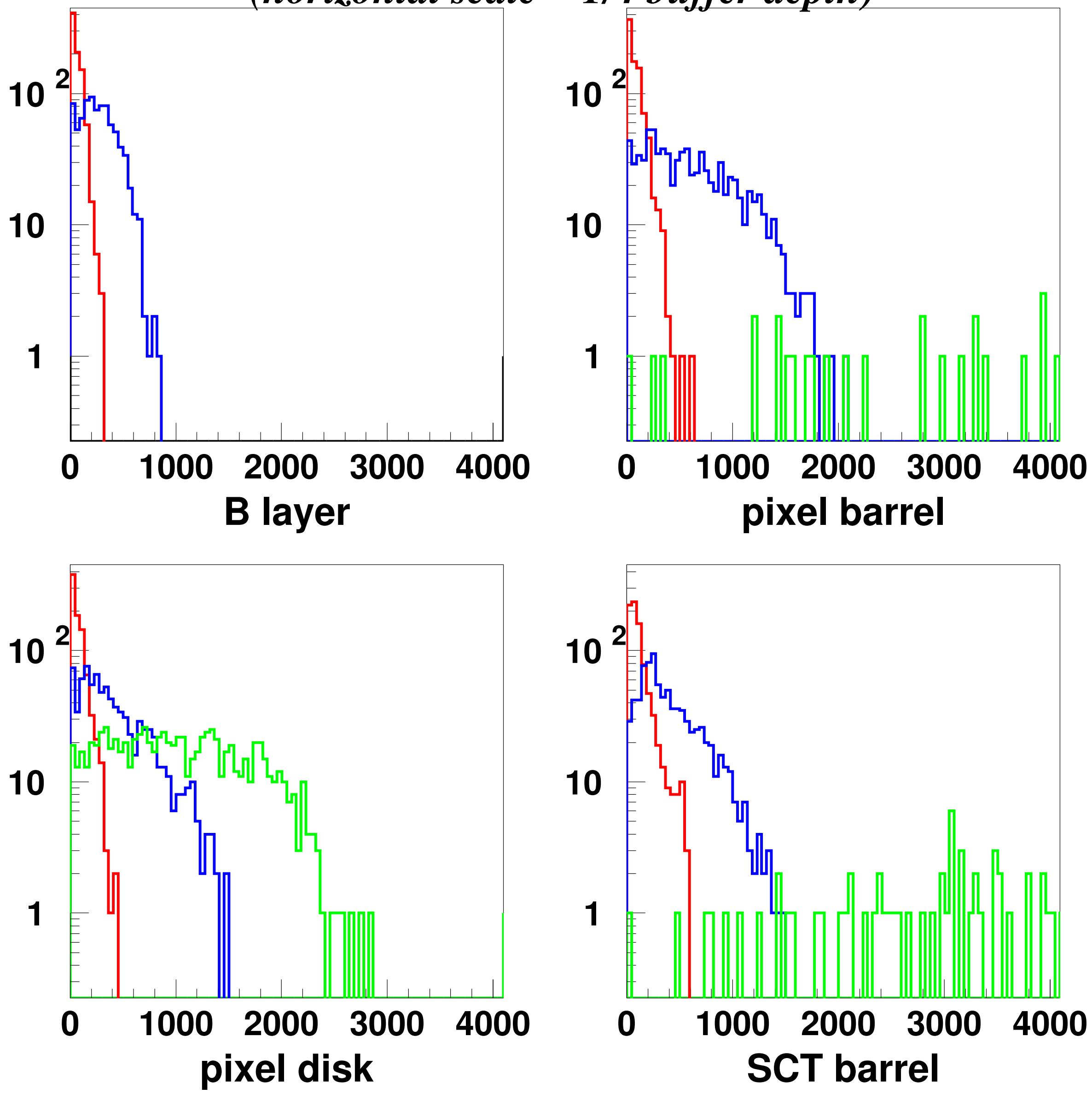

output buffer contents every 5000 clocks
(vertical scale = 1/4 buffer depth)
expected occupancy
2 times expected occupancy
2.3 times expected occupancy
pixel disk
expected occupancy
2.0 expected occupancy
2.8 times expected occupancy
SCT barrel

some runaway cases



output buffer contents, projections

(horizontal scale = 1/4 buffer depth)



Summary

Detector	Link Count	Occupancy Scale Factor	S-Link Rate (MWps)	Band-width Used (MWps)	Fraction Header Only Events
B layer	6	1.0	40	19.2	–
	6	2.0	40	33.4	–
	6	2.4	40	35.8	–
pxl brl	26	1.0	40	19.9	–
	26	2.0	40	35.9	–
	26	2.3	40	39.9	.03
pxl dsk	28	1.0	40	19.1	–
	28	2.0	40	33.9	–
	28	2.3	40	38.2	–
SCT brl	96	1.0	40	17.8	–
	96	2.0	40	30.4	–
	96	2.8	40	39.9	2×10^{-4}
B layer	12	2.0	∞	65.9	1×10^{-5}
pxl brl	50	2.0	∞	68.0	.01
pxl dsk	55	2.0	∞	66.6	.001
SCT brl	96	3.5	∞	49.3	5×10^{-4}