Efficiency limitations for wide-band-gap chalcopyrite solar cells

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Abstract

Wide-band-gap chalcopyrite solar cells, most prominently Cu(In,Ga)Se_2 (CIGS) with high Ga content, have failed over the past years to achieve conversion efficiencies consistent with those achieved with lower-Ga CIGS. Starting from a simple baseline case of a ZnO/CdS/CIGS solar cell, numerical modeling tools were used to investigate the effects of bulk and interface recombination for a broad range of absorber band-gap energies assuming that the Ga/In ratio primarily affects the conduction band. The model predicts that even very small interface recombination velocities limit the open circuit voltage, when the conduction-band offset between window and absorber layer is close to zero or is negative. This is the case for CdS/CIGS structures with absorber band gaps above 1.3 - 1.4 eV. The simulations further predict that surface phases or pinning of the Fermi level at the interface can inhibit interface recombination, and hence, lead to an improvement in cell efficiency. Conversion efficiency for all band-gap energies is calculated based on a generic window layer/absorber structure assuming that the band alignment can be arbitrarily chosen. The implication of this work is that although the record CIGS efficiencies have been achieved with CdS window layers, CdS may not be the best window layer for wide-band-gap chalcopyrite solar cells. Our results agree very well with the reported record efficiency for CdS/$CuInSe_2$, CdS/CdTe, CdS/$CuGaSe_2$, and CdS/Cu(In,Ga)Se_2 solar cells.

1 Introduction

Earlier work discussed the effect of the conduction-band offset (CBO) for CdS/CIS [1–3] or low Ga content CdS/CIGS solar cells [4] assuming a fixed absorber band gap while the CBO was varied. It has been observed that increasing recombination at the window-absorber interface lowers the open circuit voltage, V_{oc}, for negative CBO [2–4] and, hence, a positive band offset is important for high device performance. Many attempts in recent years to increase V_{oc} of the Cu(In,Ga,Al)Se_2 system beyond 0.8 V have not been successful [5–8]. The open circuit voltage increases proportionally to the absorber band gap, E_g, up to band-gap energies of about 1.3 eV; in this lower regime the approximate expression $V_{oc} = E_g - 500$ mV holds reasonably well [7]. For larger band gaps, the difference between V_{oc} and E_g increases, and for high band gaps V_{oc} is constant at about 0.8 V.

Numerical simulation tools are used to evaluate the effect of increasing bulk and interface recombination for a wide range of absorber band gaps. The valence-band offset (VBO) is kept fixed while the band gap increases and the CBO decreases. Interface recombination can limit the open circuit voltage to a value that is determined by the interface quality in agreement with a recently proposed analytical model [9]. For an interface dominated model, we also evaluate the effects of (1) "conduction band" widening at the surface ("grading"), (2) "valence band" widening at the surface (i.e. Cu-poor surface phases), and (3) pinning of the interface by charged deep states. Our results are in good agreement with the design criteria discussed by Klenk [10] and show that the crucial parameter in achieving high open circuit voltages is the hole depletion at the CdS/CIGS interface.

2 Device Model

The modeling calculations discussed in the following sections used the software tool SCAPS [11]. SCAPS calculates the steady-state band diagram, recombination profile, and carrier transport in one dimension based on the Poisson equation and the hole and electron continuity equations. Recombination currents are calculated with the Shockley-Read-Hall

(SRH) model for bulk defects and an extension of the SRH model for interface defects. The SRH interface approach allows carriers from both conduction and valence bands to participate in the interface recombination process. In this contribution, interface quality is expressed by the interface recombination velocity, v_{intf} , as a fraction of the thermal velocity, v_{th} ($\approx 10^7$ cm/s).

The baseline (BL) used for the calculations is our reported CIGS (E_g = 1.15 eV) baseline case [12] with additional recombination centers ("neutral" defect states, with large capture cross sections and small density) present in the bulk CIGS. The band alignment at the interface of CdS and 1.15 eV CIGS is chosen as +0.3 eV, guided by experimental [13, 14] and theoretical studies [15]. The default illumination spectrum is set to the global AM1.5 standard for terrestrial solar-cell measurements [16]. The resulting band diagram calculated in thermodynamic equilibrium is given in Fig. 1 (a). The J-V parameters for the BL model are: short circuit current density J_{sc} = 35 mA/cm^2, open circuit voltage V_{oc} = 0.63 V, fill factor FF = 77%, and efficiency η = 17%. Starting from this BL case, the band gap is varied under the assumption that changes occur in the conduction band only, as it would be expected for interchanging Ga or Al for In in $CuInSe_2$ [17]. Optical absorption for the 1.15 eV CIGS material is taken from experimental data reported by Paulson et al. [18] and is shifted on the energy axis for other band-gap energies. J-V curves are calculated for band-gap energies in the range from 0.85 – 2.05 eV, which intentionally exceeds the physical limits of the $Cu(In,Ga)Se_2$ system, since the results should be general and not limited to this particular material system. The conduction-band offset varies in the model from +0.6 eV to –0.6 eV. The CBO is positive ("spike", i.e. Fig. 1 (a)), by convention, if CBO and VBO are both smaller than the band gap difference ΔE_g. If the VBO is larger than ΔE_g, then the CBO is negative ("cliff", i.e. Fig. 1 (b)).

3 Results

3.1 Bulk Recombination

Fig. 2 shows the simulated J-V results with spatially uniform bulk recombination centers for the range of band gaps investigated. V_{oc} increases with the band gap as $V_{oc} = E_g - 530$ mV, and J_{sc} decreases with increasing band gap due to the lower-wavelength cut off. For a CBO greater than 0.5 eV, J_{sc} is dramatically reduced due to the large spike barrier for photogenerated electrons. The fill factor is relatively flat and decreases with large offsets in either direction due to cliff or spike barriers. The highest efficiency of 18.3% in this simulation without interfacial recombination is achieved with a band gap of 1.35 eV, however, 17 – 18% devices are calculated with band gaps from 1.15 – 1.55 eV, which corresponds in our model to conduction band offsets of +0.3 eV to –0.1 eV.

The previous results change only quantitatively if the density, $N_{Baseline}$ or N_{BL}, of the "charge-free" recombination centers, which are assumed mid-gap for all band gaps, is increased (3x, 10x, 30x, 100x) (Fig. 2). V_{oc} losses are slightly higher for band gaps below 1.5 eV. With $100xN_{BL}$, the highest efficiency drops to 11.4%, and 10 – 11% devices are found for band-gap energies of 1.25 – 1.75 eV.

3.2 Interfacial Recombination

When charge-free interface recombination centers at the CdS/CIGS interface are added to the model, there is a qualitative change in the variation of voltage with band gap energy. V_{oc} and η are shown for the range of absorber band gaps (Fig. 3) for interface recombination velocities $v_{intf} = 0$, 0.0002, 0.002, 0.02, and 0.2 v_{th}. $v_{intf} = 0$ corresponds to the baseline in Fig. 2.

For negative CBOs, V_{oc} depends on the interface quality, but becomes independent of the absorber band gap. This is in good agreement with earlier results [2–4] that showed that for a constant absorber band gap V_{oc} decreases approximately at the same rate as the CBO and the analytical predictions of a band-gap independent open circuit voltage [9]. For the devices with negative CBO the dominating recombination current flows through the interface states and depends only on the electron and hole density at the interface. With $v_{intf} = 0.02$ v_{th},

the highest efficiency is only slightly reduced to 17% with a band gap of 1.25 eV, but the range of high efficiency results (16 – 17%) is limited to band gaps (1.15 – 1.35 eV) that have a positive band offset. J_{sc} and FF results are unchanged except that no FF reduction occurs for large negative CBO since the cliff barrier is ineffective when the dominating current flows through the interface. The case with $v_{intf} = 0.02\ v_{th}$ is the starting point for the calculations discussed in following sections and will be referred to as the interface-baseline (IF-BL).

3.3 Alternative Windows

Considerable current may be lost due to absorption in a CdS window layer. In addition, the above results imply that a favorable band alignment is necessary to achieve high open circuit voltages. A possible solution for larger band-gap CIGS is alternative window or buffer materials such as Zn(O,S) compounds that have larger band gaps and a more optimal CBO. For Zn(O,S) the CBO should increase with S content according to theoretical studies [19]. Experimental efficiency of 18.6% has been demonstrated [20], which is very promising for future work.

To evaluate the potential of alternative windows, the calculations for the same band gap range are repeated starting from a *modified* IF-BL that has an alternative window layer instead of the standard ZnO-CdS. The window layer is assumed to have characteristics similar to ZnO (n^+, E_g ~ 3 eV). The window/absorber band alignment is set to be +0.9 eV, +0.6 eV, +0.3 eV (IF-BL), or 0 eV, respectively, for the 1.15 eV absorber material in each case and will track the absorber band gap. The larger offsets are a more favorable match for higher band-gap absorbers. The V_{oc} and η results are shown in Fig. 4. For window layers that create larger offsets, the limitation on voltage occurs at progressively higher voltages. This allows device efficiencies greater than 18% in the range from 1.15 eV to 1.75 eV absorber band gap, covering almost the complete $Cu(In,Ga)Se_2$ range. Large spike barriers (CBO > 0.4 – 0.5 eV) cause the sharp efficiency drop on the lower band-gap side for high-offset models. Calculations assuming a fixed band offset of +0.2 eV for all band-gap materials form an

envelope of the previous results (thick line in Fig. 4 (b)). The highest efficiency in this envelope is 20.2%, which occurs near 1.45 eV.

The highest experimental efficiencies for CdS/CIS, CdS/CIGS, CdS/CGS, and CdS/CdTe solar cells are shown for comparison with the modeling calculations (open squares). Except for the CdS/CGS solar cell, the record efficiencies all lie on the +0.3 eV curve, which was used as the CBO in the previous calculations for the CdS/CIGS band offset. For the CdS/CGS system, efficiencies up to 14% are predicted, if a CGS film with comparable quality to CIS films can be grown. An alternative window with an appropriate offset, increases the highest predicted CGS efficiency above 19%.

3.4 Near-Surface Absorber Phases

The band gap approaching the surface of a CIGS absorber is often different from the bulk. Typical examples are copper poor surface phases (i.e. $Cu(In,Ga)_3Se_5$, which shift the valence band downwards [21]) or intentional band-gap grading (i.e. increasing Ga/In ratio towards the junction, which shifts the conduction band upwards). Calculations were performed starting from the IF-BL assuming a surface phase that has (1) 100 nm thickness, (2) a band gap increased by $\Delta E = 0.1$, 0.2, or 0.3 eV in either the conduction or the valence band, (3) optical absorption shifted according to ΔE, and (4) otherwise the properties of the bulk material. J_{sc} and FF results are unchanged. V_{oc} for all band gaps is shown in Fig. 5 (a) for conduction band widening and 5 (b) for valence band widening. The results are nearly unaffected if the widening occurs in the conduction band. Valence band widening, however, leads to a depletion of holes at the interface that directly affects V_{oc}. It is apparent from these results that the hole concentration is the recombination-limiting parameter and V_{oc} is limited to such voltage where sufficient holes are supplied to the interface. This is in good agreement with the analytical findings that the valence band position at the interface determines the voltage limitation [9] and that holes are the minority carrier at the interface for a n^+p junction [22].

3.5 Fermi-Level Pinning

A sufficiently high number of charged defects at the CdS/CIGS interface (10^{14} cm^{-2} are used in the simulation) pin the Fermi level at the interface. These defects are introduced with very small capture cross sections to decouple pinning and recombination effects. Acceptor states at a fixed distance above the CIGS valence band (0 – 1 eV) were found to reduce the depletion width; the V_{oc} limitations always occur, and no overall efficiency gain was achieved. Donor states, however, can increase the depletion width and representative results are shown in Fig. 6. Donors a fixed distance above the CIGS valence band (shown in Fig. 6 for 1.4 eV above E_V) increase the inversion, reduce the hole concentration, and increase the V_{oc} limit by about 0.2 V. Donors a fixed distance below the CIGS conduction band (shown for 0.4 eV below E_C) couple the hole depletion to the band gap increase, and V_{oc} increases proportional to the band gap, but is slightly lower than for the interface-recombination free baseline (Fig. 2).

4 Conclusions

Inclusion of interface recombination in our model shows that the open circuit voltage has a limiting value independent of the absorber band gap for negative conduction-band offsets, in good agreement with a number of experiments. The voltage limitation should be addressable by appropriate matching of window and absorber to preserve a favorable offset. The voltage situation also improves if the band gap widens in the valence band towards the interface, or if pinning states increase the depletion width. Both clearly indicate that hole concentration is the limiting, voltage-modulated parameter that determines V_{oc}. Although details may change with variations in some parameters of calculations or experiments, for example the selection of ΔE_C = +0.3 eV for 1.15 eV CIGS, the basic concept of an upper limit for V_{oc} independent of E_g appears to be a general characteristic. The results are highly suggestive that the typical window/buffer layer materials for low band gap CIGS materials will not allow high device efficiencies for wide band gap CIGS. To overcome these

difficulties the exploration of alternative window materials or of CIGS surface modification is recommended.

5 Acknowledgments

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Figure Captions

Figure 1: Conduction and valence band for a small (a) and a large (b) band-gap ZnO/CdS/CIGS solar cell.

Figure 2: Simulated J-V parameters with increasing density of bulk recombination centers. Filled circles correspond to the baseline trap-density case with varying absorber band gap. CdS window is assumed.

Figure 3: Effects of interface recombination. Interface quality is parameterized as an approximate interface recombination velocity. The case with 0.02 v_{th} is used as basis for further investigations (IF-BL).

Figure 4: V_{oc} and η with different band alignments. The +0.3 eV curve corresponds to the CdS/CIGS interface baseline case (IF-BL). Details will vary with choice of parameters. Highest reported cell efficiencies (open squares) follow the predicted efficiencies.

Figure 5: Band gap is widened towards (a) the conduction band or (b) the valence band.

Figure 6: Pinning of the Fermi level by donor (D) interface states. The defect positions are a fixed distance above the valence band E_V or below the conduction band E_C.

Figures

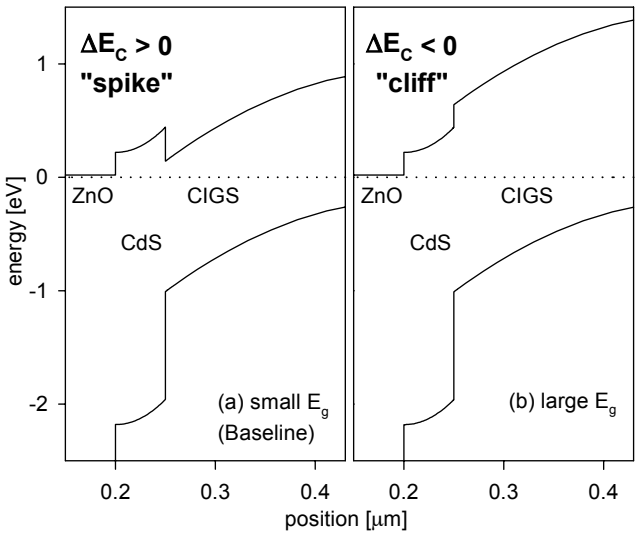
ΔE_C > 0
"spike"
ΔE_C < 0
"cliff"
ZnO
CIGS
CdS
ZnO
CIGS
CdS
(a) small E_g
(Baseline)
(b) large E_g
energy [eV]
position [μm]
1
0
-1
-2
0.2
0.3
0.4
0.2
0.3
0.4

Figure 1

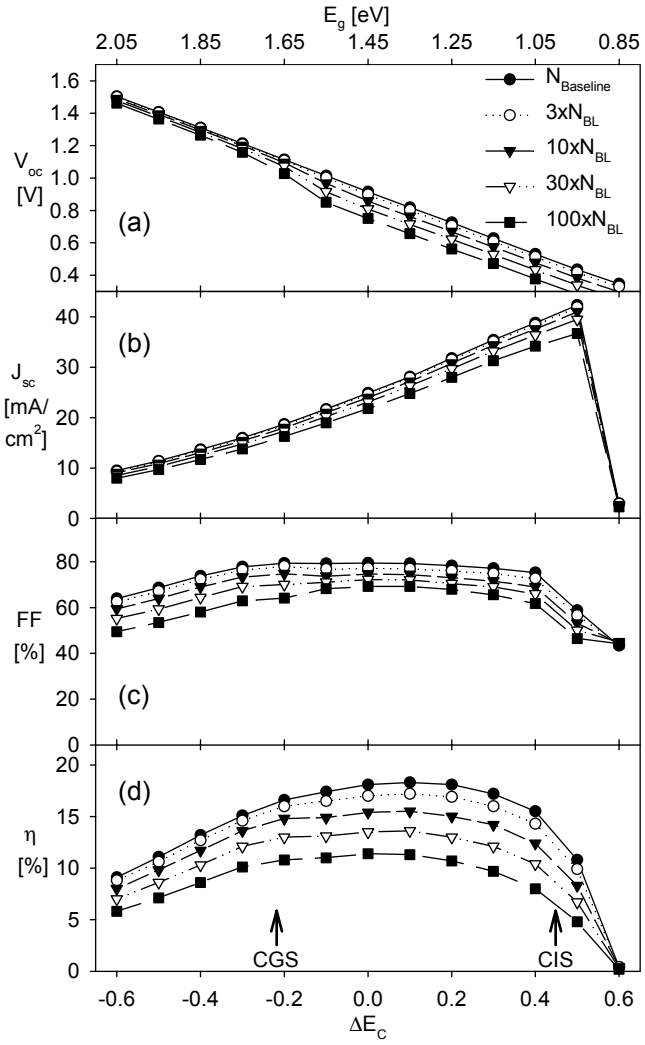
E_g [eV]
2.05
1.85
1.65
1.45
1.25
1.05
0.85
V_oc [V]
(a)
N_Baseline
3xN_BL
10xN_BL
30xN_BL
100xN_BL
J_sc [mA/cm^2]
(b)
FF [%]
(c)
η [%]
(d)
CGS
CIS
ΔE_C

Figure 2

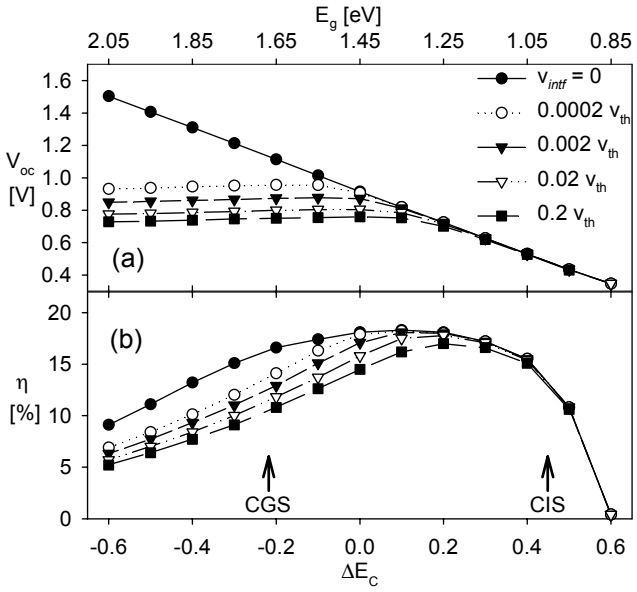
E_g [eV]
2.05
1.85
1.65
1.45
1.25
1.05
0.85
V_oc [V]
v_intf = 0
0.0002 v_th
0.002 v_th
0.02 v_th
0.2 v_th
(a)
(b)
η [%]
CGS
CIS
ΔE_C

Figure 3

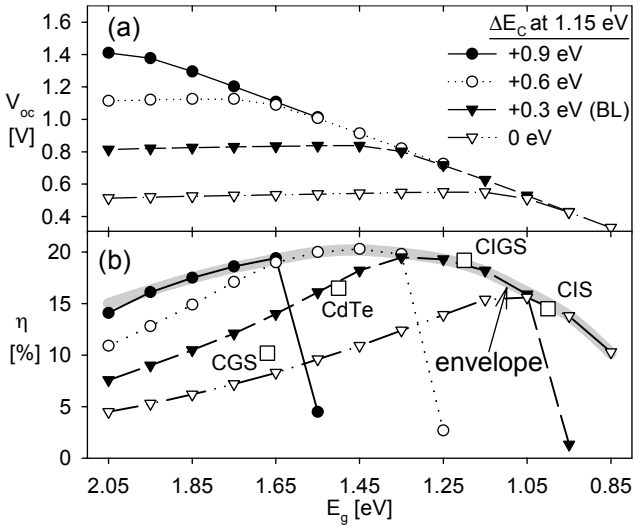
(a)
(b)
ΔE_C at 1.15 eV
+0.9 eV
+0.6 eV
+0.3 eV (BL)
0 eV
V_oc [V]
η [%]
CIGS
CIS
CdTe
CGS
envelope
E_g [eV]
2.05
1.85
1.65
1.45
1.25
1.05
0.85

Figure 4

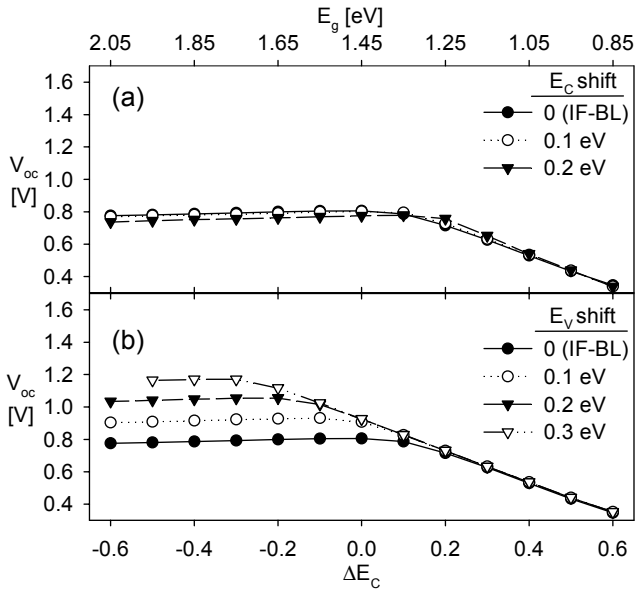
E_g [eV]
2.05
1.85
1.65
1.45
1.25
1.05
0.85
(a)
E_C shift
0 (IF-BL)
0.1 eV
0.2 eV
V_oc [V]
(b)
E_V shift
0 (IF-BL)
0.1 eV
0.2 eV
0.3 eV
ΔE_C

Figure 5

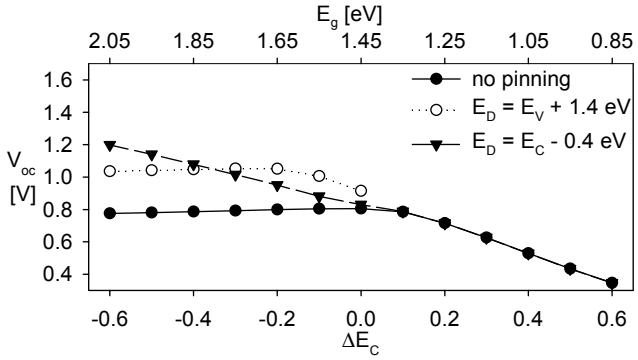
E_g [eV]
2.05
1.85
1.65
1.45
1.25
1.05
0.85
1.6
1.4
1.2
1.0
0.8
0.6
0.4
V_oc [V]
no pinning
E_D = E_V + 1.4 eV
E_D = E_C - 0.4 eV
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
ΔE_C

Figure 6