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Meso-/Micro-Optical System Interface Coupling Solutions

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Meso-/Micro-Optical System Interface Coupling Solutions

LDRD 67006 Final Report

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Abstract

Optoelectronic microsystems are more and more prevalent as researchers seek to increase transmission bandwidths, implement electrical isolation, enhance security, or take advantage of sensitive optical sensing methods. Board level photonic integration techniques continue to improve, but photonic microsystems and fiber interfaces remain problematic, especially upon size reduction.

Optical fiber is unmatched as a transmission medium for distances ranging from tens of centimeters to kilometers. The difficulty with using optical fiber is the small size of the core (approximately 9 μm for the core of single mode telecommunications fiber) and the tight requirement on spot size and input numerical aperture (NA). Coupling to devices such as vertical cavity emitting lasers (VCSELs) and photodetectors presents further difficulties since these elements work in a plane orthogonal to the electronics board and typically require additional optics. This leads to the need for a packaging solution that can incorporate dissimilar materials while maintaining the tight alignment tolerances required by the optics.

Over the course of this LDRD project, we have examined the capabilities of components such as VCSELs and photodetectors for high-speed operation and investigated the alignment tolerances required by the optical system. A solder reflow process has been developed to help fulfill these packaging requirements and the results of that work are presented here.

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Introduction

Optoelectronic microsystems are more and more prevalent as researchers seek to increase transmission bandwidths, implement electrical isolation, enhance security, or take advantage of sensitive optical sensing methods. Board level photonic integration techniques continue to improve, but photonic microsystems and fiber interfaces remain problematic, especially upon size reduction. The challenge of coupling a chip or board level photonic microsystem to off board photonic interconnects exists due to the large mismatch between the chip domain and longer distance photonic circuits. Specifically, optical fiber is an excellent solution for photonic interconnects where distances range from tens of centimeters to kilometers. Its extremely low loss and superior signal characteristics cannot be matched by any other transmission medium; unfortunately, optical fiber can be difficult to couple to the required optoelectronics.

While the single mode optical fiber core is small (approximately 9 μm core), it is encased within a large, 125 μm diameter, cladding that cannot be stripped away. Mechanically the apparent size of fiber is 125 μm; however, the actual target is less than one-tenth this size at the center of the fiber. The fiber core emits and accepts light only within its numerical aperture (NA). Efforts to modify this axial configuration by angle polishing the endface or evanescently coupling light through the cladding remain so inefficient and of low tolerance as to be impractical on a standard process scale. At the board level, photonic components including VCSELs and photodetectors present further challenges. Both of these components are surface-normal devices that couple light in a plane orthogonal to the electronics board. For close board-to-board spacing and better mechanical stability, fiber generally lies along the board plane leading to the need for a coupling solution that can provide a ninety-degree turn. This translates into a minimum 125 μm free space propagation distance from the photonic component to the fiber endface. The result is a spot size mismatch loss of approximately 14 dB. To mitigate this “configuration mismatch” and spot size mismatch, optical elements are typically added to increase the overall efficiency.

The inclusion of optical components leads to two complications. First, the materials used for optical components differ significantly in their electrical characteristics from the electrical components and board materials. Electrical transmissions lines may need to be routed across these differing materials and the packaging system will need to be able to accommodate this change. Additionally, the optics require precise and consistent alignment. Allowable misalignments can be less than 0.5 μm for some applications. One of the goals of this LDRD is to develop a self-aligning process for both photonic and electrical components that will ensure the necessary precise and consistent device positioning. Development of a process such as flip-chip C4, controlled collapse chip connection [1], for the mismatched materials is a significant deviation from industry practice.

The original goal of this LDRD was to develop a packaging process that was capable of joining dissimilar materials while providing good optical alignment and high speed electrical connections. This effort was to culminate in a technology demonstration at the end of the third year; however, the program has been ended after the second. An investigation of the ability of common optical and electrical materials to provide high speed electrical transmission lines has been done as well as the simulation and testing of current optoelectronic components. The

results of this work will be presented in the next section. Additionally, a low temperature solder reflow self-alignment process has been demonstrated. Indium tin solder was investigated because its low eutectic temperature of 118 ºC was attractive for joining dissimilar materials. The lower process temperature would reduce the stress induced due to mismatched thermal expansion coefficients. Also, indium tin is fairly ductile and would therefore withstand material stress better than more brittle alloys. The results of this development will be given in the subsequent sections.

High Speed Electrical Models and Measurements

The final demonstration planned for the third year was a high-speed photonic link utilizing the self-alignment process developed earlier in the program. A substantial amount of work was done on the preliminary electrical design including the measurement and modeling of high-speed lasers and detectors. In addition, transmission line models were developed to help design the electrical interconnections that would be routed across multiple materials. This section summarizes the various measurements performed and the models developed.

Vertical Cavity Surface Emitting Lasers (VCSELs) offer several advantages over conventional edge-emitting lasers for data communications and/or analog-microwave optical links. Most notably, due to their surface emitting nature, VCSELs are fabricated by low-cost standard microelectronic methods and do not require cleaved facets. This simple fabrication allows for 2-dimensional laser arrays, which offer the possibility of spatial signal multiplexing for increased aggregate optical link bandwidth. VCSELs fabricated at Sandia have demonstrated wall-plug efficiencies as high as 50% and modulation bandwidths in excess of 20 GHz. These large efficiencies are due to the recent advances of alloy-graded mirrors and selective mirror oxidation. As indicated by the large intrinsic bandwidths of VCSELs, future modulation bandwidths can be expected to considerably increase. Present commercial sources of VCSELs are primarily focused on one to several Gbps data communication applications at 850 nm (suitable for plastic fibers). In the future, devices with much larger bandwidths will become commercially available if applications are developed. Figure 1 shows the VCSEL input impedance at 2, 4, 8, and 10 mA of current, and one can see that the input resistance is lower at the higher current.

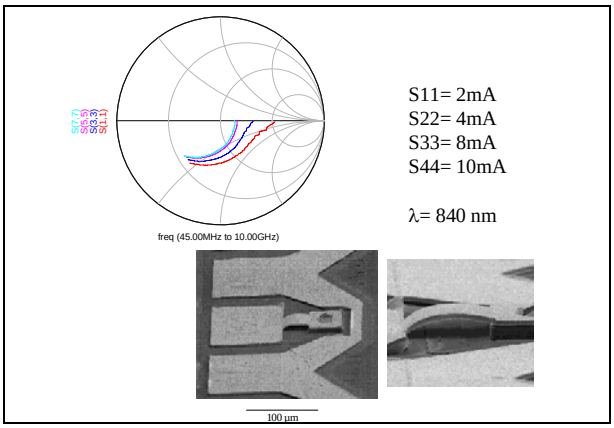

Figure 1. Sandia VCSEL input impedance plot at different bias conditions.

VCSELs are attractive sources for high speed data applications, particularly those with growing bandwidth requirements and the reason chosen for characterization in this study. Fundamentally, the high finesse and small active volume of VCSELs promotes high photon densities without excessive photon lifetimes and hence the potential for high speed operation. Experiments have demonstrated intrinsic relaxation oscillation frequencies as high as 71 GHz in VCSELs. However, the practical modulation frequency of VCSELs has been limited by parasitics, such as excessive resistance, capacitance and thermal heating. We have previously demonstrated small signal modulation up to 21 GHz, and large signal modulation rate up to 12 Gbit/sec. This performance was achieved using selectively oxidized VCSELs with implanted regions around the active region to reduce the device capacitance. Figure 2 shows the bandwidth of devices used for this study as a function of bias. It shows that the bandwidth increases from 8 GHz to 12 GHz as the VCSEL bias current increases from 2 to 10 mA.

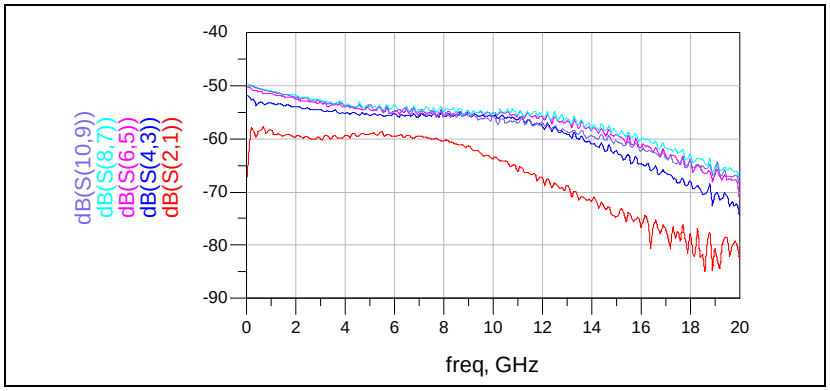

Figure 2. VCSEL Bandwidth at 2, 4, 8, & 10mA

Representative light and voltage versus current (LIV) curves for a 5x5 µm oxide aperture selectively oxidized VCSEL fabricated for this project were also done. The threshold current (voltage) is approximately 1.85 mA (1.75 V) with 9.4 mW maximum output power. In Figure 3 a circuit model of the VCSEL was generated from the S11 measurements at 8 mA of current. This model can be used to design high-speed optical interconnects to determine the expected system properties.

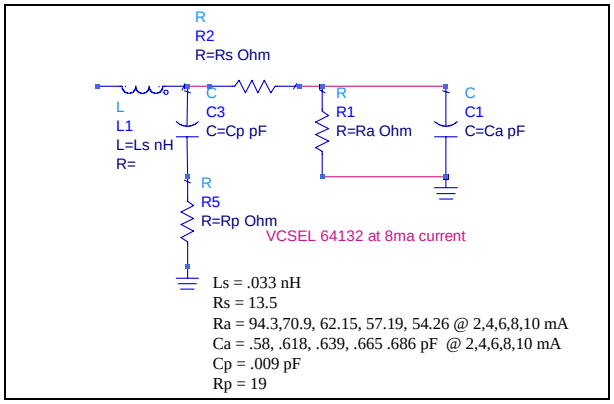

Figure 3. VCSEL circuit model at 8 mA of current

In Figure 4, the two models shown were generated at 2 mA (top model) and 10 mA (bottom model) of current bias. The model and simulation shows the diode resistance going from 94 ohms to 54 ohms as the current increases from 2mA to 8mA.

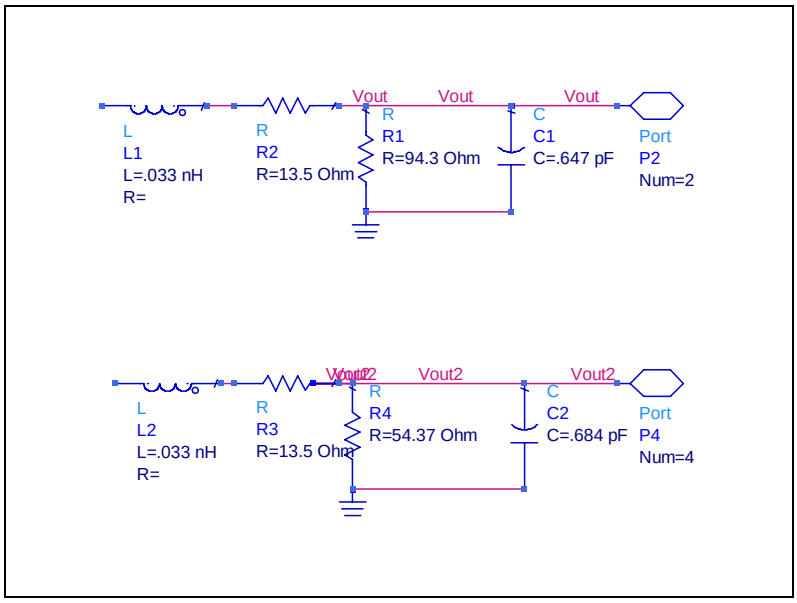

Figure 4. Top model at 2 mA and bottom model at 1 mA of bias current

Figure 5 shows the transient response using the Advance Design System (ADS) from Agilent and the model that was developed for the VCSEL, analysis shows the pulse rise time and fall times which are in good agreement with measured response and shown in Figure 6. The rise time and fall times were measured to be about 111 ps.

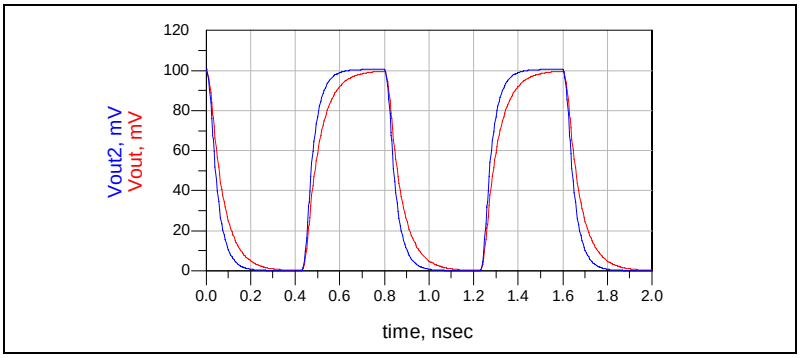

Figure 5. Transient simulation of VCSELS bias at 2mA (red) & 10 mA (blue)

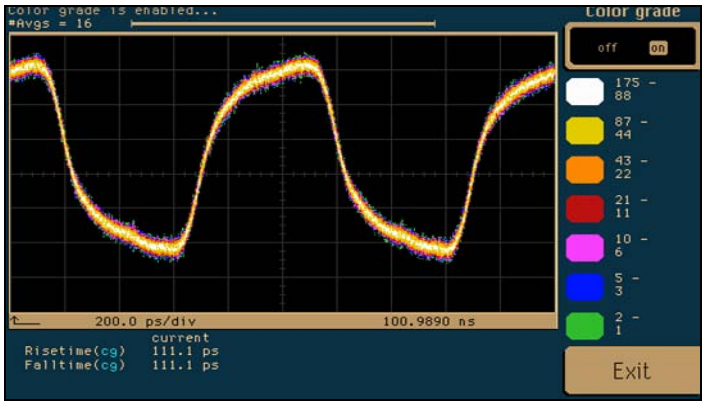

Figure 6. Pulse shape of a VCSEL biased at 6 mA

As part of the optical receiver that will complement this VCSEL a high-speed detector from Optolynx was characterized and modeled. The lump circuit equivalent model is shown in Figure 7 and the impedance plot of the measured and modeled circuit is shown in Figure 8.

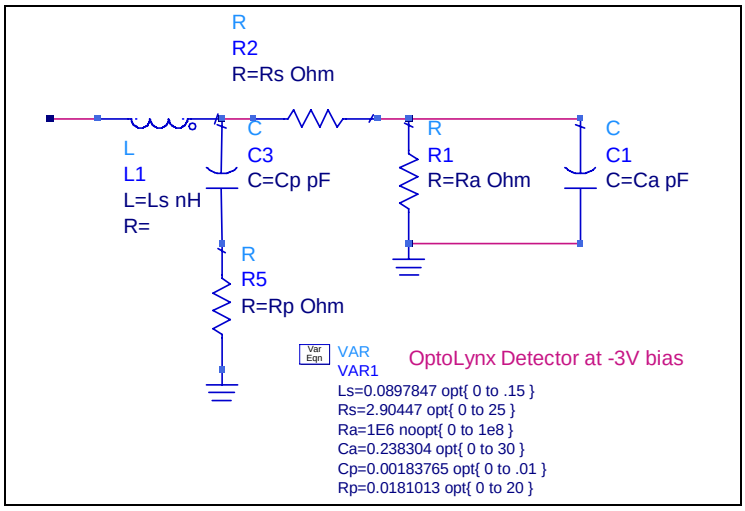

Figure 7. Circuit model of Optolynx high-speed detector

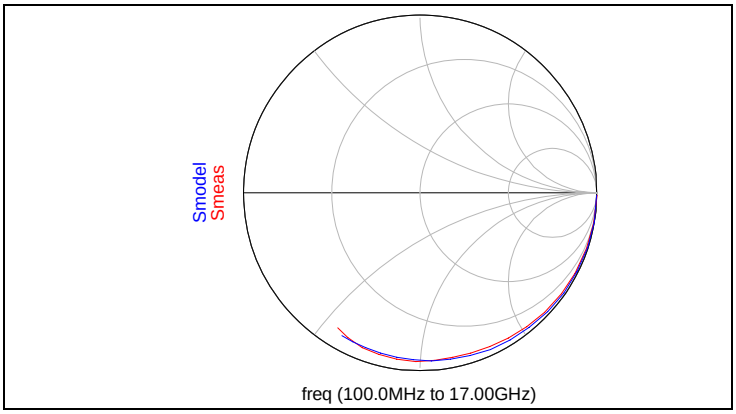

Figure 8. Measured and modeled input impedance of Optolynx detector

As part of this study, high-speed differential transmission lines on various substrates were analyzed using ADS. This will enable us to select substrates that can be used for this optical platform. The transmission line circuit description is shown in Figure 9 and the results using the various substrates are shown in Figure 10. It shows that all the various substrates can be used for the 10Gbps using the same mask set. The mask set was designed for fused silica, which is our first choice. Once the substrate material is chosen, the transmission lines can be optimized.

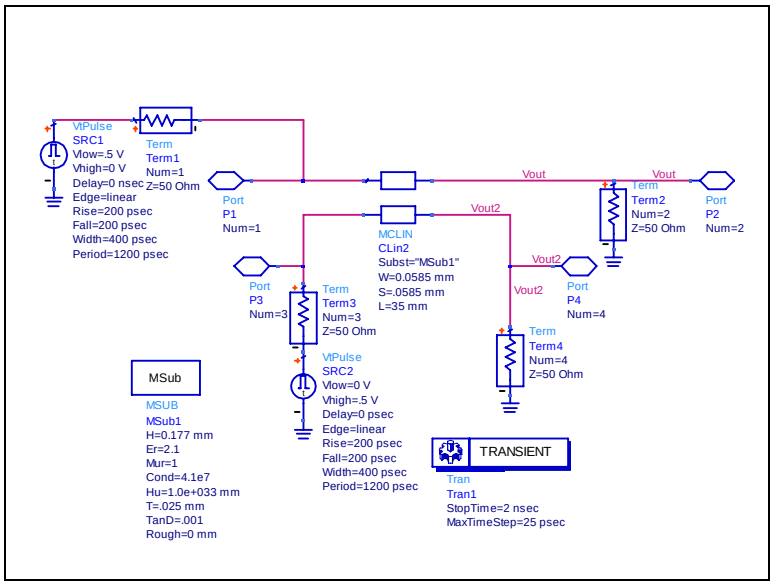

Figure 9. ADS simulation for differential transmission lines

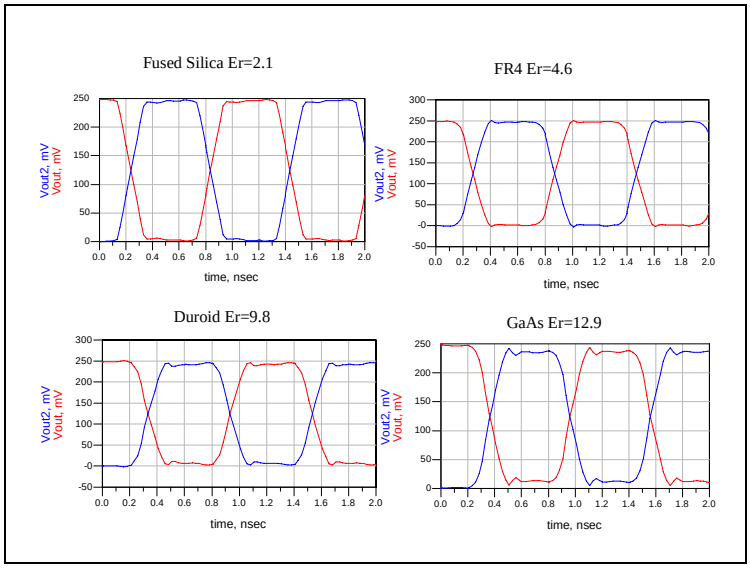

Figure 10. Simulation of transmission lines for various substrates

High-speed VCSELs and detector were characterized and modeled for insertion into possible designs of this study. In addition, high-speed interconnect microwave structures to launch to

photonic components were also designed. Microstrip and coplanar designs could accommodate either flip-chip or regular chip configurations. Subsequently, the preliminary optical, electrical, and mechanical tasks may be performed in parallel. These include a comparison survey of possible solder, self-align process scenarios, and simulation of the mechanical effectiveness of each process.

Optical Alignment Requirements

The required alignment accuracy the solder reflow process needs to achieve had to be quantified before beginning that development. A typical micro-optical system was modeled and its tolerances analyzed to provide appropriate guidelines. The results of this analysis are presented here.

We ran ray trace simulations to predict the expected optical coupling from an optical source, through a simple lens, and into a detector. The source had a numerical aperture of 0.14 to represent a singlemode fiber input. The detector aperture diameter was 40 microns, which is a typical aperture for a 10 GHz, high-speed detector. The other design distances are shown on Figure 11: source distance in air = 800 microns, fused silica thickness = 1mm and detector distance in air = 50 microns. This last thickness is a nominal glue line thickness.

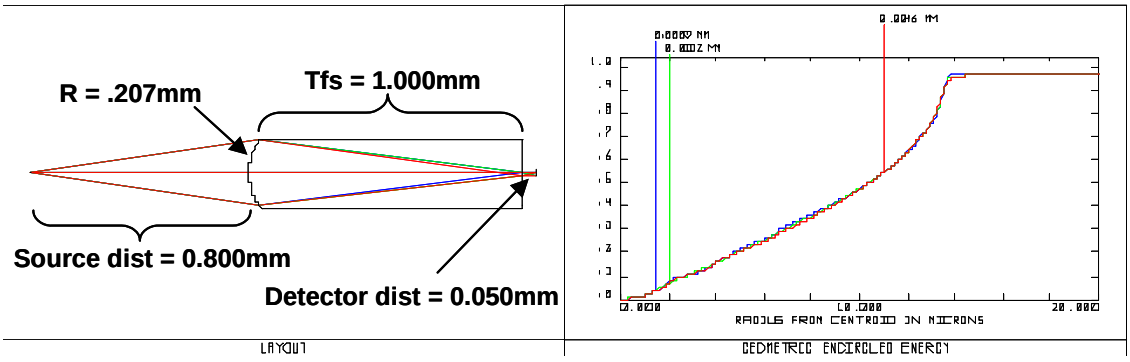

Figure 11. Optical ray tracing layout for optical coupling and tolerance simulations.

The following figures illustrate the required tolerances for this lens design. These allowed ranges were based upon optical throughput of an apertured spot at the detector. The targeted spot size of 48 microns is indicated by the red, dotted box. From Figure 12, the allowed range for the lens radius of curvature is 202-218 microns and that for the source distance in air is 719 microns to at least 850 microns. Both of these are within reasonable fabrication tolerances. From Figure 13, the fused silica thickness can range from 870-1070 microns and the detector distance in air may range from 0 to 93 microns. Again, these targets are relatively straightforward to achieve. Figure 14 shows the most challenging aspect of optical placement: the lens lateral decenter away from the optical axis and the lens element tilt and/or face tilt on the substrate. Here the lateral decenter must stay within 5 microns and the tilt within 2 degrees to maintain 95% efficiency.

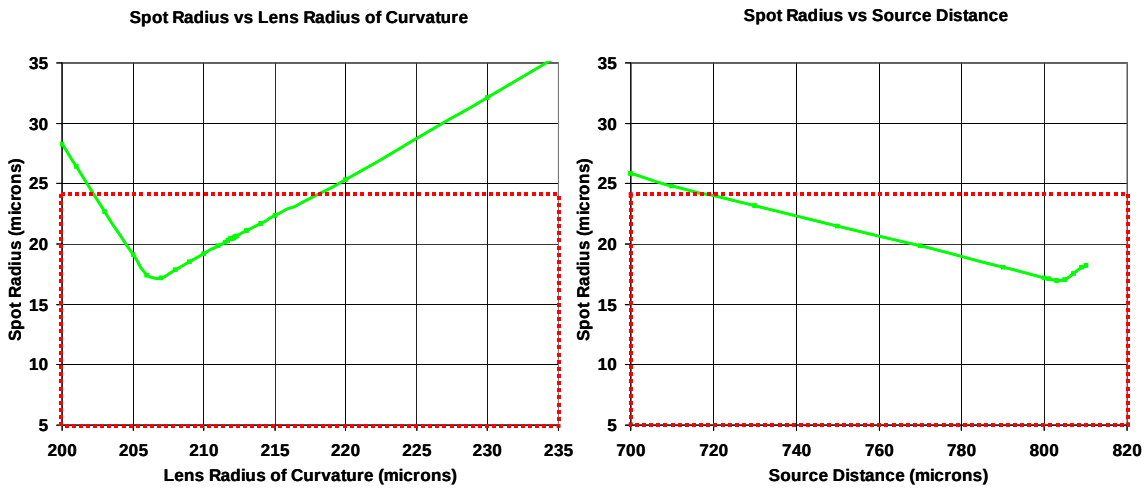

Figure 12. Allowed tolerance ranges for the lens radius of curvature and the source distance.

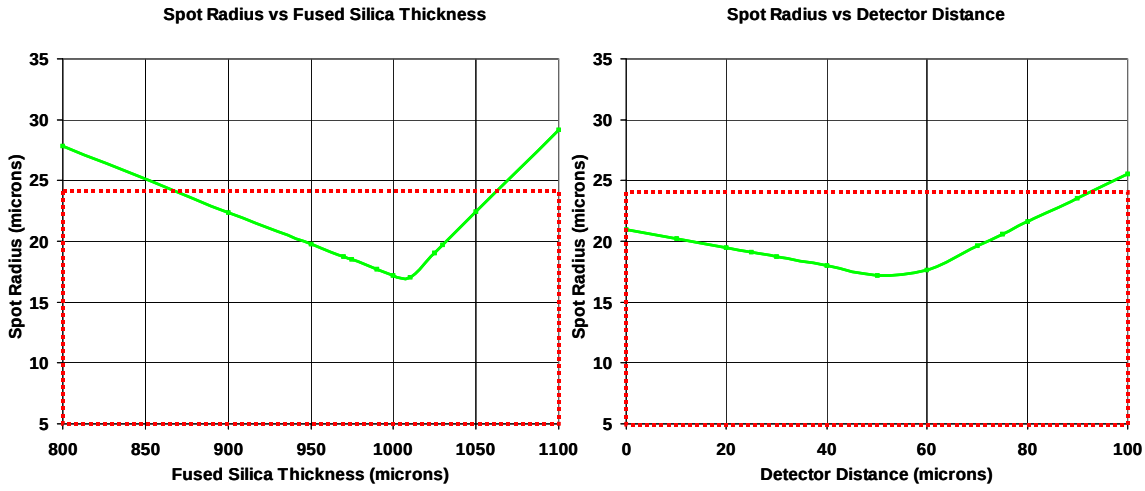

Figure 13. Allowed tolerance ranges for the fused silica thickness and the detector distance in air.

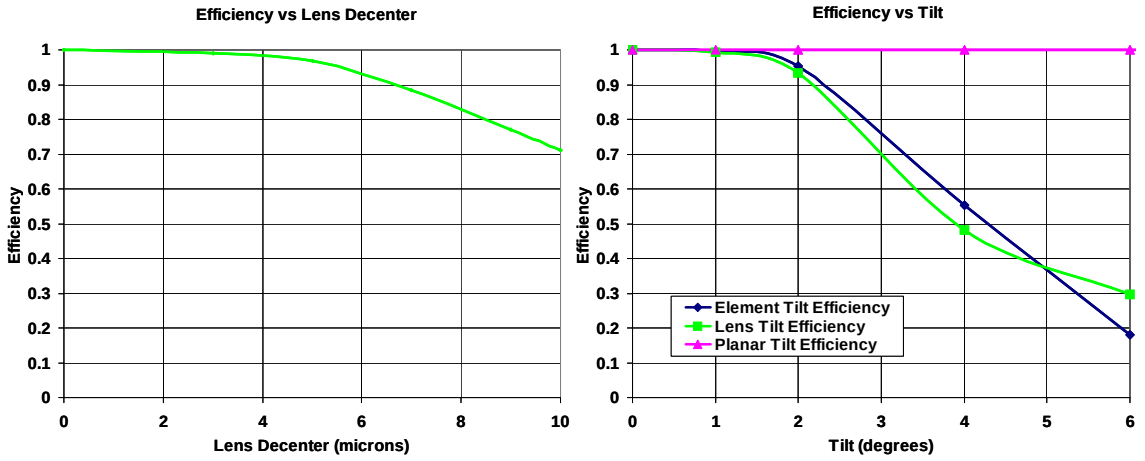

Figure 14. Reduced optical throughput as a function of lens lateral decenter and lens and surface tilt.

Solder Reflow Simulation

Simulations were done assuming thick electroplated solder. For this initial series of experiments, a nominal 75 μm ball height was assumed. A surface evolution for these dimensions is shown in Figure 15, below. The model predicted a solder volume of 5 x 10^{-7} cm^3 assuming 460 dyne/cm surface tension and 1 g of gravitational normal force.

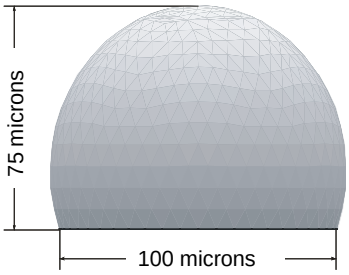

Figure 15. Surface evolution of a 75 μm high solder ball on a 100 μm diameter pad.

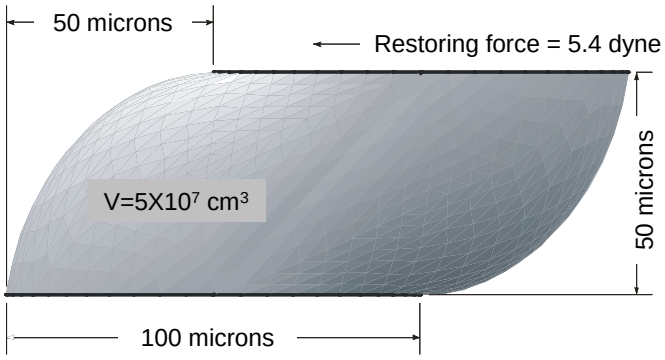

Figure 16. Surface evolution calculation of restoring force for case of ½ bondpad misalignment (50 μm).

Figure 16 shows expected surface deformation and restoring force for a maximum misalignment of 50 μm (half bondpad). The total restoring force is the sum of individual forces arising from each solder ball, in this example ~300 dyne or about 3 mN. The restoring force increases with misalignment along with the equilibrium gap height up to about 25 μm of offset. Restoring force continues to increase after 25 μm in this simulation, but the equilibrium gap height begins to decrease. At some point the column will collapse. A general rule of thumb for maximum offset is less than half the bondpad diameter. A graph of restoring force and gap height for the conditions cited above are contained in Figure 17.

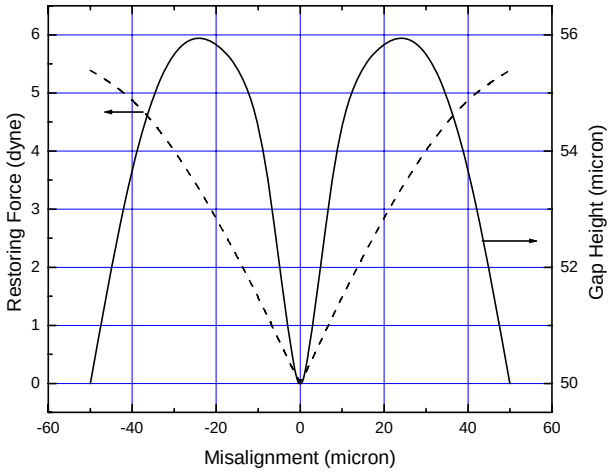

Figure 17. Plot of restoring force and equilibrium gap height as a function of horizontal offset for a single solder ball connecting two 100 μm diameter pads and volume = 5 x 10^{-7} cm^3. This simulation was performed using Surface Evolver.

These simulations indicate that the solder reflow should provide adequate force to properly align two die with tall solder bumps. Shorter bumps were also investigated experimentally and it has been shown that for a given pad size, reduced solder volume will actually increase the restoring force per joint [2].

Test Die for Solder Experimental Development

To aid in the development of the solder self-alignment process, a test die was designed to provide alignment aids and verniers for evaluating the success of the process as well as several pad designs. A 4x4 mm die size was chosen to allow for ease of handling while still allowing for a large number of devices per wafer. Four different pad layouts were used. Each pad layout was a peripheral pattern with the pitch and sizes of the pads varied as shown in Table 1.

Design	Diameter [μm]	Pitch [μm]	#	Total Area [μm^2]
A	50	100	140	274889
B	100	250	56	439823
C	150	350	40	706858
D	100	350	40	314159

Table 1. Different pad designs used to evaluate solder process.

In addition to the peripheral pads, several alignment fiducials were added to the test die. Linear and circular Moiré patterns were added as well as verniers in each corner. A larger set of verniers provided misalignment measurement accuracy of 1 μm while a smaller set could provide accuracies of 0.2 μm. Figure 18 shows the overall die layout and Figure 19 shows a close up of the Moiré patterns and verniers.

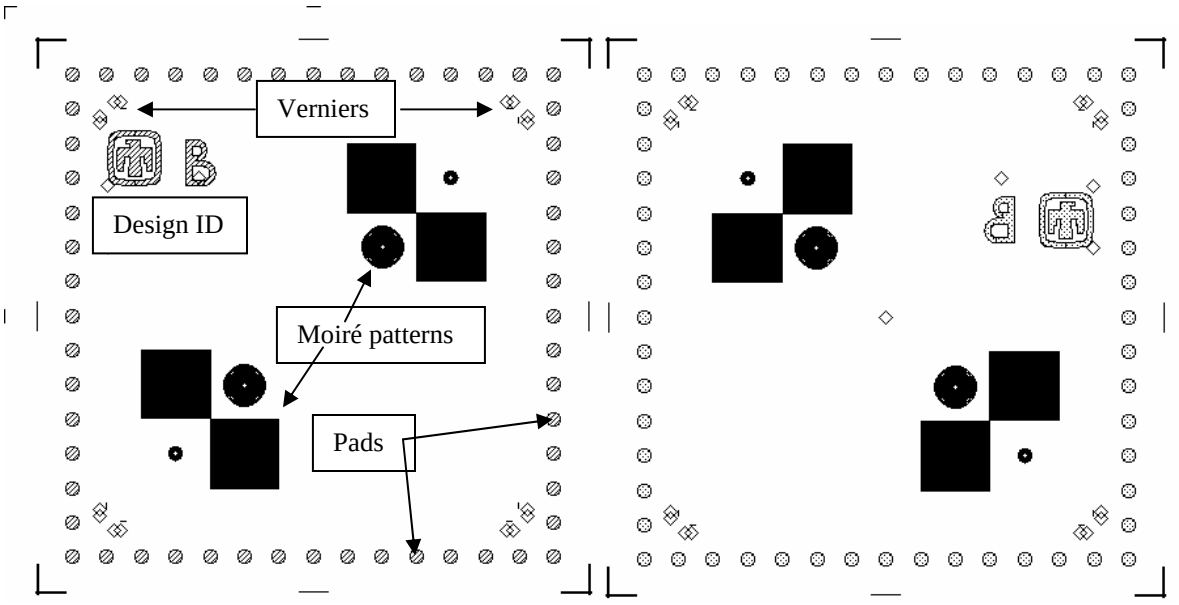

Figure 18. Layout of silicon (left) and fused silica (right) test die.

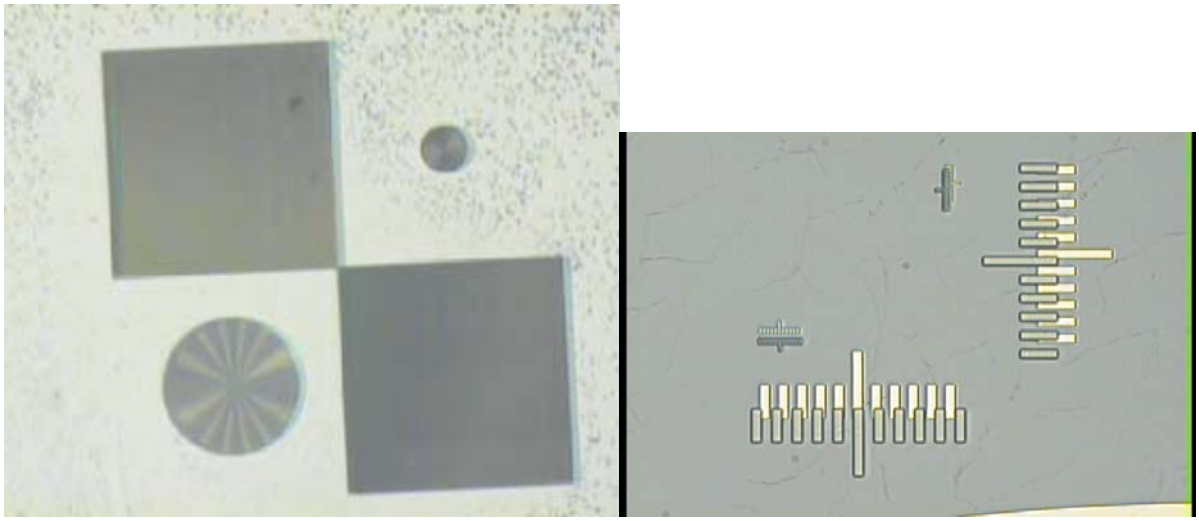

Figure 19. Closeup of Moiré patterns (left) show fringes in circular pattern due to large lateral offset between the silicon and fused silica die. The angular alignment is good enough so that only a single fringe is visible in the upper left linear Moiré pattern. The verniers (right) show a lateral displacement of approximately 4 μm in the vertical direction and 1 μm in the horizontal. At higher magnification, the smaller verniers can be used for a better measurement.

Solder Deposition

Four different solder deposition methods were investigated in an effort to find a process that could provide the necessary volume control for the desired alignment tolerances. The four deposition methods were electroplating, screen printing, jetting deposition and vacuum evaporation. A summary of the results for each method are presented below.

Electroplating

We pursued the development of an electroplating process for eutectic indium tin solder with Surfect, Inc. (Albuquerque, NM) as a means for obtaining tall solder bumps with good volume uniformity. Solder bumps with a height of 75µm and volume variation less than 5% were the initial targets. These geometric parameters would provide the proper angular alignment (< 0.5º) and the restoring force would be adequate to align the two die within 5µm. Initially, the solder bumps formed on test wafers had little or no adhesion after a single reflow cycle. The under bump metallization (UBM) used did not include a diffusion barrier between the adhesion and wetting layers. Fortunately, there were enough bumps formed to evaluate the other aspects of the process.

A thick photoresist process is necessary to help pattern the electroplated solder and provide good volume control. The process used in this first trial (supplied by a subcontractor to Surfect) did not provide fully opened holes over the UBM pads due to underdeveloped photoresist. This resulted in non-uniform plating and, in some cases, no plating at all. Figure 20 shows an SEM of several bumps on a silicon test wafer after the photoresist was removed and a single reflow cycle was performed.

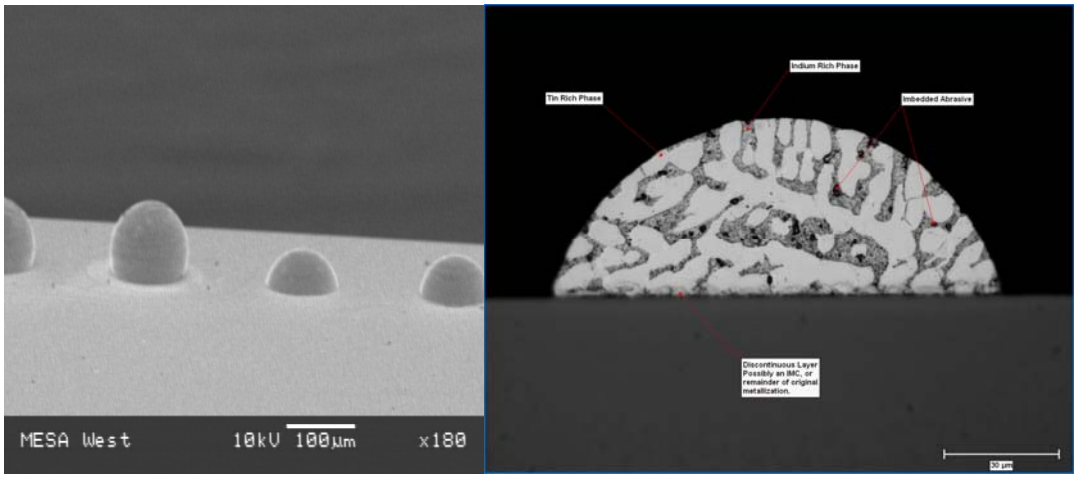

Figure 20. SEM of InSn solder bumps formed on silicon test wafer using electroplating (left) and cross-section of individual bump (right).

Surfect successfully developed the process for plating InSn solder with a eutectic stochiometry. Differential scanning calorimetry (DSC) verifies the eutectic temperature of 118ºC and estimates of the volume ratio from cross-sections verify a eutectic composition, see Figure 20.

Time and cost constraints did not allow for a subsequent electroplating trial and the available samples could not be used for any reflow experiments due to the large volume variations and lack of adhesion to the substrate.

Screen Printing

Screen printing processes use a stencil to lay down solder paste over the UBM pads on a substrate. The solder paste contains the desired alloy with an appropriate flux incorporated in the paste. The thicknesses for the printed bumps are comparable to thicknesses available using electroplating. The drawbacks include limitations on pad size and pitch. The thickness of the stencil and the particle size of the paste are the main factors limiting the pad designs.

For indium tin solder, available pastes have particles with sizes of 25 - 50 μm. This leads to a required stencil thickness of at least 100 μm. In order to achieve good release of the stencil after printing (and good bump uniformity), the aspect ratio of openings in the stencil should be twice the thickness of the stencil. This leads to a minimum pad size of 200 μm – smaller than the pads on the test die used in this study. Pastes with finer particle sizes are available, e.g. bismuth tin, but not with indium tin. The indium tin solder does not reflow well if the particles in the paste are smaller then 25 μm and leads to inconsistent bump geometry. Screen printed indium tin bumps were attempted with a finer paste; however, the resulting sample exhibited the nonuniform bump geometry expected.

Jet Deposition

Jetting deposition uses molten solder forced through a nozzle to coat a wafer with the desired alloy. This process has the advantage of using a predetermined alloy composition and a relatively cool process temperature at the substrate. Before deposition, photoresist is patterned on the wafer providing openings over the pads. After deposition, the photoresist is removed leaving patterned solder ("lift-off" process). The process is capable of forming solder heights up to approximately 20 μm.

Several wafers were processed by Jet Process Corp. (North Haven, CT) providing eutectic indium tin and a thin overcoating of gold to help inhibit oxide formation on the surface of the solder. The jet vapor process provided solder with a thickness of 8 – 15 μm over the entire surface of several 4" round wafers. The overall quality of the solder film is shown in Figure 21 and exhibited substantial roughness; however, the roughness was substantially finer that the pad sizes and did not present difficulties during reflow.

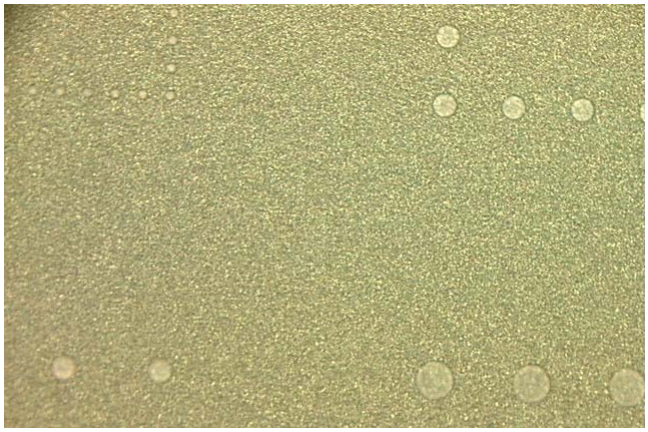

Figure 21. Center of wafer with jet vapor deposited InSn solder before liftoff. Openings in photoresist are visible as well as roughness of solder.

In addition to the roughness, the deposition process had a tendency to deposit the solder in an isotropic fashion. This resulted in solder filling up the space underneath the undercut photoresist and leading to inconsistent lift off patterning. Figure 22 shows an image of patterned solder and peeling around the edge of the solder is clearly visible. One detrimental result was the loss of the 50 μm pads. The patterned photoresist had well defined openings (see Figure 21), but these openings expanded due to the undercut of the developed photoresist. This undercut resulted in the openings intersecting at the substrate level for the smallest pads. Since the solder deposition filled in below the undercut, it did not pattern into individual bumps for the small pad size, see Figure 22.

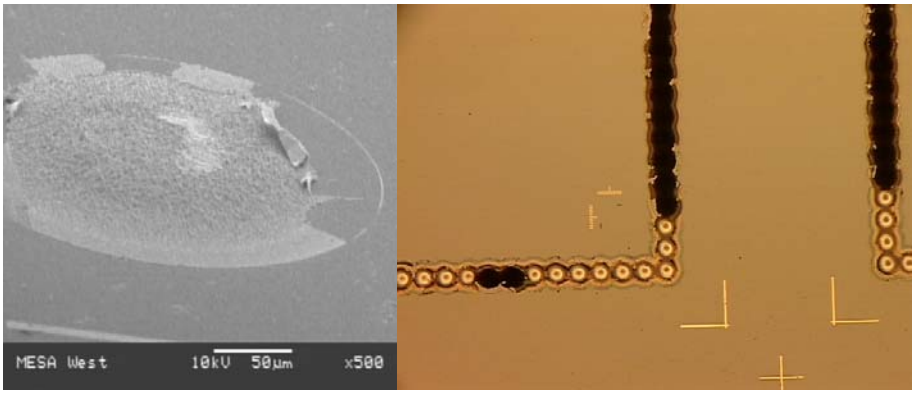

Figure 22. SEM image of patterned solder deposited using jet vapor process (left). Apparent peeling around edge is partially due to deposition method of solder. The small pads did not pattern properly due to the solder filling the space underneath the undercut photoresist(right).

The solder on several individual die were reflowed and the volume of the bumps was measured using a Wyko white light interferometer. Despite the inconsistent peeling after liftoff, the measured volume showed excellent uniformity as shown in Table 2.

Pad Diameter [μm]	Samples	Mean Volume [μm^3]	Standard Deviation
100	40	35858	2711
150	120	97554	4710
100 – extra solder	40	85736	3768

Table 2. Uniformity of jet vapor deposited solder bumps.

Evaporation

The final deposition process used was vacuum evaporation of alternating layers of indium and tin. This work was done at Sandia at the Advanced Manufacturing facility (AMPL) by the Thin Film, Vacuum and Packaging Department. Using the same photoresist process used with the jet vapor deposition, solder was successfully patterned on several wafers. In contrast to the jet vapor deposition, the evaporated solder exhibited a more anisotropic deposition and resulted in a more consistent patterning. Even the smallest, 50 μm, pads were properly patterned using this deposition method, see Figure 23.

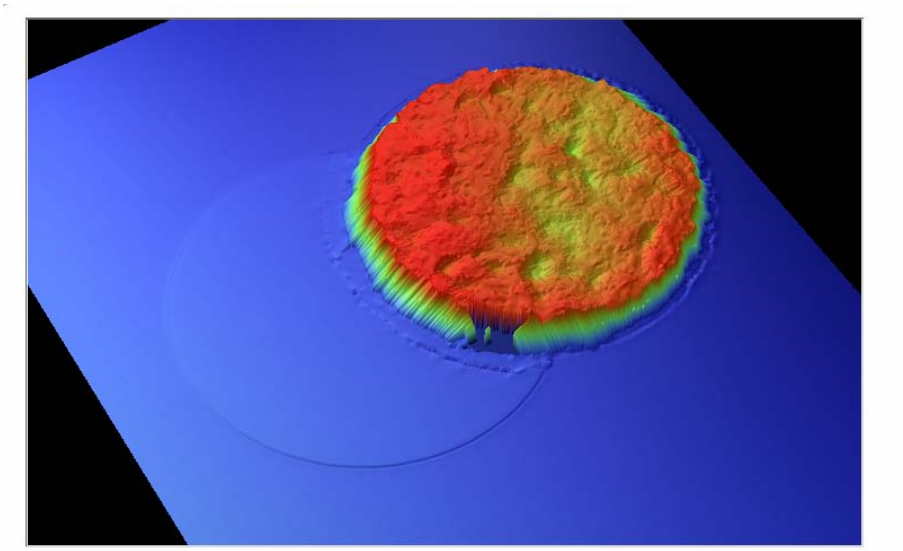

Figure 23. Two-dimensional profile of evaporated solder taken using white light interferometer. The shallow circle to the left of the solder is the UBM for the 50 μm diameter pad.

The volume of the evaporated solder bumps was also measured and the volume again showed excellent uniformity, see Table 3.

Pad Diameter [μm]	Samples	Mean Volume [μm3]	Standard Deviation
50	20	13021	1136
100	16	56329	1380
150	16	85113	3324

Table 3. Measured volume of evaporated solder bumps.

Solder Reflow Processing and Self Alignment

The original goals of the program included the development of a bonding technique that would provide for passive alignment of components at a low temperature without the need for a flux. The ability of solder reflow to provide self alignment of components lead to the pursuit of a viable solder process. Past work on self-aligning processes have typically used lead based solders with melting points ranging from 183 ºC to 310 ºC [3]. Indium tin solder has a sufficiently low eutectic temperature, 118 ºC, to make it an attractive alternative material for joining dissimilar materials. Unfortunately, indium tends to form a resilient oxide layer that needs to be removed to allow good wetting (bonding) of the solder to the UBM pads. Experiments run using an evacuated furnace still required a temperature of 250 ºC to provide reflow of deposited indium tin solder indicating the presence of an oxide layer.

A common approach to solder reflow without flux is to use a gold tin alloy, 80Au20Sn. The gold does not oxidize readily and flux is not required for good bonding. Unfortunately, the eutectic temperature is 280 ºC, and this is often too high to accommodate optical and electrical materials. Fluxless bonding has been demonstrated with indium tin solder systems [4-7]. The processes detailed in these references had three main components. First, the deposited solder had a cap layer of gold or silver applied to inhibit oxidation of the underlying indium. We used gold cap layers with both the jet vapor deposited and evaporated solder trials. Second, the bonded parts were held together with 50- 85 psi of static pressure during bonding. Since we want to allow the parts to self-align, they cannot be held during reflow, at least one part must be allowed to move freely. Third, while no flux was used, the bonding was done in a forming gas, hydrogen rich, environment. We did not attempt bonding using forming gas, but did run trials using formic acid vapor in an effort to reduce any oxides that had developed.

Flux Based Reflow

As mentioned earlier, individual bumps were reflowed to facilitate volume measurements. This reflow was done using a water soluble organic acid flux, Superior Supersafe® No. 30 [8,9]. This reflow was done by manually applying flux to the die and heating the die on a hotplate set to 150 ºC for two minutes. This process provided consistent reflow of the solder bumps.

The flux based reflow process was then applied to the bonding of silicon and fused silica die. The solder was only deposited on the silicon and the fused silica die had UBM pads. The process that was finally developed used flux manually applied only to the edges of the die where the bond pads were located. The silicon die with flux was then placed on a hotplate at 80 – 90 ºC while the fused silica die was initially aligned. The fused silica die was placed using motor controlled stages and camera system with initial alignment accuracies ranges from a few microns up to 70 μm. Moiré patterns on the die provided easily visible fringe patterns to facilitate both lateral and rotational alignment. The hotplate temperature was then raised to 130 – 150 ºC. Reflow was observed at the eutectic temperature of 118 ºC. The success of these bonding

experiments will be discussed in the next section. The hotplate was then set back to 80 ºC and the parts were allowed to cool down to below the eutectic temperature of the solder.

Self Alignment Demonstration

Bonding experiments using die with jet vapor and evaporated solder were performed using the flux based process outlined above. Table 4 provides a summary of the alignment achieved with both solders and various pad sizes.

Deposition	Pad	#	Average Lateral Alignment		Average Rotational Alignment	
			Initial [μm]	Final [μm]	Initial [deg]	Final [deg]
Jet vapor	B	4	14.8	0.122	0.659	0.010
Jet vapor	C	5	32.0	0.271	0.442	0.004
Jet vapor	D	3	24.5	4.58	0.166	0.071
Evaporated	A	5	13.2	5.36	0.162	0.025
Evaporated	B	3	12.3	4.07	0.037	0.024
Evaporated	C	3	17.8	4.34	0.166	0.000
Evaporated	D	1	17.3	4.78	0.029	0.010

Table 4. Alignment accuracy achieved using flux based reflow process.

The best alignment was achieved with the jet vapor solder; however, this may be due to the overfilling of the pads by the jet vapor solder and the gross misalignment of the evaporated solder with the UBM pads on the silicon die. Figure 24 shows an example of jet vapor deposited solder which has been scratched to reveal the UBM pad underneath.

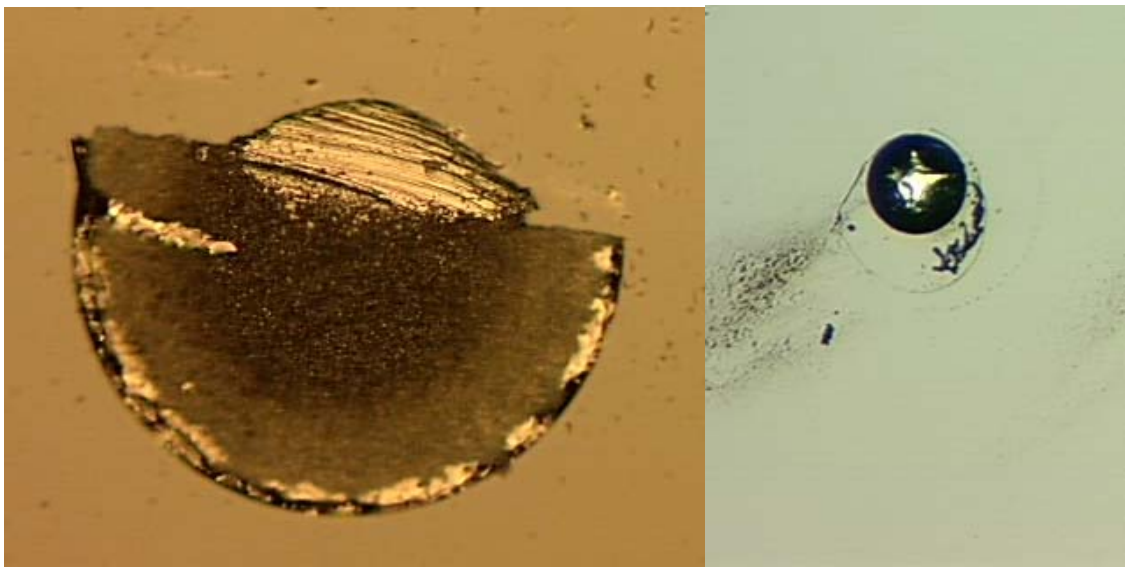

Figure 24. Jet deposited solder overfilled the UBM pads (left), but successfully wetted to the UBM upon reflow (right).

In contrast, the evaporated solder did not overfill the UBM and the die used for the self-alignment experiments had a large misalignment between the silicon UBM and solder. Figure 25 shows the initial alignment of the silicon and fused silica bond pads and the resulting alignment after reflow.

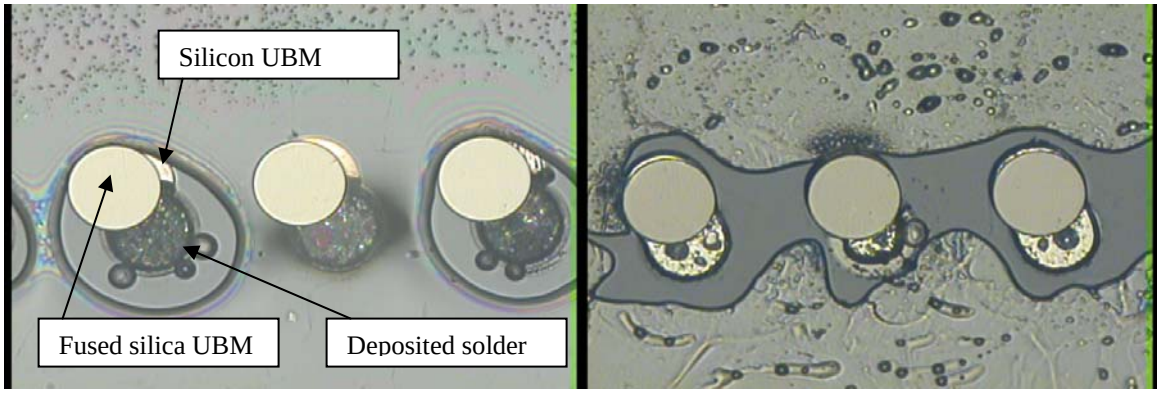

Figure 25. Initial alignment of 50 μm pads on silicon and fused silica die (left). The pad in the foreground is the UBM on the fused silica while the dark mottled circles are the deposited solder. A small section of the silicon UBM is visible as well. After reflow (right), the solder is no longer visible while an approximate 5 μm misalignment between the fused silica and silicon pads is visible.

For each die, the alignment was evaluated using the verniers patterned in the corners of the die. Figure 26 shows one set of verniers before and after reflow. Note that the initial image has significant flux residue that evaporates during reflow.

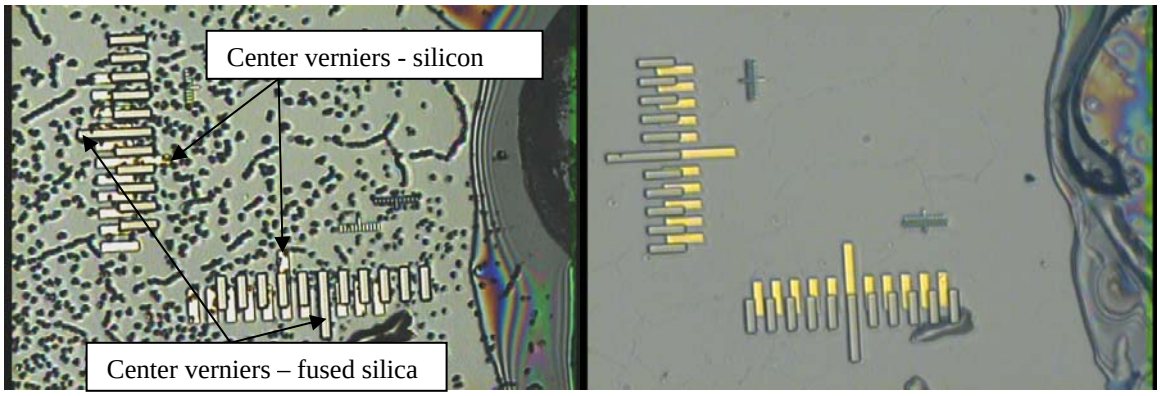

Figure 26. Alignment verniers before and after reflow.

The demonstrated lateral and rotational alignment tolerances fulfill the needs for the candidate optical systems discussed earlier. The relatively low process temperature also allows for the bonding of dissimilar materials like silicon and fused silica.

Mechanical Testing of Bonds

Several bonded die pairs were tested mechanically. Nine pairs were pull tested and six pairs were die shear tested. The number of samples tested did not provide any clear correspondence between bond strength and pad layout, bonding accuracy or solder deposition method. One interesting result was that some die with reduced pull test strength exhibited cracking in the glass. This would seem to indicate that the glass had been stressed around the UBM; weakening it below the strength of the solder. In most cases the area of failure was the solder with the pads on the separated die still covered with solder over the entire UBM. The average pull test force required to separate the die was 3.6 lbs. (1.64 kgs) and the average die shear force required was 2.86 lbs. (1.30 kgs).

Formic Acid Vapor Reflow Trial

Several attempts were made to reflow die using formic acid vapor; however, the results were unsatisfactory. A fused silica die was manually aligned to a silicon die on a hotplate and then covered with a Teflon container. The container was purged with dry nitrogen gas for 5 – 15 minutes. The nitrogen flow was then redirected through a container of formic acid acting as a bubbler for 30 – 60 minutes with the temperature of the hotplate set to 70 – 90 ºC. The hotplate temperature was then raised above the eutectic temperature in an effort to reflow the solder. Out of six trials, four did not successfully bond the die together. The other two did result in bonded die, but there was no evidence of self-alignment.

Conclusions

We have investigated the electrical, optical and mechanical requirements for a passively aligned optoelectronic system and pursued the development of an appropriate packaging technology to facilitate its realization. High speed components including VCSELs and photodetectors have been characterized and models developed to aid in the design of a fully functional optical link demonstration. Electrical transmission line models using the diverse materials required for this type of link have also been developed.

The required optical alignments for use with optical fibers and high speed detectors have been determined. These mechanical requirements along with the limitations imposed by the use of dissimilar materials guided the development of an appropriate bonding process. Indium tin solder was pursued with emphasis on developing a deposition process (that provided the desired eutectic alloy as well as good volume control) and a reflow process capable of providing self-alignment. Self-alignment with sub-micron accuracy was demonstrated with a flux-based process that successfully bonded together fused silica and silicon test die.

References

[1] L.F. Miller, “Controlled Collapse Reflow Chip Joining,” IBM J. Res. Develop., May 1969, pp. 239-250.

[2] Wei Lin, Susan K. Patra and Y.C. Lee, “Design of Solder Joints for Self-Aligned Optoelectronic Assemblies,” IEEE Trans. Components, Packaging and Manufacturing Technology – Part B, vol. 18, no. 3 (August 1995) pp. 543-551.

[3] Michael J. Wale and Colin Edge, “Self-Aligned Flip-Chip Assembly of Photonic Devices with Electrical and Optical Connections,” IEEE Trans. Components, Hybrids and Manufacturing Tech., vol. 13, no. 4 (December 1990) pp. 780-786.

[4] Selah Choe, William W. So and Chin C. Lee, “Low Temperature Fluxless Bonding Technique Using In-Sn Composite,” Proc 50th Electronic Components and Technology Conference 2000, pp. 114 – 118.

[5] Ricky W. Chuang, Selah Choe and Chin C. Lee, “A Fluxless Sn-In Bonding Process Achieving High Re-Melting Temperature,” Proc 51st Electronic Components and Technology Conference 2001.

[6] Ricky W. Chuang and Chin C. Lee, “High-temperature non-eutectic indium-tin joints fabricated by a fluxless process,” Thin Solid Films, vol. 414 (2002) pp. 175-179.

[7] Kun-Mo Chu, Jung-Sub Lee, Han Seo Cho, Hyo-Hoon Park and Duk Young Jeon, “A Fluxless Flip-Chip Bonding for VCSEL Arrays Using Silver-Coated Indium Solder Bumps,” IEEE Trans. Elec. Pack. Manuf., vol. 27, no. 4 (October 2004) pp. 246-253.

[8] Superior Supersafe® No. 30 Datasheet, Superior Flux & Mfg. Co.

[9] Superior Supersafe® No. 30 Material Safety Data Sheet, Superior Flux & Mfg. Co.

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