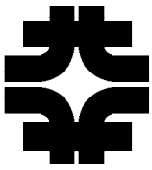

Fermi National Accelerator Laboratory

SVX II Silicon Strip Detector Upgrade Project
Readout Electronics

Configuration ROM,
Control and Status Registers and
Geographical Addressing Definitions
for
SVX II Silicon Strip Detector Upgrade Project
Readout Electronics VMEbus Module Designs

Version 1.0

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1. GENERAL INFORMATION

The information for these register definitions has been gathered from the VME64 (rev 1.11, 2/4/95) specification and VME64 extensions ballot (Draft 1.0, 12/7/95) specification. After review of the VME64 and VME64 Extensions it has been deemed inappropriate to include those CR/CSR definitions in to the SVX system. A greatly reduced set of CR/CSR information is presented here which is independent of but not in conflict with the VME64/VME 64 Extensions technique.

1.1 System Introduction

The VMEbus modules being designed for this project are responsible for the control and readout of the SVX-III Integrated Circuit chips as part of the SVX Silicon Strip Detector Upgrade Project.

1.2 Configuration ROM and Control and Status Register Requirements

To improve both system and software maintenance the following primary features are to be implemented on the SVX VMEbus modules:

- Geographical Address Assignment
- Board Identification

2. THEORY OF OPERATION

2.1 Bus Monarch

During system configuration there is assumed to be one Bus Master that is assigned the task, often referred to as the Resource Manager Task, of dynamically allocating board location/base address This Bus Master can be referred to as the Bus Monarch. The SVX addressing scheme detailed below obviates the requirement for a Bus Monarch and is processor-independent.

2.2 Addressing of SVX Modules

To allow for base address assignment, and the other features provided by CR and CSR registers, there must be some mechanism to "force" the CR and CSR registers to a known location at boot-up. In the SVX system there is no dynamic allocation of addresses. Module addresses are defined such that each module is allocated a space of 128 MBytes, with the starting address of every module determined solely by its Geographic Address. The base address of the module may not be modified by the Bus Monarch or any other processor.

Upon power up each module takes the Geographic Address as found on the GA pins and shifts it left 27 bits to determine the module Base Address (see Figure 1 on the next page). All SVX modules are to be addressed in A32 mode.

2.3 Address Modifies Used by SVX modules

SVX Modules shall respond to the following Address Modifier Codes ONLY:

- 0x08 A32 non-privileged D64 transfer
- 0x09 A32 non-privileged D32/D16/D08 transfer
- 0x0A A32 non-privileged program access
- 0x0B A32 non privileged block transfer

2.4 CR/CSR Base Address - Geographical Addressing Mechanisms

The CR/CSR Logical Address can be set using two different mechanisms.

- Geographical Address pins GA0..GA4,GAP on the 160-pin J1 as defined in the VME64 Extensions specification, or
- optional jumpers on the board which override the GA pins for non-VME64 Extensions subracks or for diagnostics.

SVX modules shall ignore the parity on the J1 connector. A map of how all SVX modules fit in to VME address space is shown in Figure 1 on the next page.

SVX Module Geographic Addressing Map

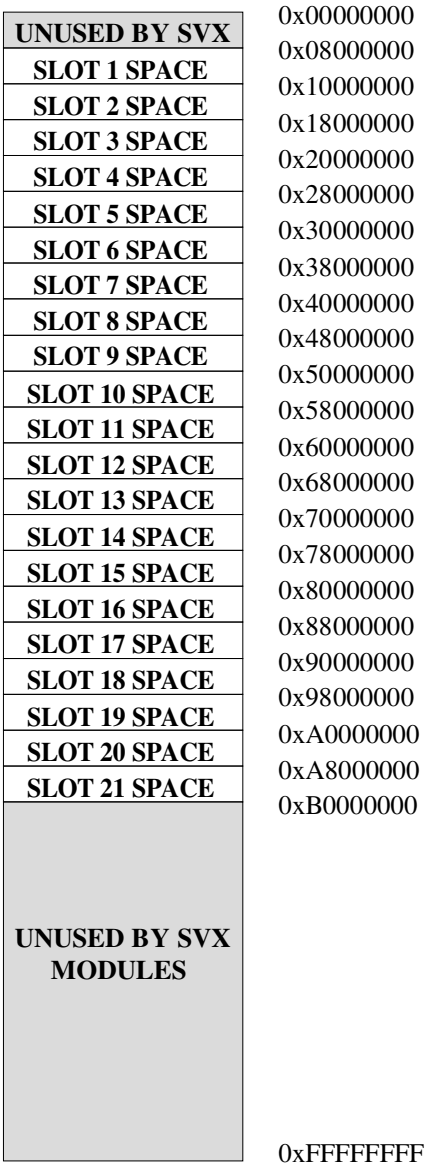

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Figure 1

SVX Address Map

2.4.1 160 Pin P1/J1

As defined in the VME64 Extensions, when a 160 Pin J1 connector is used, the following Geographical Address Pins have been pre-defined:

Table 1
J1 Geographic Address Pins

Pin Number (row d)	Pin Assignment
J1 - 9	GAP*
J1 - 10	GA0*
J1 - 11	GA1*
J1 - 13	GA2*
J1 - 15	GA3*
J1 - 17	GA4*

Table 2 below shows how these pin assignments are translated to the Slot Address:

Table 2
GA pin voltages for various slot addresses

Slot Address	GAP* pin (even parity)	GA4* pin	GA3* pin	GA2* pin	GA1* pin	GA0* pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

- Please note that the maximum current through the geographical address pin will be limited to 2 mA.
- All open positions will be pulled up to VCC on the SVX modules.

3. CR AND CSR TABLES

Table 3 below defines the single Configuration ROM location which is common to SVX Modules. SVX Modules have no common CSRs, although individual modules may define them as needed within their allowed address space.

3.1 Configuration ROM

Table 3
SVX Configuration ROM

Address Offset	Definition
0x00	Module Type code: 00: illegal 01: SRC 02: FIB 03: VRB 04: FIB Fanout 05: SVX Test Module 06 - FE: Reserved for future use. FF: illegal
0x01, 0x02, 0x03	User defined bytes. The authors suggest these be used to encode module revision data such as ECO number, netlist revision, firmware version, serial number, etc.

4. Front Panel LED - VMEbus SELECT

One front panel amber LED is required, labeled SELECT, which indicates when the module recognizes its address on the bus.

The LED should stay on for a minimum of 100 milliseconds, so that the human eye can recognize that the LED did turn on.

The LED should be mounted at the top of the front panel, as close as possible to the top extraction handle, as shown in Figure 2.

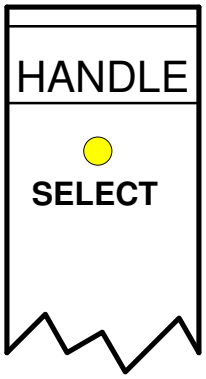

Figure 2

Select LED Mounting

4.1 LED Color Guidelines

Red should only be used for error indicators.

Green should only be used for static status indicators.

Amber should only be used for transient status indicators (e.g. operation in progress, module addressed, etc.)

Blue may be used for any other indicator purpose.