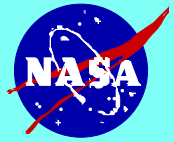

Silicon Carbide Buried-Gate Junction Field Effect Transistors for High-Temperature Power Electronic Applications

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Key Accomplishments Using Site-Competition Epitaxy

- Very low doped CVD SiC epilayers

  Record 3C-SiC (300 V) and 6H-SiC (2000 V) high voltage p-n diodes

- Very degenerately doped n- and p-type epilayers

  "Ohmic as deposited" contacts for most metals

  Typical as-deposited 6H-SiC contact resistivities:

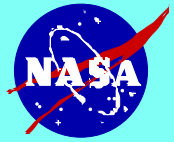
  n^+: ρ_c $1\text{-}3\times10^{-4}$ Ω cm^2 (Kuphal's four point)

  p^+: ρ_c $0.3\text{-}2\times10^{-3}$ Ω cm^2 (Kuphal's four point)

  Lowest measured:

  Tantalum on n^+: ρ_c 2×10^{-5} Ω cm^2 (Kuphal's four point)

  Titanium on n^+: ρ_c 2×10^{-5} Ω cm^2 (Linear TLM)



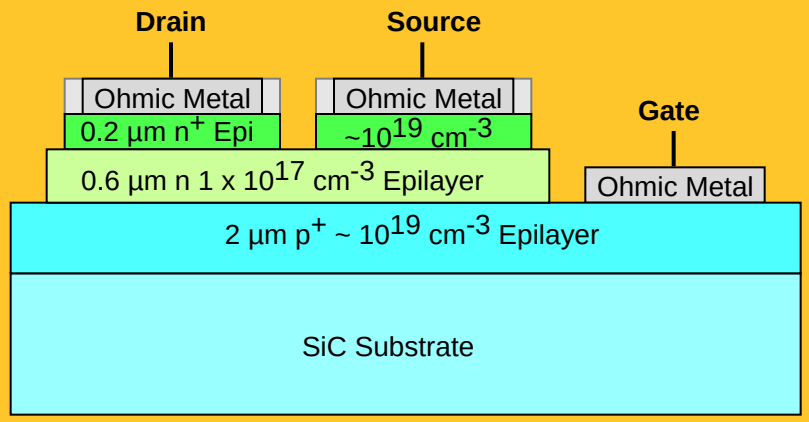
Approach

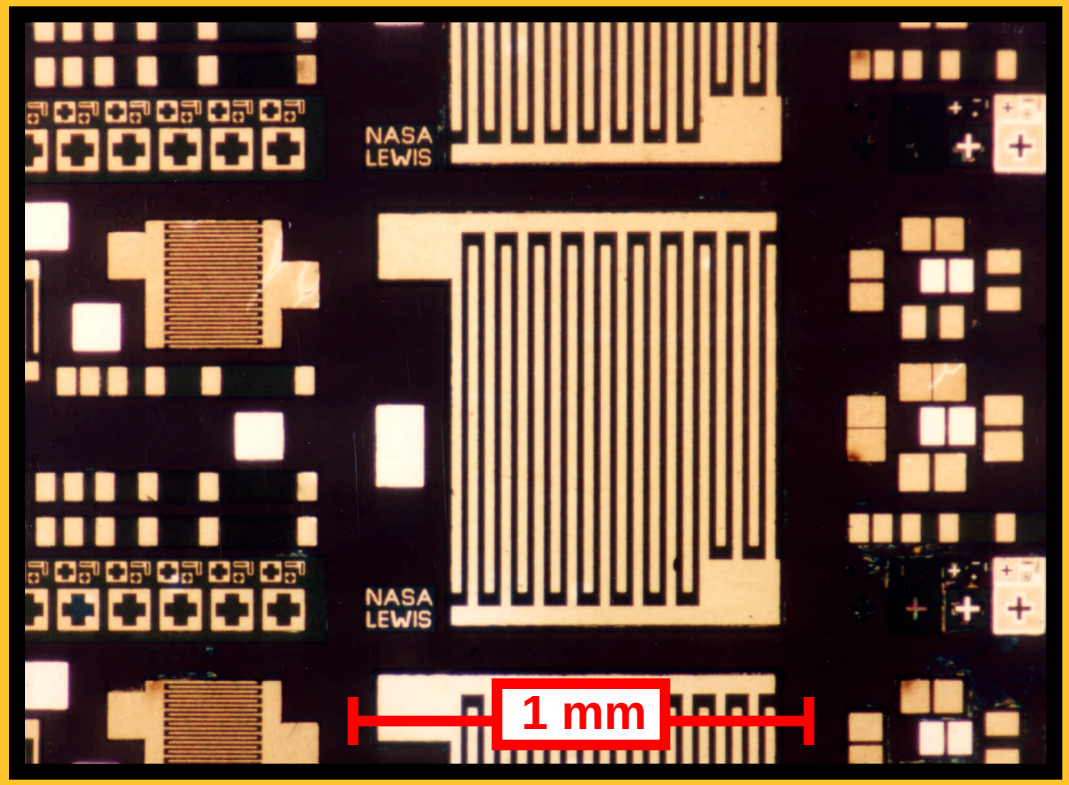
- Use **Site Competition Epitaxy** to provide JFET device epilayer structures with highly degenerate "ohmic-as-deposited" SiC contact layers.

- Fabricate generic buried-gate JFET mesa structures without ohmic contacts.
  - Small-area JFET's and test structures for proof-of-concept, high temperature operational testing.
  - Large-area JFET's for state-of-SiC-art power devices.

- Apply and test a variety of ohmic contact metallization schemes.
  - NASA Milestone Requirement: 30 hours of operation at 600 °C **in air**.

NASA Lewis 6H-SiC Buried-Gate Junction Field-Effect Transistors





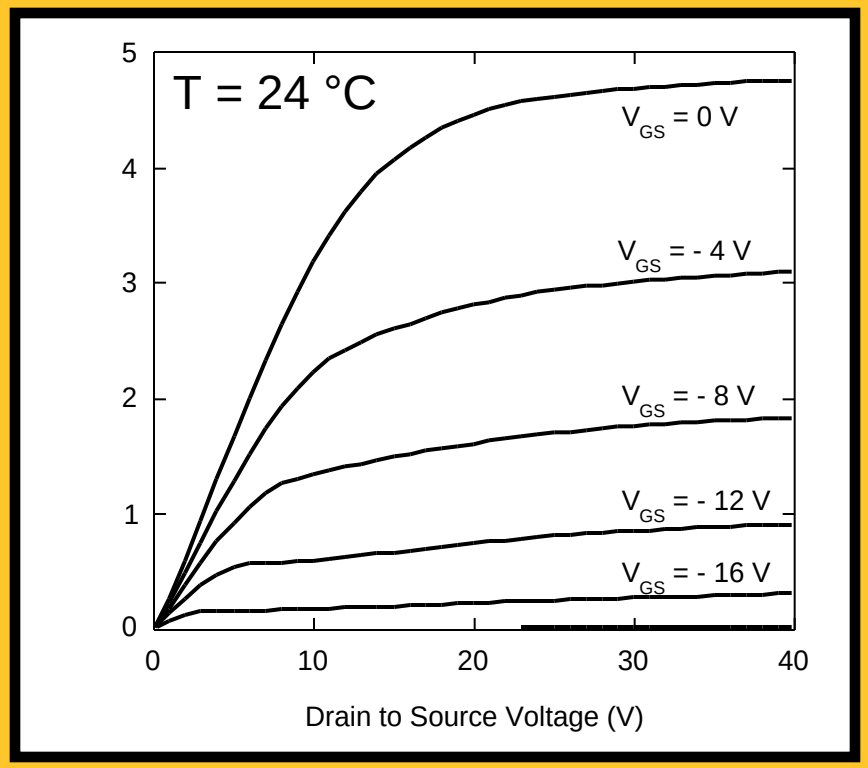
National Aeronautics and
Space Administration
Lewis Research Center

**INSTRUMENTATION & CONTROL
TECHNOLOGY DIVISION**

6H-SiC Buried Gate N-Channel JFET

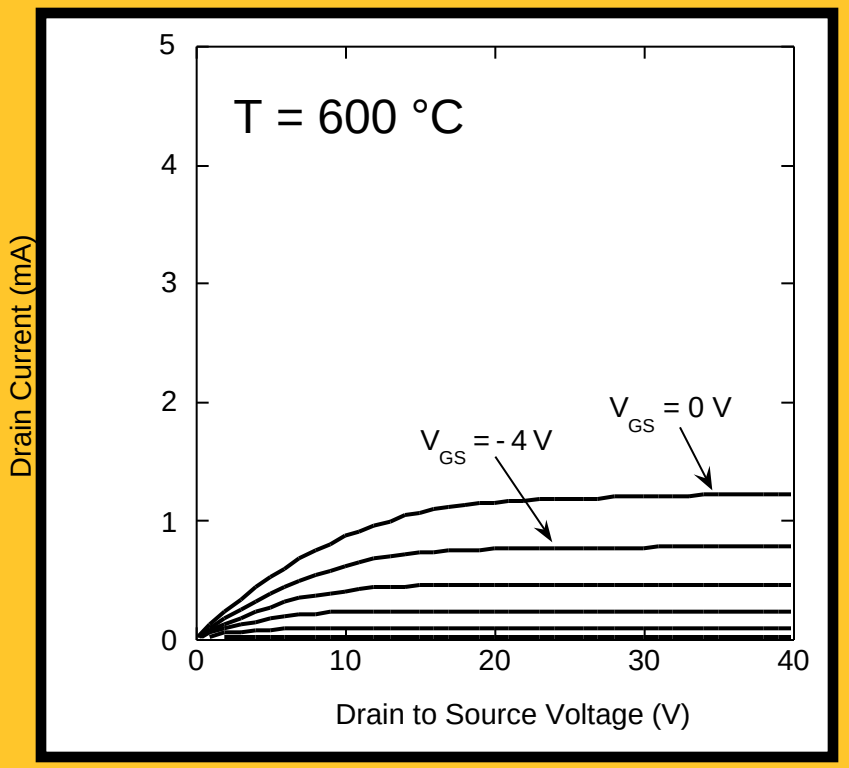
L_G = 10 µm W_G = 90 µm

Room-Temperature Characteristics



g_{max} 4.8 mS/mm

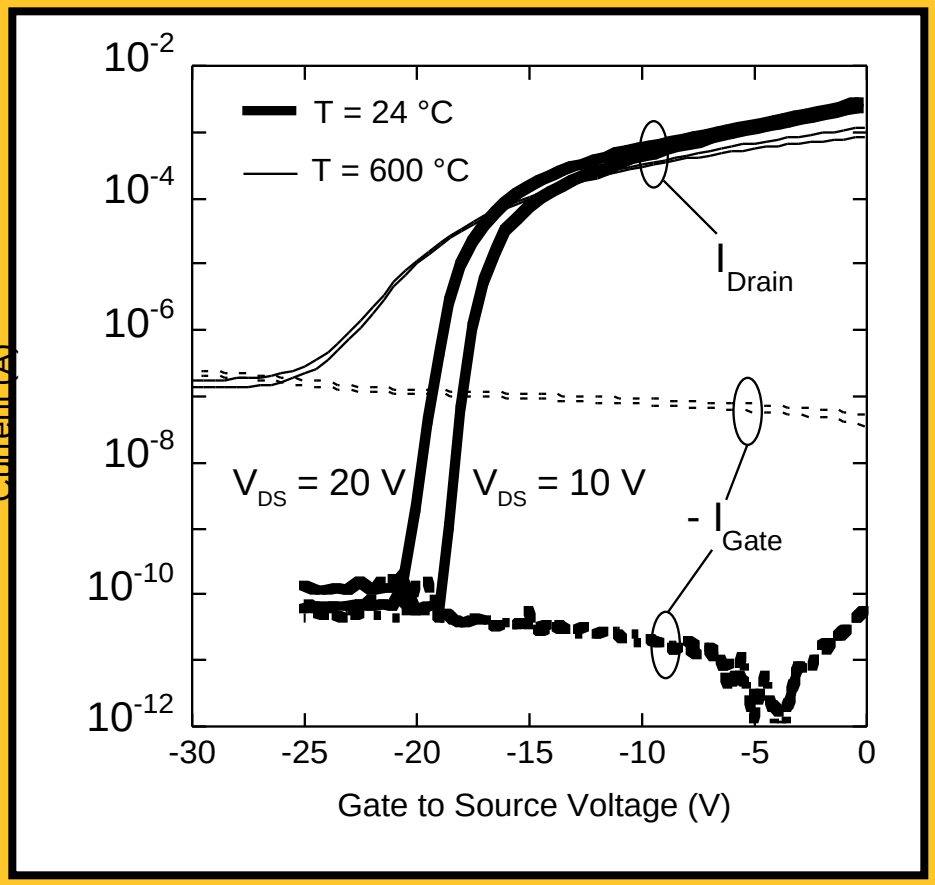
High-Temperature Characteristics

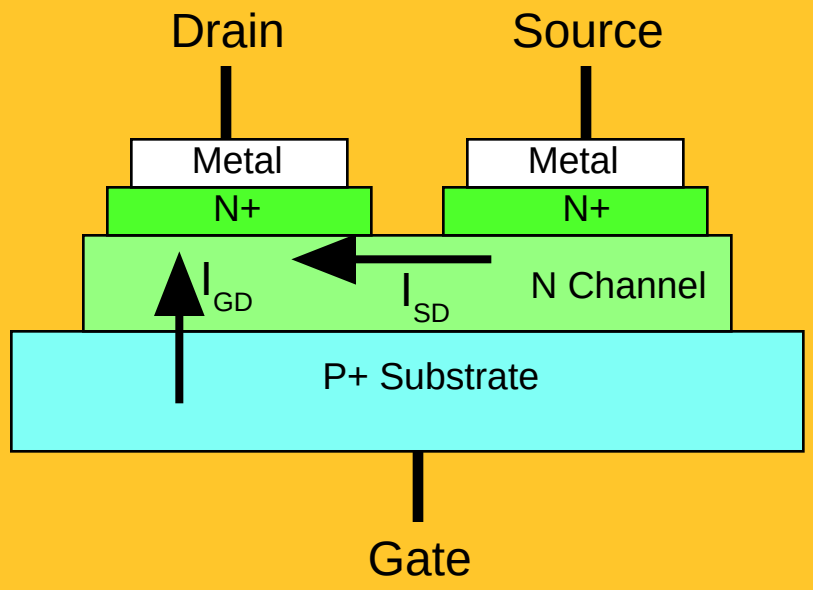


g_{max} 1.1 mS/mm

JFET Turn-Off Characteristics

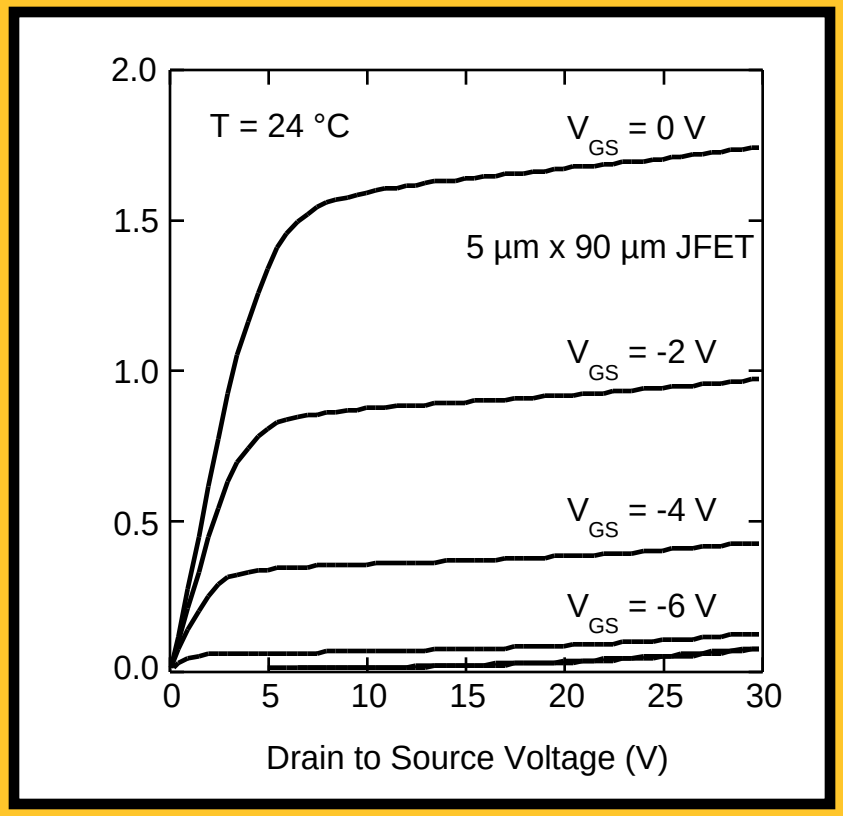
10 µm x 90 µm 6H-SiC JFET



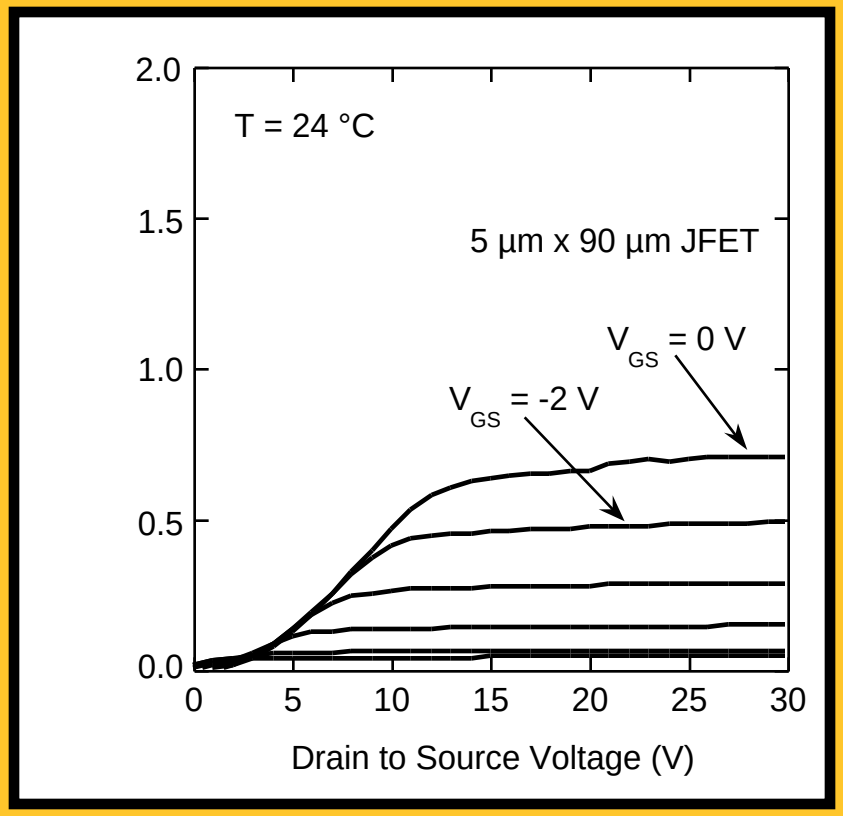


500 Å Mo / 1000 Å Pt Contact JFET

After 1-hour 600 °C **Vacuum** Anneal

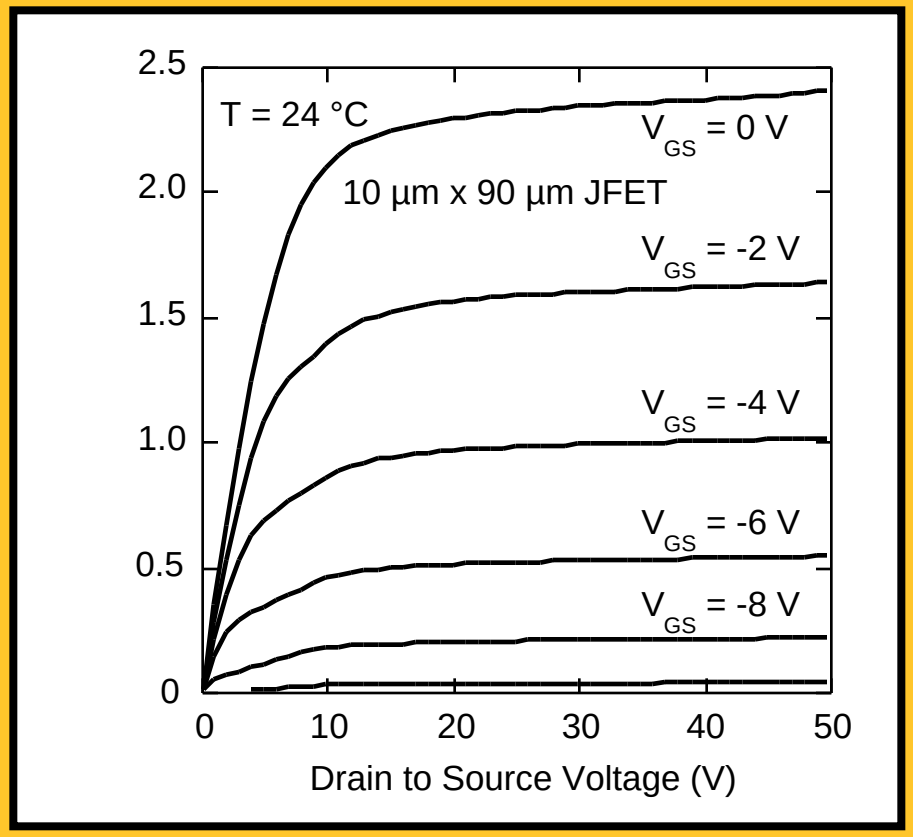


After 1-hour 600 °C **Air** Anneal

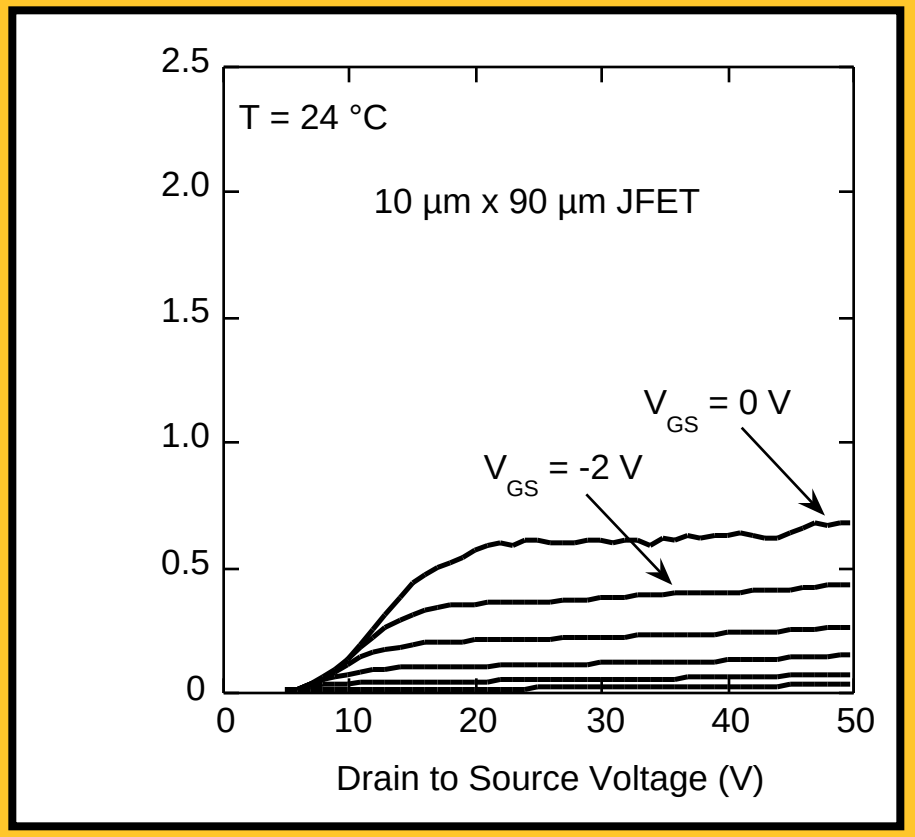


250 Å Ta / 500 Å TaN / 600 Å Pt Contact JFET

After 15-hour 600 °C **Vacuum** Anneal

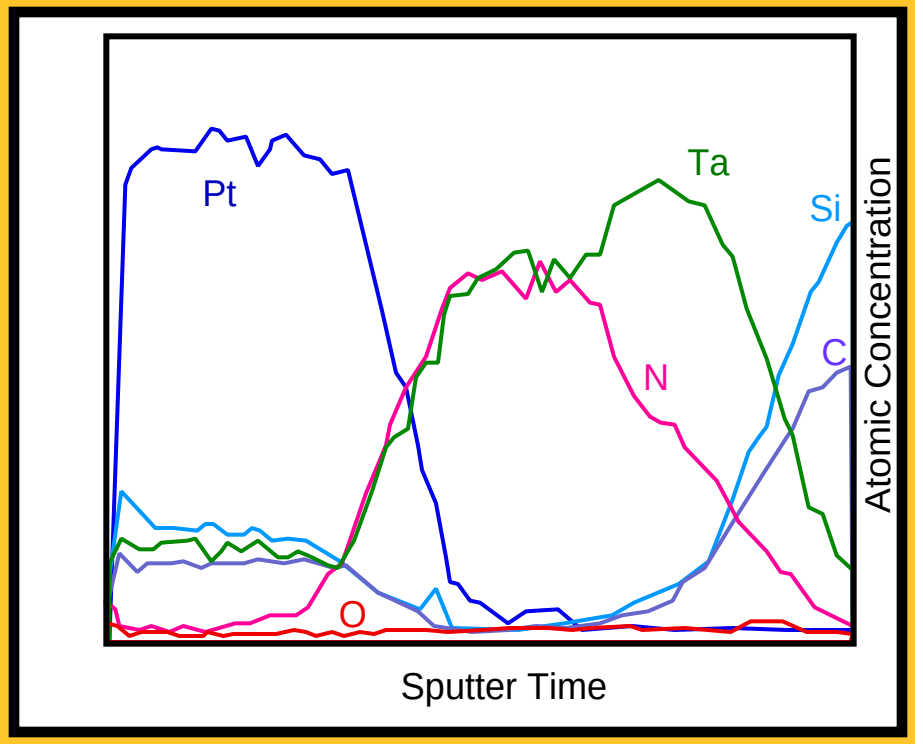


After 15-hour 600 °C **Air** Anneal

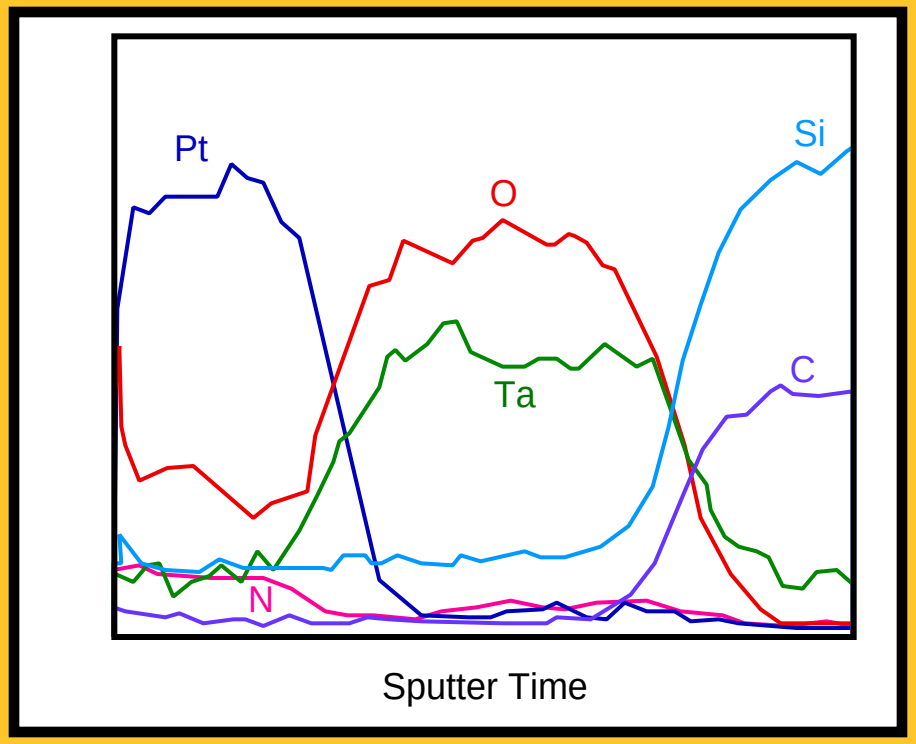


Auger Data taken on
250 Å Ta / 500 Å TaN / 600 Å Pt Contact JFET

After 15-hour 600 °C **Vacuum** Anneal

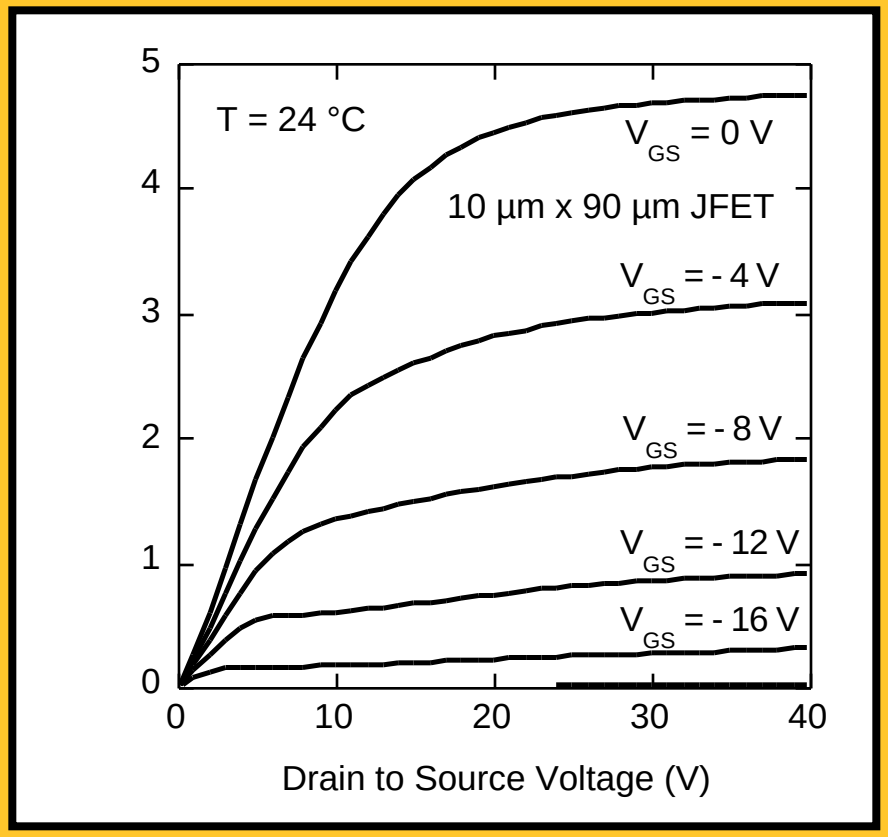


After 15-hour 600 °C **Air** Anneal

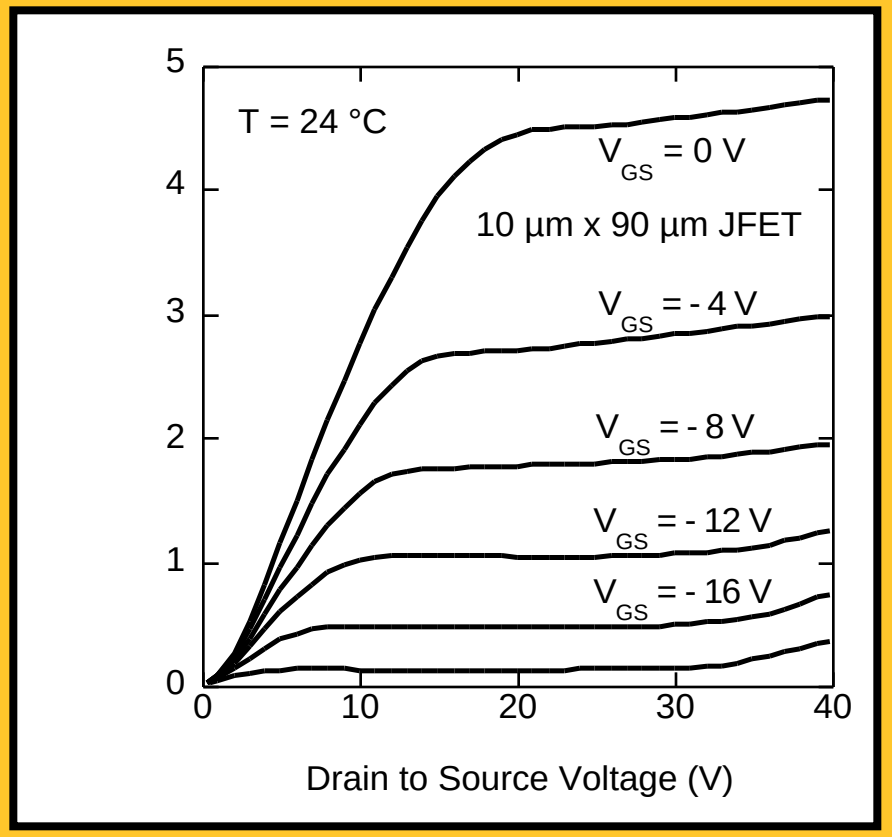


900 Å Si / 700 Å Pt Contact JFET

After 30-hour 600 °C **Vacuum** Anneal

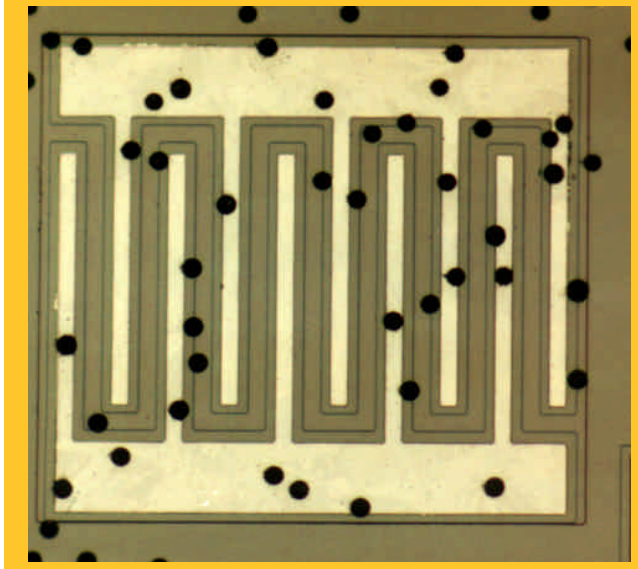


After 30-hour 600 °C **Air** Anneal

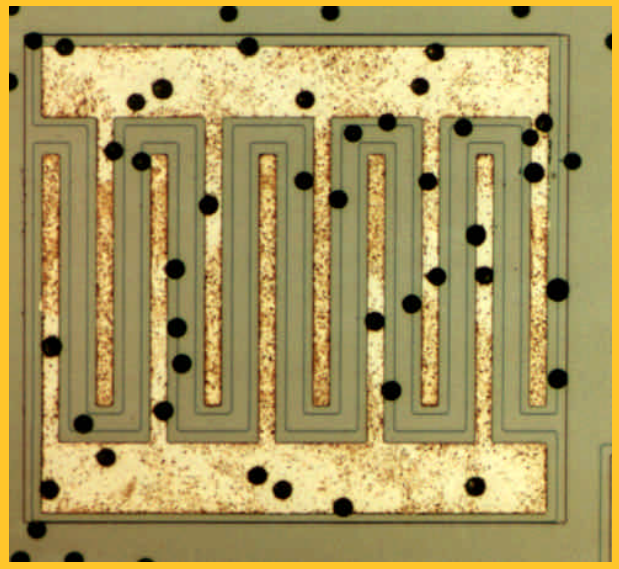


Si/Pt High Temperature Ohmic Contact to 6H-SiC JFET

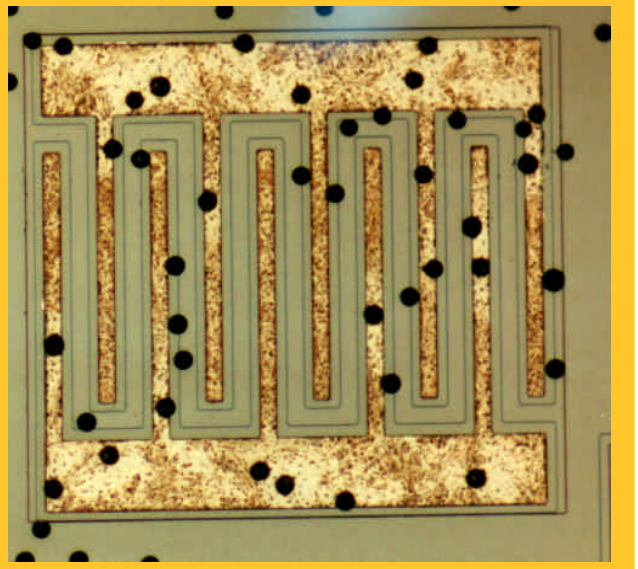
As-deposited, and following 30 hours 600 °C **vacuum** anneal



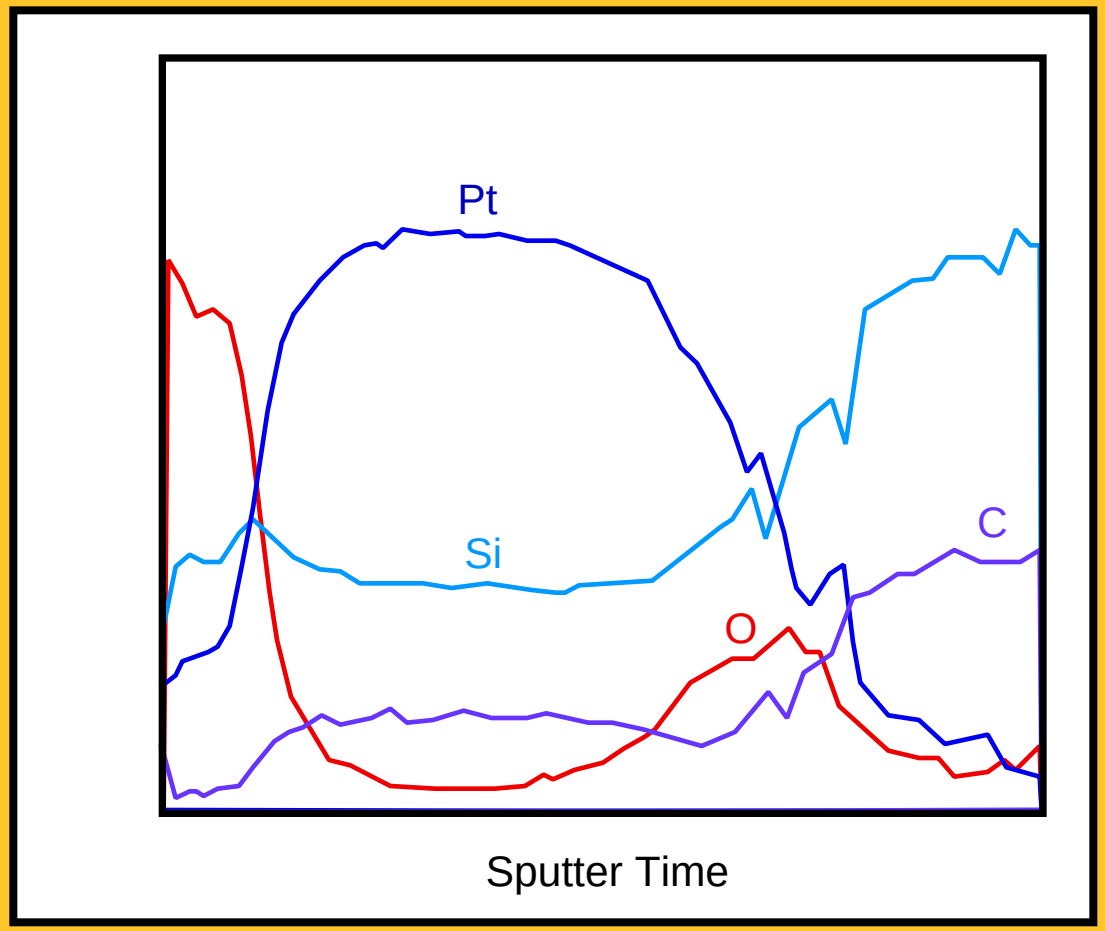
Following 15 hour 600 °C **air** anneal

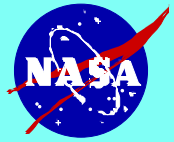


Following 31 hour 600 °C **air** anneal



Auger Data taken on 900 Å Si / 700 Å Pt Contact JFET Following 30-hour 600 °C **Air** Anneal

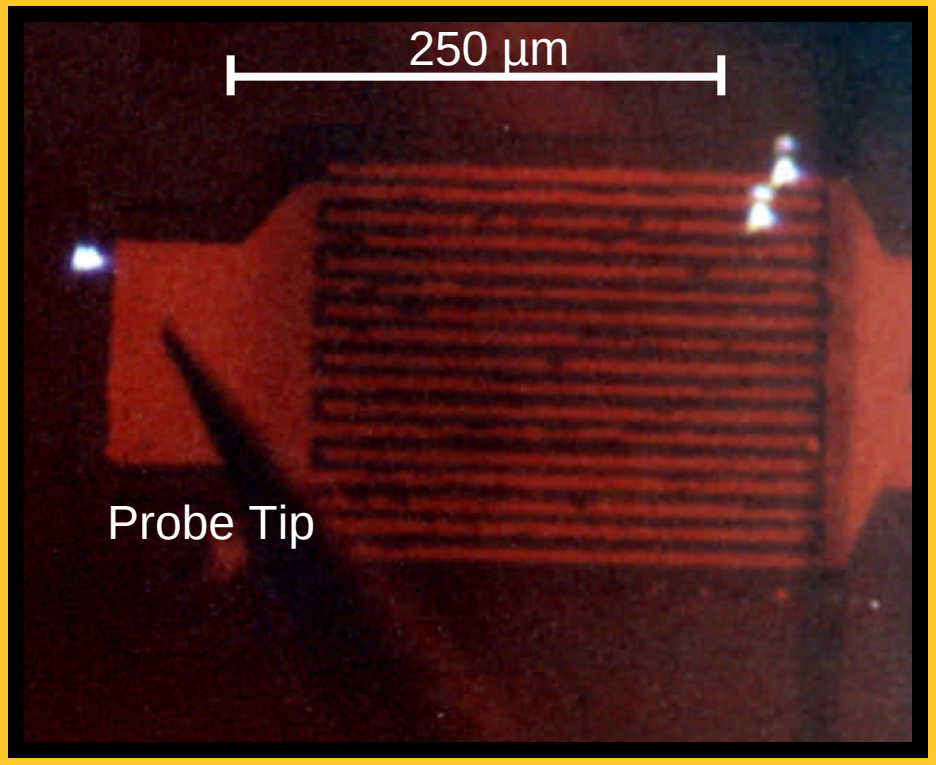




600 °C 6H-SiC JFET Summary

- Operation after 30-hour 600 °C air exposure.
- Ohmic contact stability is limiting factor.
- Oxidation plays key role in 600 °C air-environment contact degradation.
- Much work remains before truly useful 600 °C electronics can be realized.

Higher Current JFET's



Defects (primarily micropipes) present in SiC wafers and epilayers prevent scale-up of small-area power device results beyond 1 mm^2.

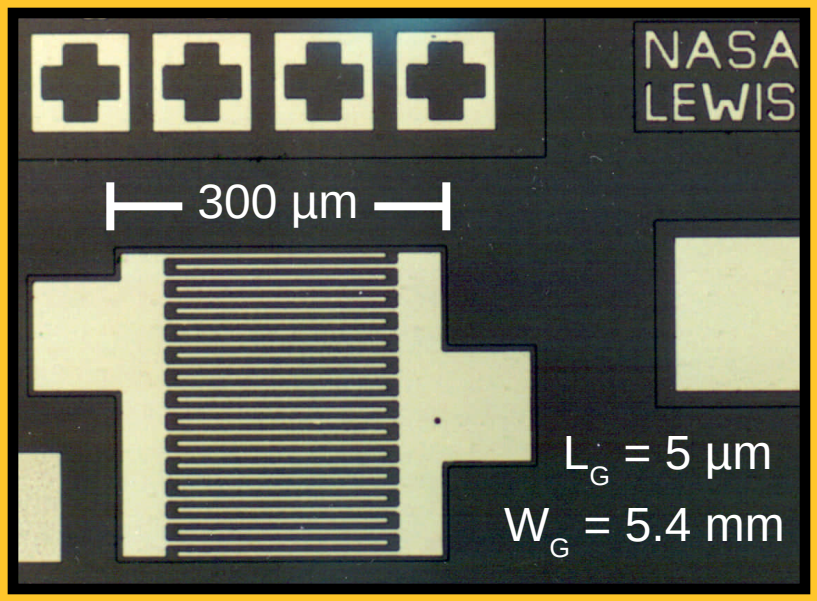
Undertook scale-up of JFET to see what could be done with lateral buried-gate device design in area of less than one square millimeter.

Goal: Demonstrate SiC device currents on the order of 1 A.

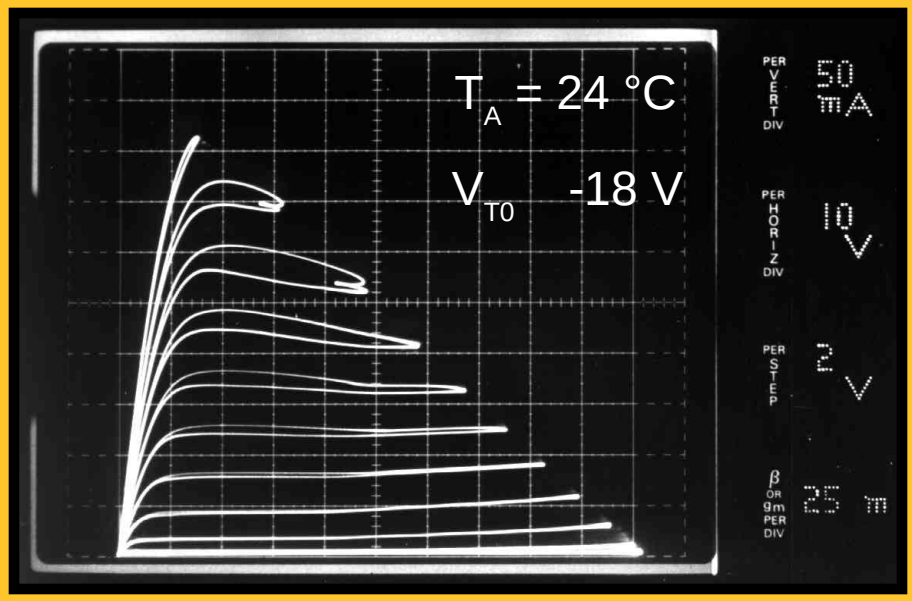
NASA Lewis 6H-SiC Buried-Gate N-JFET

(Nonoptimized lateral device geometry)

Device Area 9×10^{-4} cm^2



0.4 A Peak Current, 100 V Device



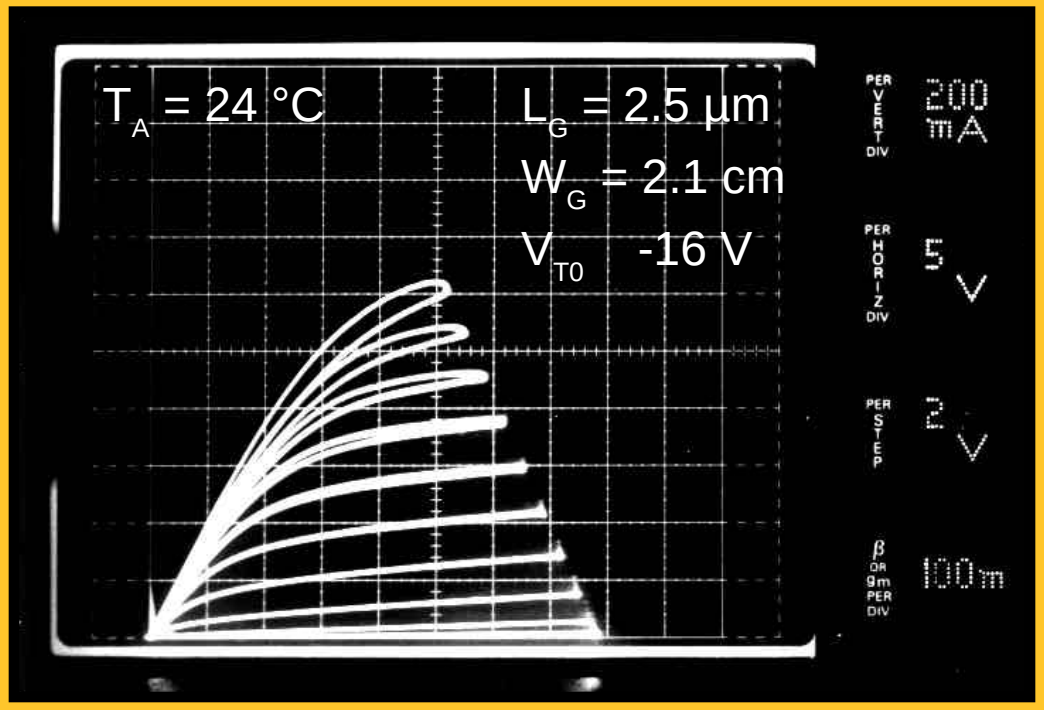
Measured ON Resistance 17 Ω = 15 mΩ • cm^2

Peak Current Density 440 A/cm^2

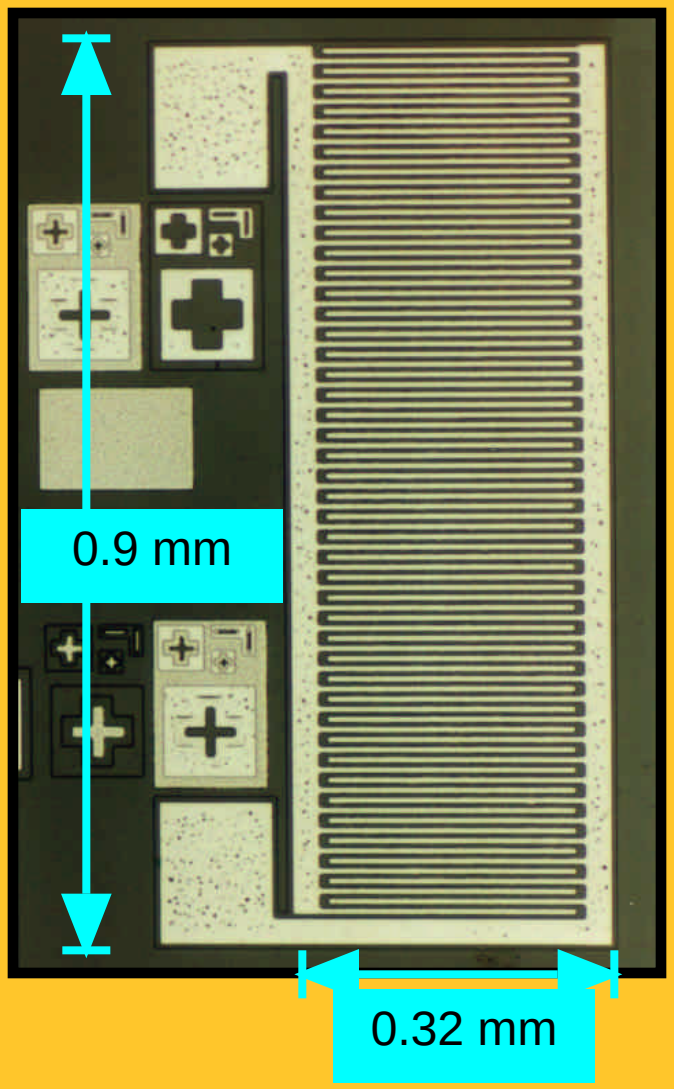
NASA Lewis 6H-SiC Buried-Gate N-JFET

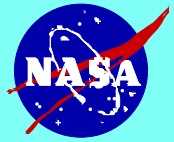
(Nonoptimized lateral device geometry)

1.2 A Peak Current, 100 V Device



ON Resistance 7 Ω = 20 mΩ • cm^2
(with probe resistance subtracted)





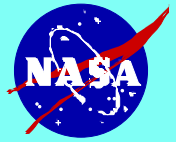
Summary

6H-SiC Buried-gate JFET's demonstrating:

- 30-hour stability in 600 °C air environment
- 1.2 A / 100-V operation

have been fabricated and characterized at NASA Lewis.

Process optimization, continued high-temperature contact metallization research, and vertical device geometries should enable further performance enhancements.



Acknowledgment

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NASA Lewis Research Center

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