NAVSEA LTC1272 Total Dose Test Report

Surface Warfare Center Division

Final Report

Prepared for:
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Code 562.1
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Summary

NAVSEA Crane Division performed total dose testing (using a dose rate of 0.8 rad(Si)/sec) on Linear Technologies LTC1272, 12 bit ADC's. Two parts were statically biased, six dynamically biased. Results of the total dose testing indicate:

- Both devices biased statically and one device biased dynamically had missing codes at 7.5krad(Si).
- Both devices biased statically showed degradation in effective number of bits at 7.5krad(Si). Three devices biased dynamically showed degradation in effective number of bits at 7.5krad(Si).
- Both devices biased statically had (maximum) differential non-linearity greater than +1.0 (specification limit) at 5krad(Si). Five devices biased dynamically had (maximum) differential non-linearity greater than 1.0 at 7.5krad(Si).
- Parametric shifts were observed at 5krad(Si).
- All eight devices were still functional, though at a significantly degraded performance level, at 30krad(Si).
- After a 168-hour biased room temperature anneal, all eight devices showed a significant improvement in performance, but did not improve to pre rad levels.

Introduction

Purpose

This testing was performed to provide parametric and radiation hardness performance information on the LTC1272 ADC for NASA.

Background

The LTC1272 is a commercial 12 bit, 250 kHz monolithic sampling analog-to-digital converter (ADC) manufactured by LTC Inc on their LTBiCMOS process. A total of four boards were manufactured by NAVSEA Crane to facilitate testing. Four boards were used for testing. Two boards were used for in-situ bias and anneal, one board was used for parametric testing and one board was used for dynamic testing.

Test Samples

A total of eight LTC1272's (serial numbers 1 through 8, inclusive) were tested. The eight devices were tested in two separate test runs. Parts #2, #3, #4, #5, and #6 were tested on November 9, 2001; parts #1, #7, and #8 were tested on November 11, 2001. All devices had a date code of 0018.

Table 1 gives a summary of the LTC1272 specifications of interest.

	LTC1272
Resolution	12 bits
Speed	f_{clk} (max) = 4.0 MHz
Power Consumption (max)	150 mW
Analog Input	-0.3 – 15V peak-peak
DNL	±1.0 LSB (max)
SINAD	72 dB at 10kHz input
ENOB	11.66 bits

Table 1 – LTC1272 Specifications of interest
(Refer to LTC1272 Specification Sheet in Appendix B for further information.)

Figure 1 shows a photograph of the LTC1272 die.

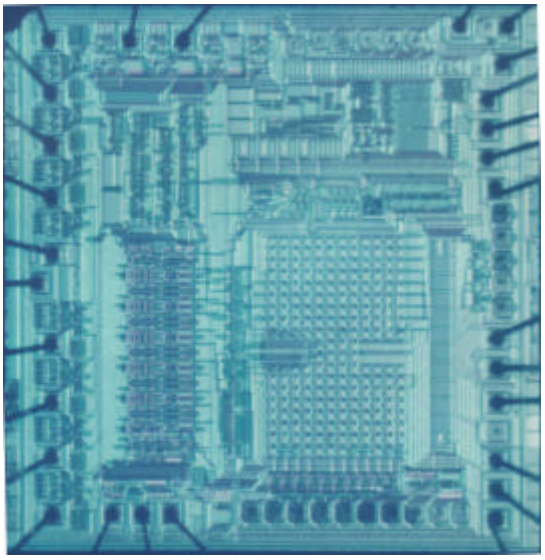


Figure 1 - LTC1272 Die

Facilities

All testing was performed at NAVSEA Crane Code 6054, using a Shepherd Model 484 Cobalt-60 tunnel irradiator.

Test Setup

The electrical testing was done on a customized ADC test bench. The ADC test bench utilized a HP6626A System DC Power Supply, two HP 8644(A&B) Synthesized Signal Generators, a HP 8175A pattern generator, a HP 33250A waveform generator and an HP8131A Pulse Generator. An HP82000 ATE was used for parametric tests as well as some dynamic functional testing. All parts were retained for possible future testing and analysis, if required.

Two parts were tested with a static bias applied during irradiation and six parts were tested with a dynamic bias applied. Static bias devices were irradiated with nominal DC power applied, while the clock and all other inputs were grounded. Dynamic bias used the same nominal DC power as the static bias condition, a 3.125 MHz clock signal and a 9.995 kHz, 4.8 volt peak-to-peak sinusoidal input signal.

The parameters tested were signal-to-noise and distortion (SINAD), effective number of bits (ENOB), total harmonic distortion (THD), spurious free dynamic range (SFDR) and differential non-linearity (DNL). Functional power supply currents and the DC Parameters were measured using an HP82000.

Bias conditions used for total dose tests:

Static:
- Vdd = +5.0V
- Clock = Ain = GND

Dynamic:
- Vdd = +5.0V
- Clock = 3.125 MHz
- Ain = 10 kHz, 4.8Vp-p Sinusoid

Voltage output high (Voh) and voltage output low (Vol) were measured using current loads shown as follows:

Voh -> -10 μA Vol -> 1.6 mA
Voh2 -> -200 μA

Power supply currents were monitored during irradiation. All testing was performed using a dose rate of 0.83 rad(Si)/sec. The dose increments of interest were 2.5, 5.0, 7.5, 10, 15, 20 and 30 krad(Si). A 168-hour biased room temperature anneal was performed immediately after irradiation.

Test Results

LTC1272

Statically biased devices showed drop in ENOB of approximately 10% at 5.0krad(Si) and a drop in ENOB of approximately 20% at 7.5krad(Si). From Figure 2 it can be seen that the dynamically biased parts responded to radiation in two separate groups. Group 1 consisted of part #2, #4 and #7, and group 2 consisted of part #1, #3, and #8. Group 1 parts showed a drop in ENOB of approximately 3% at 7.5krad(Si) and a drop in ENOB of approximately 5% at 10.0krad(Si). Group 2 parts showed a drop in ENOB of approximately 3% at 10.0krad(Si) and a drop in ENOB of approximately 8% at 15krad(Si). Although all eight devices were still functional at 30krad(Si), ENOB values showed a drop of more than 25%, except part #3 which actually recovered slightly at 30krad(Si).

The devices annealed very rapidly post-irradiation. It was observed, but not recorded, that some devices improved when tested again before being placed in the bias board for irradiation. The devices would be out of radiation for up to 45 minutes. As can be seen from Figure 2, part #3 apparently recovers slightly at 30krad(Si). This part was tested last, approximately 30 minutes after irradiation; it is believed that this apparent recovery could be due to annealing after radiation.

In Figure 3 it can be seen that all devices had missing codes at 10krad(Si), except part #7, which had missing codes at 15krad(Si). Figure 2 shows statically biased devices being out of the maximum DNL specification of +1.0 at 5.0krad(Si) and dynamically biased devices being out of maximum DNL specification at 7.5krad(Si). Part #3 is an exception, being out of specification at 10krad(Si).

The 168-hour anneal data shows a significant recovery in device performance with ENOB values above 9.0 for all devices. As can be seen from Figures 2 through 4, part #3 and part #8 recovered to near pre-irradiation performance, while the other devices also exhibited dramatic improvements in performance. Part #3 still had missing codes after the 168-hour anneal. All eight devices were out of maximum DNL specification after the 168-hour anneal.

In-situ bias conditions did have an impact on performance, with the dynamically biased parts showing a more gradual degradation in performance beginning at 7.5krad(Si), and the statically biased parts having a more rapid degradation in performance beginning at 5.0krad(Si), see Figure 2.

Parametric failures were observed at 5krad(Si) on all devices. This was made evident by an inability of the device to produce all low voltage levels or all high voltage levels on all bits. Thus when a voltage output low test was performed, not all bits would be low, creating parametric failures on some outputs. Adjusting input voltage levels would compensate for the problem initially; however, as radiation levels increased it became impractical to continually adjust the input voltage levels to compensate for this problem. Output bits that were at the proper levels showed no significant changes through radiation for either voltage output low or high. This would

suggest that there were no changes in the output drivers of the device and the problem is probably with the sample-and-hold circuitry on the input.

Although the power supply current did change through radiation, the change did not go out of specification. See appendix A for additional graphs of data including the power supply current.

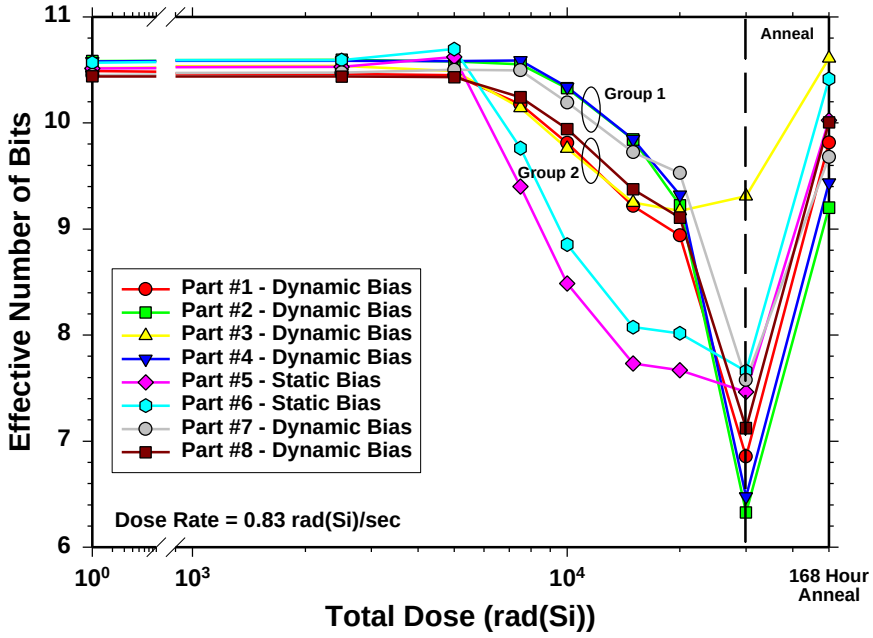


Figure 2

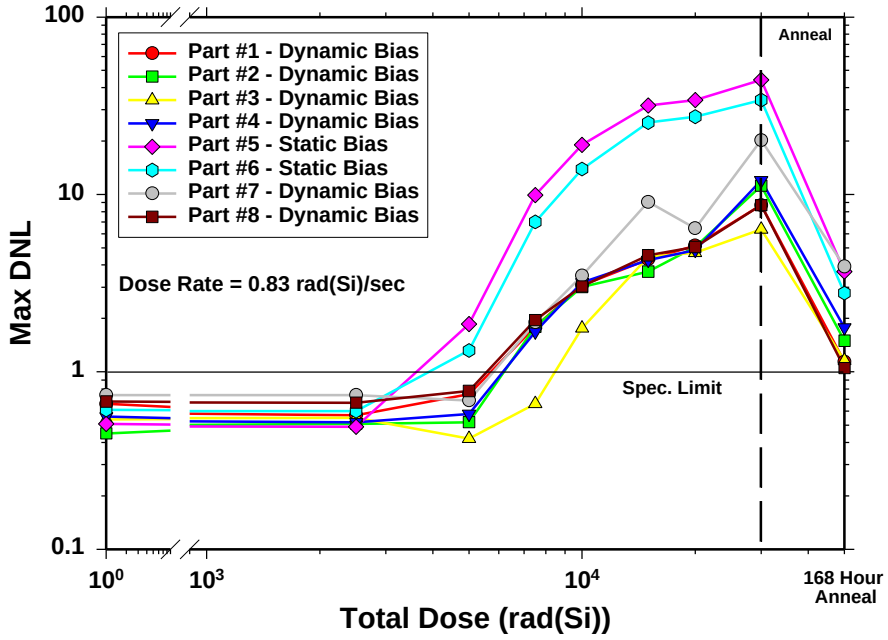


Figure 3

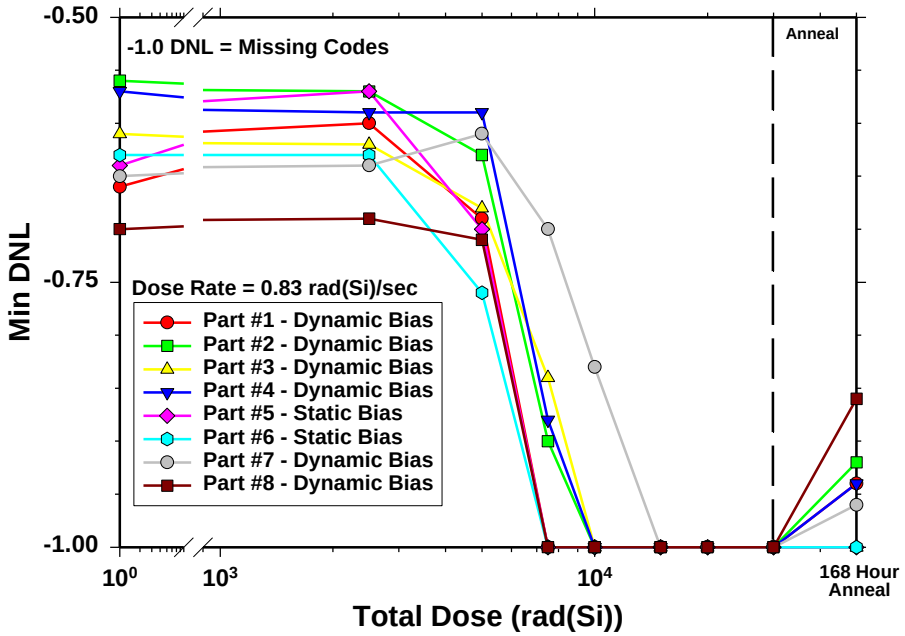


Figure 4

Appendix A contains graphs of all the device parameters measured by this test. The DC parametric data graphs showing V_{ol}, V_{oh} and V_{oh2} show no significant change with increasing dose. However, these graphs are based on averages of output pins that were at the correct level to test. As mentioned earlier, beginning at 5krad(Si) the devices could not produce all low voltage levels or all high voltage levels. Thus after 5krad(Si) these graphs do not include the output pins which were at the wrong voltage output level. The parametric data graphs shown are the average of all the device output pins at the correct output level and the variances in these data are shown representationally by error bars. The graphs of power supply currents likewise show no significant shift with device dose.

The voltage reference did show a change through irradiation for the parts tested on November 9, but did not show any significant change for the parts tested November 13. See appendix A for Vref graph. The reasons for this are unknown at this time, but it does not appear that the changes in Vref had any impact on the device response to irradiation. This is because the device response was very similar from the first and second test run on November 9 and 13. A control part was tested at every radiation level and did not show any changes in any parameter tested.

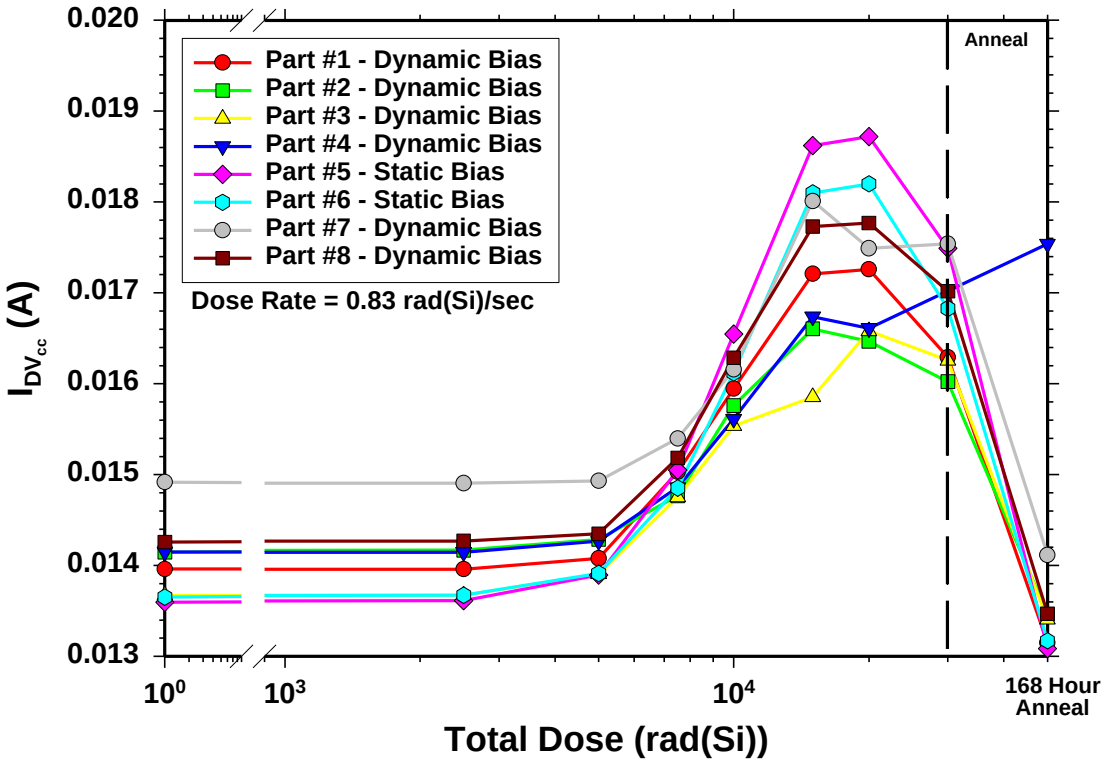
Parts #2, #3, and #4 inadvertently had the wrong bias applied (the clock signal was left off) during the irradiation from 5.0krad(Si) to 7.5krad(Si). This did not appear to affect the radiation response of the devices; as parts #1, #7, and #8 had a similar response to irradiation with correct bias applied.

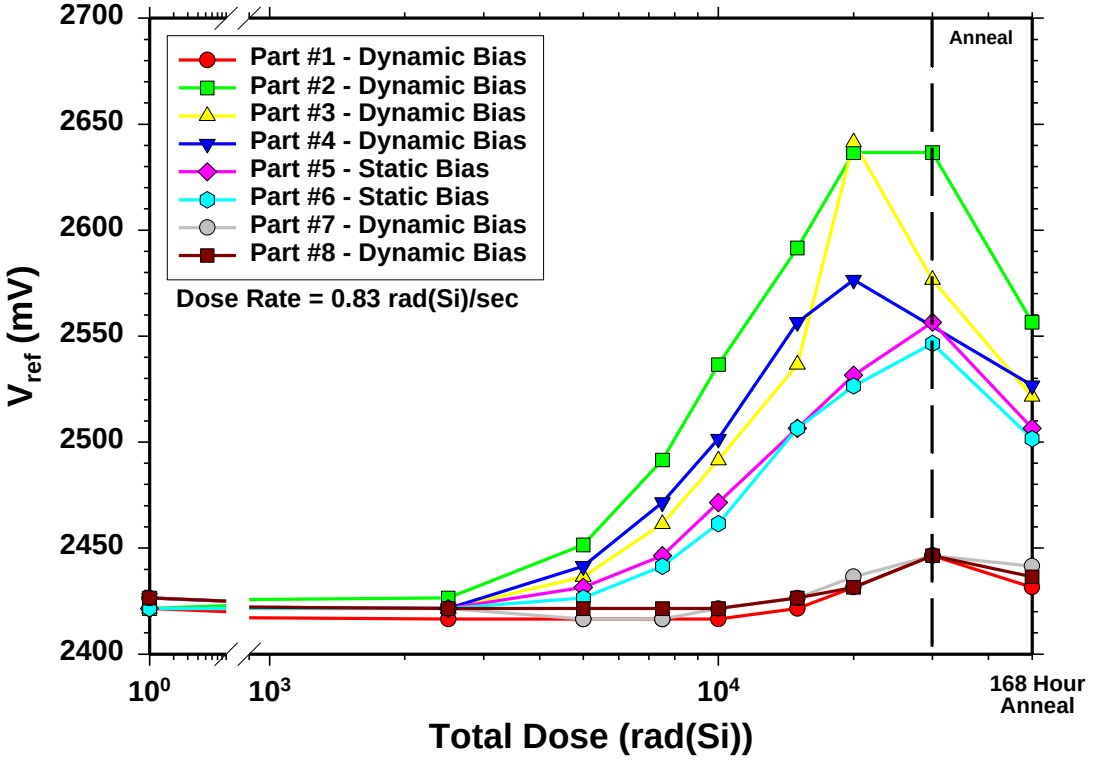
Conclusions

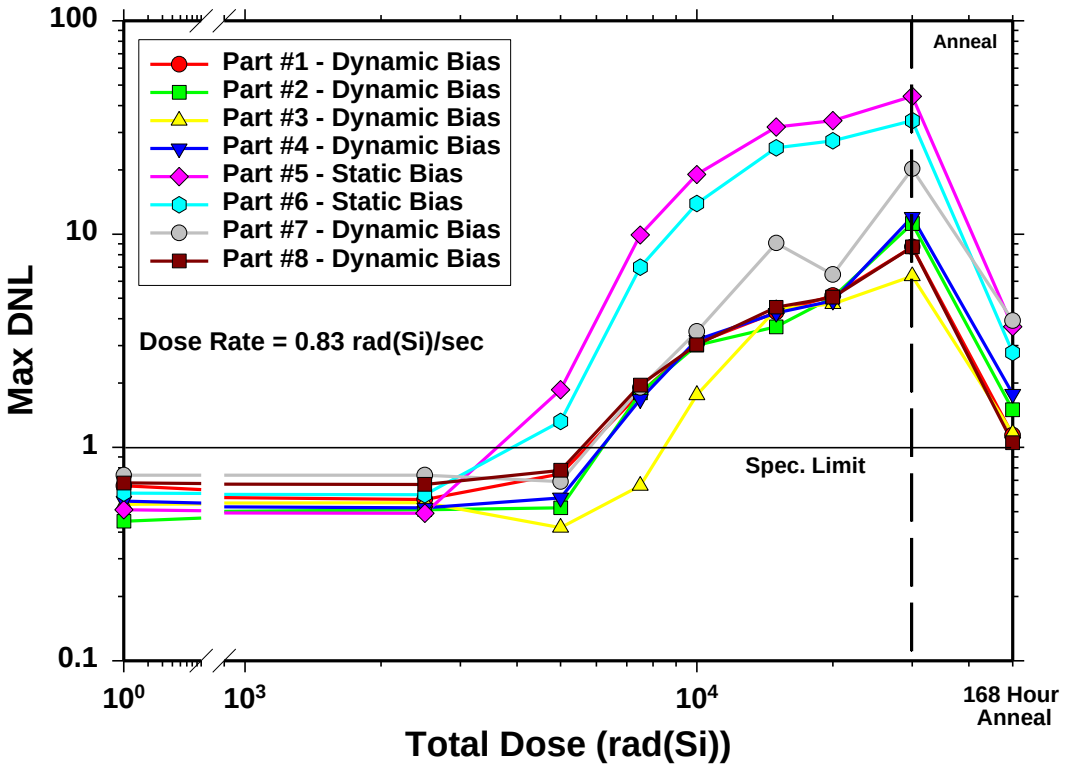
Because of the radiation performance of the LTC1272, it is not recommend that this part be used in any system with a radiation specification level of more than 3krad(Si), but even the 3krad(Si) specification the LTC1272 would only provide a 2X margin. Since there was not a wide variance in the LTC1272 radiation response, no additional radiation testing is recommended.

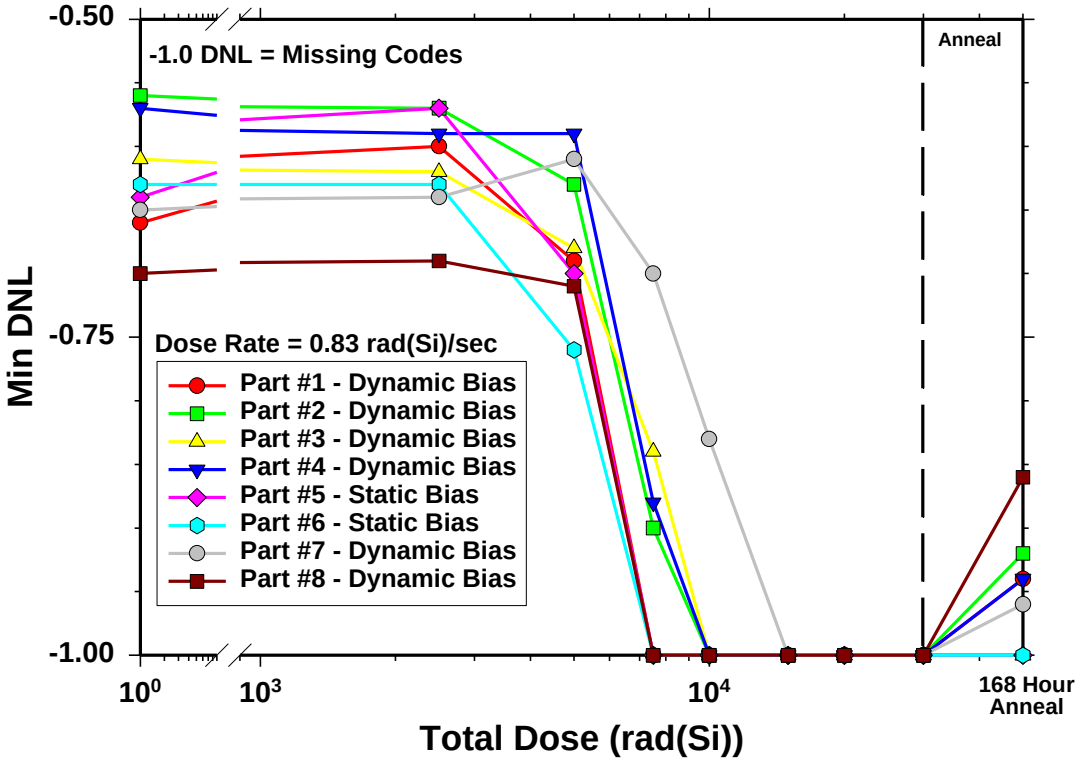
Any questions or comments should be directed to John Bings, 812-854-1672, bings@atd.crane.navy.mil or John Seiler, 812-854-2074, seiler_john@atd.crane.navy.mil.

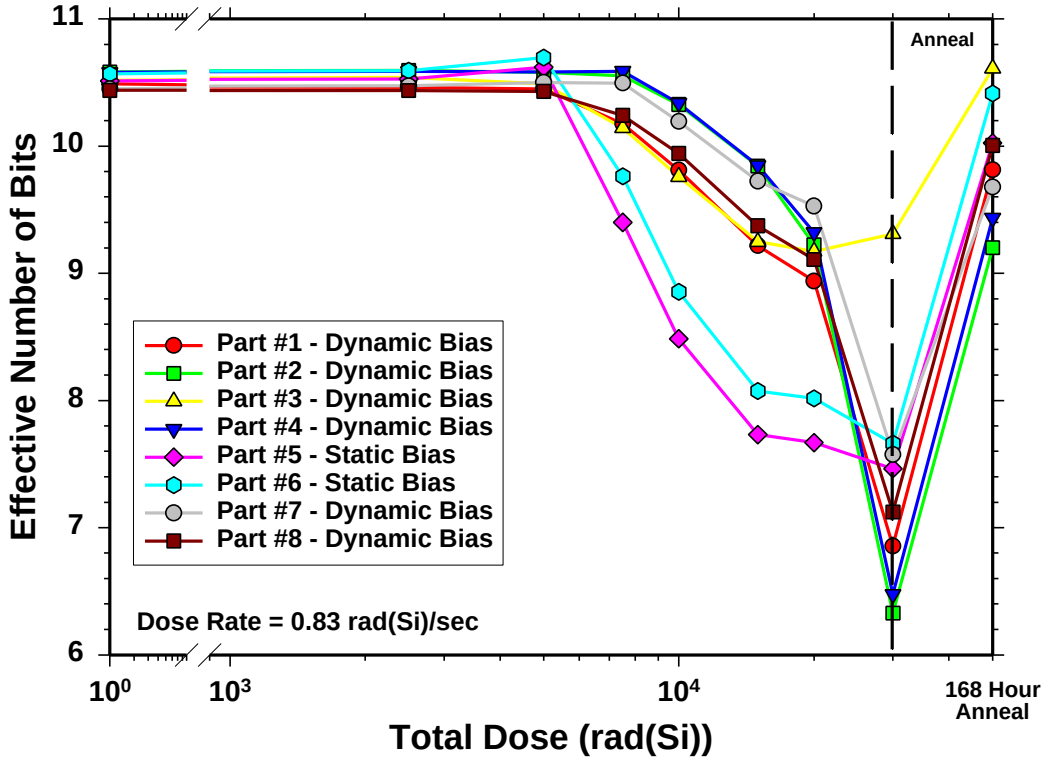
Appendix A
Data Graphs

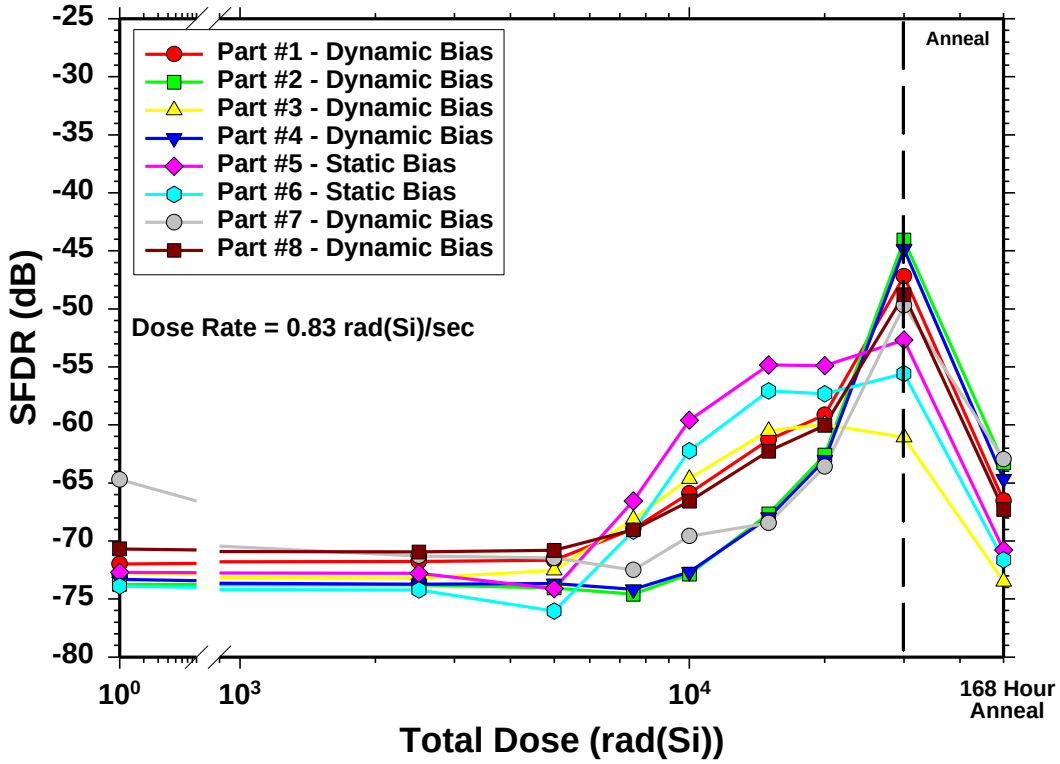

Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
Anneal
168 Hour Anneal
$I_{DV_{cc}}$ (A)
Total Dose (rad(Si))
0.020
0.019
0.018
0.017
0.016
0.015
0.014
0.013
10^0
10^3
10^4

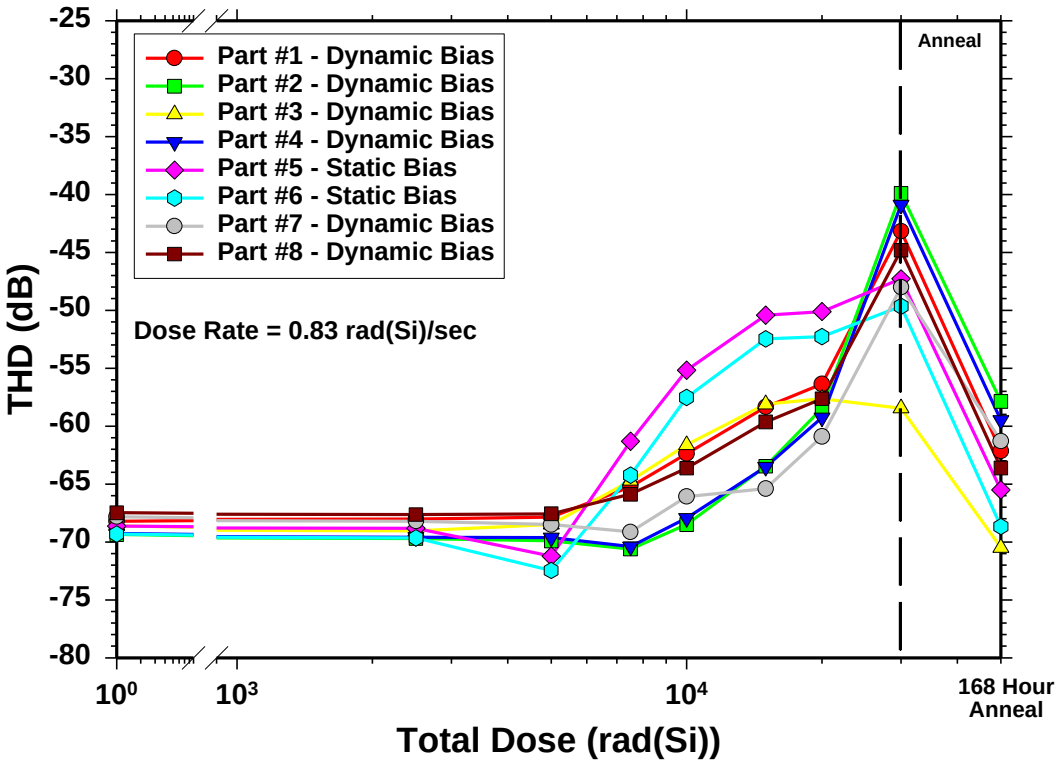

Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
Anneal
168 Hour Anneal
V_{ref} (mV)
Total Dose (rad(Si))
2700
2650
2600
2550
2500
2450
2400
10^0
10^3
10^4

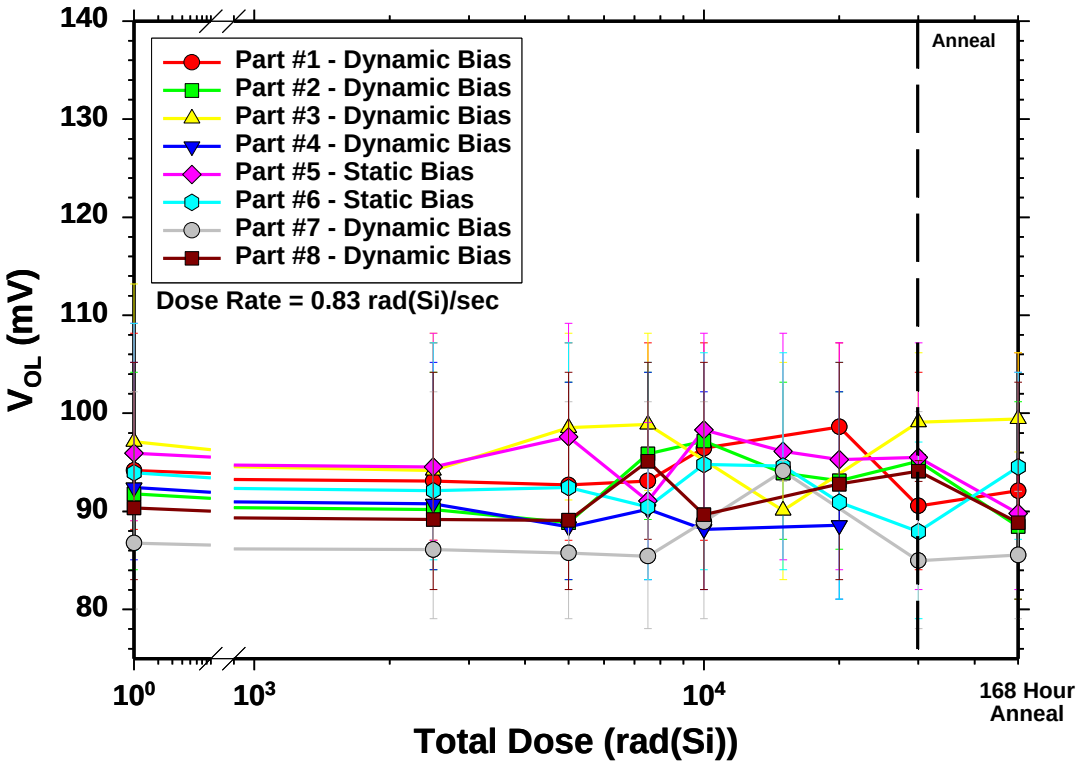

100
10
1
0.1
Max DNL
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
Anneal
Spec. Limit
10^0
10^3
10^4
168 Hour
Anneal
Total Dose (rad(Si))

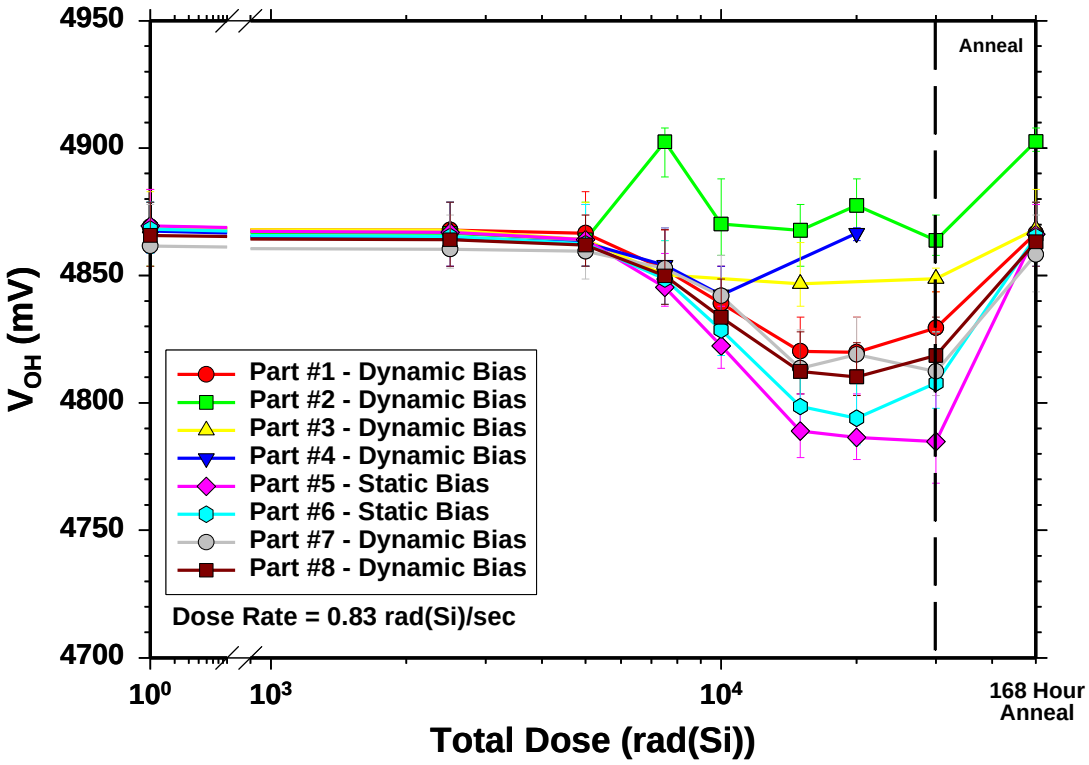

-0.50
-0.75
-1.00
Min DNL
-1.0 DNL = Missing Codes
Anneal
Dose Rate = 0.83 rad(Si)/sec
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
10^0
10^3
10^4
168 Hour
Anneal
Total Dose (rad(Si))

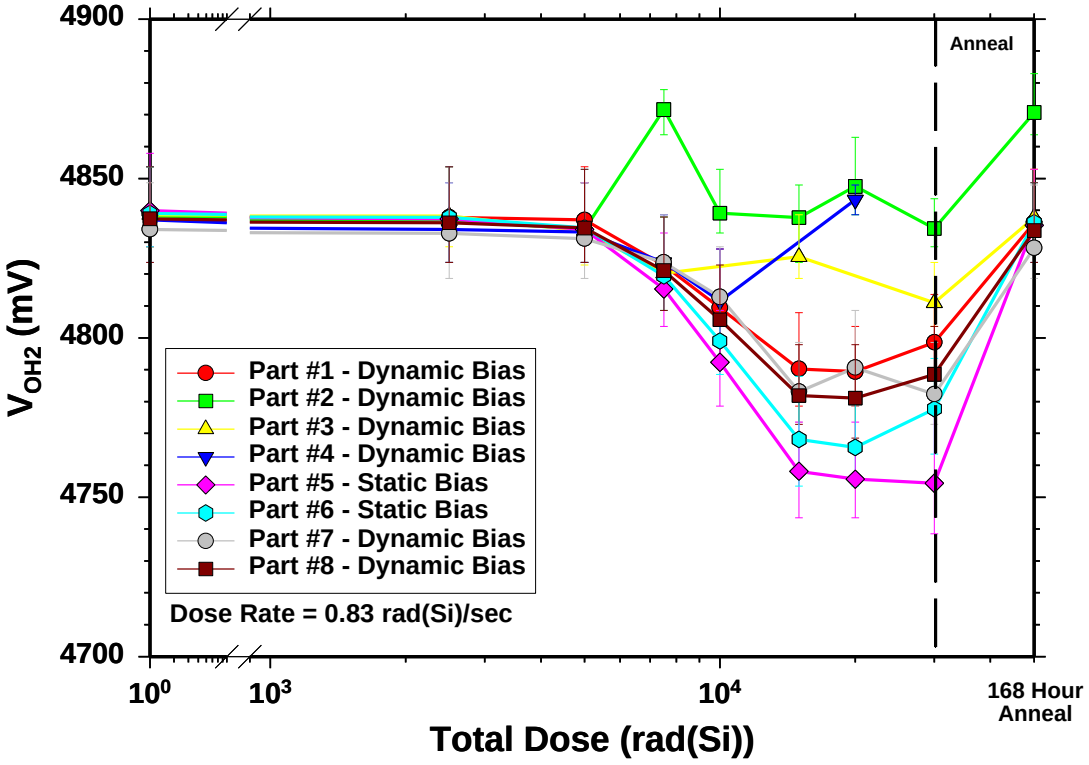

Effective Number of Bits
11
10
9
8
7
6
Anneal
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
10^0
10^3
10^4
168 Hour Anneal
Total Dose (rad(Si))


SFDR (dB)
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
-75
-80
Anneal
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
10^0
10^3
10^4
168 Hour Anneal
Total Dose (rad(Si))


Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
Anneal
168 Hour Anneal
THD (dB)
Total Dose (rad(Si))


Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
Anneal
168 Hour Anneal
V_{OL} (mV)
Total Dose (rad(Si))


4950
4900
4850
4800
4750
4700
V_{OH} (mV)
Anneal
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
10^0
10^3
10^4
168 Hour Anneal
Total Dose (rad(Si))


4900
4850
4800
4750
4700
V_{OH2} (mV)
Anneal
Part #1 - Dynamic Bias
Part #2 - Dynamic Bias
Part #3 - Dynamic Bias
Part #4 - Dynamic Bias
Part #5 - Static Bias
Part #6 - Static Bias
Part #7 - Dynamic Bias
Part #8 - Dynamic Bias
Dose Rate = 0.83 rad(Si)/sec
10^0
10^3
10^4
168 Hour Anneal
Total Dose (rad(Si))

Appendix B
LTC1272 Specification

12-Bit, 3µs, 250kHz Sampling A/D Converter

FEATURES

- AD7572 Pinout
- 12-Bit Resolution
- 3µs and 8µs Conversion Times
- On-Chip Sample-and-Hold
- Up to 250kHz Sample Rates
- 5V Single Supply Operation
- No Negative Supply Required
- On-Chip 25ppm/°C Reference
- 75mW (Typ) Power Consumption
- 24-Pin Narrow DIP and SOL Packages
- ESD Protected on All Pins

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing (DSP)
- Multiplexed Data Acquisition Systems
- Single Supply Systems

DESCRIPTION

The LTC1272 is a 3µs, 12-bit, successive approximation sampling A/D converter. It has the same pinout as the industry standard AD7572 and offers faster conversion time, on-chip sample-and-hold, and single supply operation. It uses LTBiCMOS™ switched-capacitor technology to combine a high speed 12-bit ADC with a fast, accurate sample-and-hold and a precision reference.

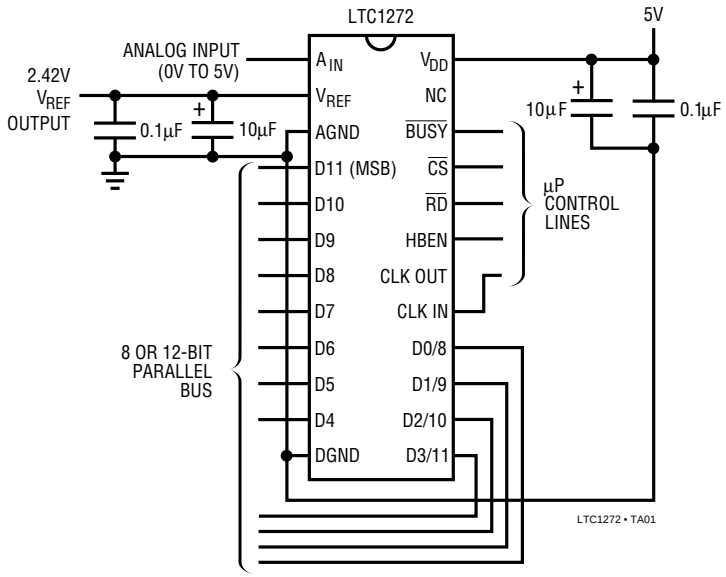
The LTC1272 operates with a single 5V supply but can also accept the 5V/–15V supplies required by the AD7572 (Pin 23, the negative supply pin of the AD7572, is not connected on the LTC1272). The LTC1272 has the same 0V to 5V input range as the AD7572 but, to achieve single supply operation, it provides a 2.42V reference output instead of the –5.25V of the AD7572. It plugs in for the AD7572 if the reference capacitor polarity is reversed and a 1µs sample-and-hold acquisition time is allowed between conversions.

The output data can be read as a 12-bit word or as two 8-bit bytes. This allows easy interface to both 8-bit and higher processors. The LTC1272 can be used with a crystal or an external clock and comes in speed grades of 3µs and 8µs.

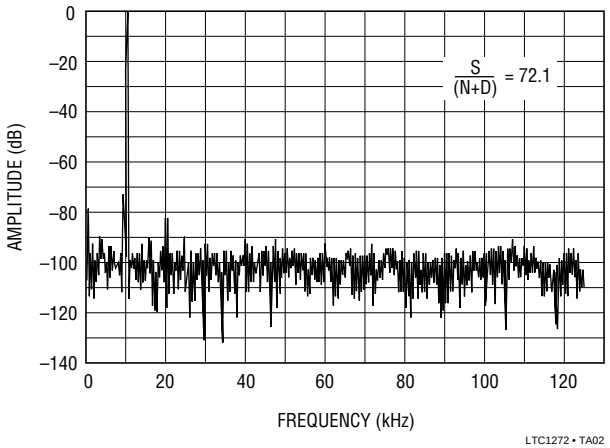
LTBiCMOS is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Single 5V Supply, 3µs, 12-Bit Sampling ADC



1024 Point FFT, f_S = 250kHz, f_{IN} = 10kHz



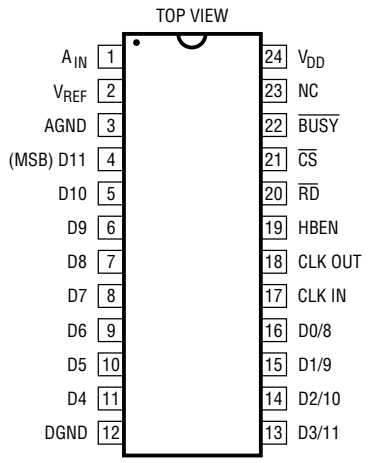
ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{DD}) 6V
Analog Input Voltage (Note 3) ..... –0.3V to 15V
Digital Input Voltage ..... –0.3V to 12V
Digital Output Voltage ..... –0.3V to V_{DD} + 0.3V
Power Dissipation 500mW

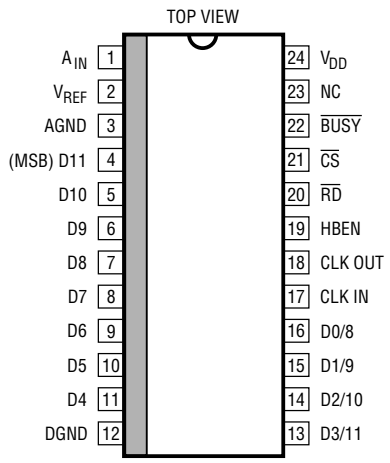
Operating Temperature Range
LTC1272-XAC, CC ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
24-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 100°C/W



S PACKAGE
24-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER	
CONVERSION TIME = 3µs	CONVERSION TIME = 8µs
LTC1272-3ACN LTC1272-3CCN	LTC1272-8ACN LTC1272-8CCN
S PACKAGE ONLY	
LTC1272-3ACS LTC1272-3CCS	LTC1272-8ACS LTC1272-8CCS

Consult factory for Industrial and Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Note 4)

PARAMETER	CONDITIONS		LTC1272-XA MIN	LTC1272-XA TYP	LTC1272-XA MAX	LTC1272-XC MIN	LTC1272-XC TYP	LTC1272-XC MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 5)	●			±1/2			±1	LSB
Differential Linearity Error		●			±1			±1	LSB
Offset Error		 ●			±3 ±4			±4 ±6	LSB LSB
Gain Error					±10			±15	LSB
Full-Scale Tempco	I_{OUT} (Reference) = 0	●		±5	±25		±10	±45	ppm/°C

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS		LTC1272-XA MIN	LTC1272-XA TYP	LTC1272-XA MAX	LTC1272-XC MIN	LTC1272-XC TYP	LTC1272-XC MAX	UNITS
V_{REF} Output Voltage (Note 6)	$I_{OUT} = 0$		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	$I_{OUT} = 0$	●		5	25		10	45	ppm/°C
V_{REF} Line Regulation	$4.75V \le V_{DD} \le 5.25V$, $I_{OUT} = 0$			0.01			0.01		LSB/V
V_{REF} Load Regulation (Sourcing Current)	$0 \le \lvert I_{OUT} \rvert \le 1mA$			2			2		LSB/mA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC1272-XA/C MIN	LTC1272-XA/C TYP	LTC1272-XA/C MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, $\overline{RD}$, HBEN, CLK IN	$V_{DD} = 5.25V$	●	2.4			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, $\overline{RD}$, HBEN, CLK IN	$V_{DD} = 4.75V$	●			0.8	V
I_{IN}	Input Current $\overline{CS}$, $\overline{RD}$, HBEN	$V_{IN} = 0V$ to V_{DD}	●			±10	µA
	Input Current CLK IN	$V_{IN} = 0V$ to V_{DD}	●			±20	µA
V_{OH}	High Level Output Voltage All Logic Outputs	$V_{DD} = 4.75V$ $I_{OUT} = -10\mu A$			4.7		V
		$I_{OUT} = -200\mu A$	●		4.0		V
V_{OL}	Low Level Output Voltage All Logic Outputs	$V_{DD} = 4.75V$, $I_{OUT} = 1.6mA$	●			0.4	V
I_{OZ}	High-Z Output Leakage D11-D0/8	$V_{OUT} = 0V$ to V_{DD}	●			±10	µA
C_{OZ}	High-Z Output Capacitance (Note 7)		●			15	pF
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{DD}$			10		mA
I_{DD}	Positive Supply Current	$\overline{CS} = \overline{RD} = V_{DD}$, $A_{IN} = 5V$	●		15	30	mA
P_D	Power Dissipation				75		mW

DYNAMIC ACCURACY (Note 4) f_{SAMPLE} = 250kHz (LTC1272-3), 111kHz (LTC1272-8)

SYMBOL	PARAMETER	CONDITIONS	LTC1272-XA/C MIN	LTC1272-XA/C TYP	LTC1272-XA/C MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	10kHz Input Signal		72		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	10kHz Input Signal		–82		dB
	Peak Harmonic or Spurious Noise	10kHz Input Signal		–82		dB

ANALOG INPUT (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC1272-XA/B/C MIN	LTC1272-XA/B/C TYP	LTC1272-XA/B/C MAX	UNITS
V_{IN}	Input Voltage Range	$4.75V \le V_{DD} \le 5.25V$	●	0		5	V
I_{IN}	Input Current		●			3.5	mA
C_{IN}	Input Capacitance				50		pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		0.45	1	µs

TIMING CHARACTERISTICS (Note 8)

SYMBOL	PARAMETER	CONDITIONS		LTC1272-XA/C MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time		●	0			ns
t_2	$\overline{RD}$ to $\overline{BUSY}$ Delay	C_L = 50pF			80	190	ns
		COM Grade	●			230	ns
t_3	Data Access Time After $\overline{RD}$↓	C_L = 20pF			50	90	ns
		COM Grade	●			110	ns
		C_L = 100pF			70	125	ns
		COM Grade	●			150	ns
t_4	$\overline{RD}$ Pulse Width			t_3			ns
		COM Grade	●	t_3			ns
t_5	$\overline{CS}$ to $\overline{RD}$ Hold Time		●	0			ns
t_6	Data Setup Time After $\overline{BUSY}$				40	70	ns
		COM Grade	●			90	ns
t_7	Bus Relinquish Time			20	30	75	ns
		COM Grade	●	20		85	ns
t_8	HBEN to $\overline{RD}$ Setup Time		●	0			ns
t_9	HBEN to $\overline{RD}$ Hold Time		●	0			ns
t_{10}	Delay Between $\overline{RD}$ Operations		●	200			ns
t_{11}	Delay Between Conversions			1			µs
t_{12}	Aperture Delay of Sample and Hold	Jitter <50ps			25		ns
t_{13}	CLK to $\overline{BUSY}$ Delay				80	170	ns
		COM Grade	●			220	ns
t_{CONV}	Conversion Time		●	12		13	CLK CYCLES

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together, unless otherwise noted.

Note 3: When the analog input voltage is taken below ground it will be clamped by an internal diode. This product can handle, with no external diode, input currents of greater than 60mA below ground without latch-up.

Note 4: V_{DD} = 5V, f_{CLK} = 4MHz for LTC1272-3, and 1.6MHz for LTC1272-8, $t_r = t_f$ = 5ns unless otherwise specified. For best analog performance, the LTC1272 clock should be synchronized to the $\overline{RD}$ and $\overline{CS}$ control inputs with at least 40ns separating convert start from the nearest clock edge.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: The LTC1272 has the same 0V to 5V input range as the AD7572 but, to achieve single supply operation, it provides a 2.42V reference output instead of the –5.25V of the AD7572. This requires that the polarity of the reference bypass capacitor be reversed when plugging an LTC1272 into an AD7572 socket.

Note 7: Guaranteed by design, not subject to test.

Note 8: V_{DD} = 5V. Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. See Figures 13 through 17.

PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input, 0V to 5V Unipolar Input.

V_{REF} (Pin 2): 2.42V Reference Output. When plugging into an AD7572 socket, reverse the reference bypass capacitor polarity and short the 10Ω series resistor.

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 4-11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11 to D0/8 (Pins 13-16): Three-State Data Outputs.

CLK IN (Pin 17): Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLK IN and CLK OUT.

CLK OUT (Pin 18): Clock Output. An inverted CLK IN signal appears at this pin.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7 to D0/8). See table below. HBEN also disables conversion starts when HIGH.

$\overline{RD}$ (Pin 20): Read Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The Chip Select Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output is low when a conversion is in progress.

NC (Pin 23): Not Connected Internally. The LTC1272 does not require negative supply. This pin can accommodate the –15V required by the AD7572 without problems.

V_{DD} (Pin 24): Positive Supply, 5V.

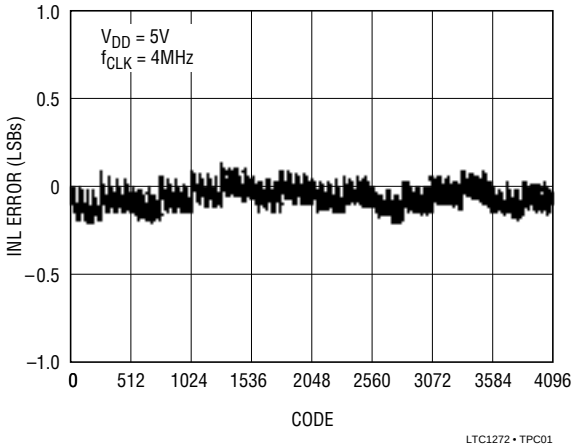
Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

TYPICAL PERFORMANCE CHARACTERISTICS

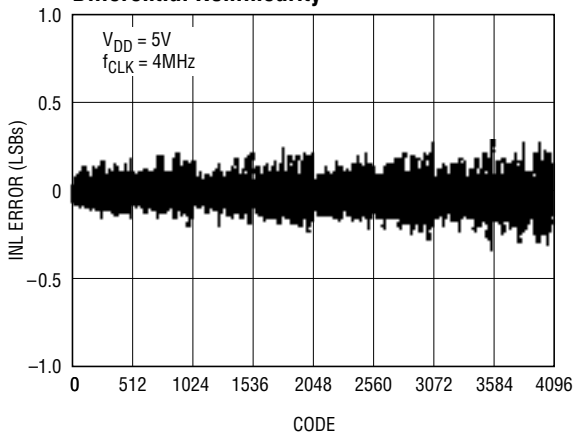
Integral Nonlinearity



LTC1272 • TPC01

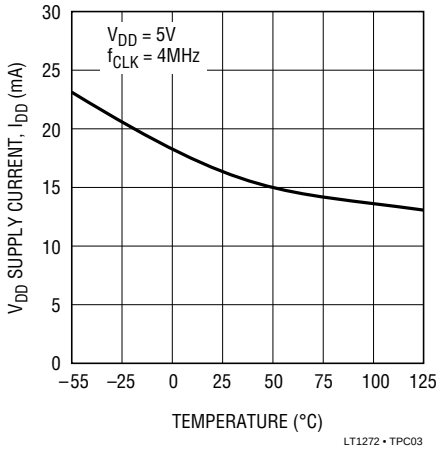
TYPICAL PERFORMANCE CHARACTERISTICS

Differential Nonlinearity



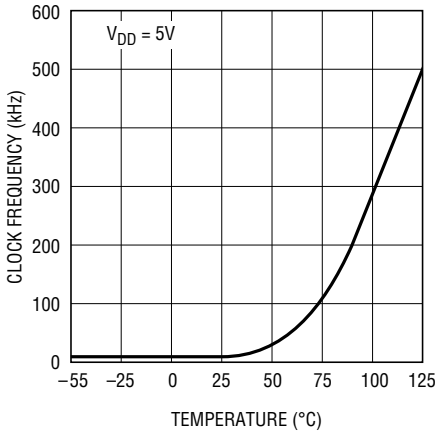
LTC1272 • TPC02

V_{DD} Supply Current vs Temperature



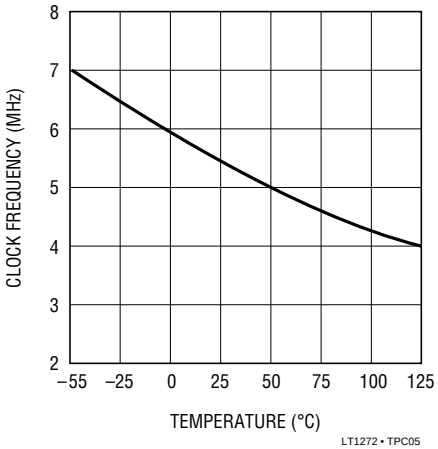
LT1272 • TPC03

Minimum Clock Frequency vs Temperature



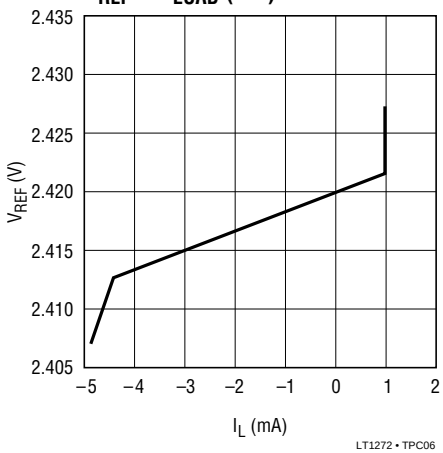
LT1272 • TPC04

Maximum Clock Frequency vs Temperature



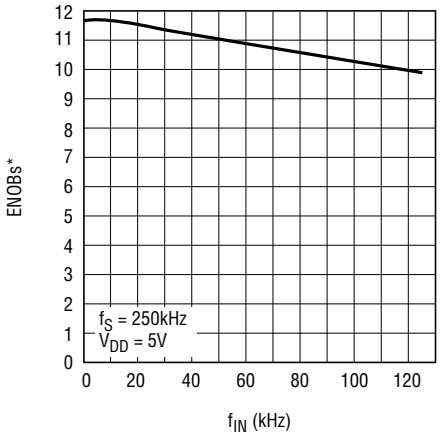
LT1272 • TPC05

V_{REF} vs I_{LOAD} (mA)



LT1272 • TPC06

LTC1272 ENOBs* vs Frequency



LT1272 • TPC07

*EFFECTIVE NUMBER OF BITS, ENOBs = $\frac{S/(N + D) - 1.76dB}{6.02}$

APPLICATIONS INFORMATION

Conversion Details

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor through a 300Ω/2.7kΩ divider. The voltage divider allows the LTC1272 to convert 0V to 5V input signals while operating from a 4.5V supply. The conversion has two phases: the sample phase and the convert phase. During the sample phase, the comparator offset is nulled by the feedback switch and the analog input is stored as a charge on the sample-and-hold capacitor, C_{SAMPLE}. This phase lasts from the end of the previous conversion until the next conversion is started. A minimum delay between conversions (t_{10}) of 1µs allows enough time for the analog input to be acquired. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The sample-and-hold capacitor is switched to ground injecting the analog input charge onto the comparator summing junction. This input charge is successively compared to binary weighted charges supplied by the capacitive DAC. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 50ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 50ns after a CLK IN edge until the conversion is finished. At the end of a conversion, the DAC output balances the A_{IN} output charge. The SAR contents (12-bit data word) which represent the A_{IN} input signal are loaded into a 12-bit latch.

Sample-and-Hold and Dynamic Performance

Traditionally A/D converters have been characterized by such specs as offset and full-scale errors, integral nonlinearity and differential nonlinearity. These specs are useful for characterizing an ADC's DC or low frequency signal performance.

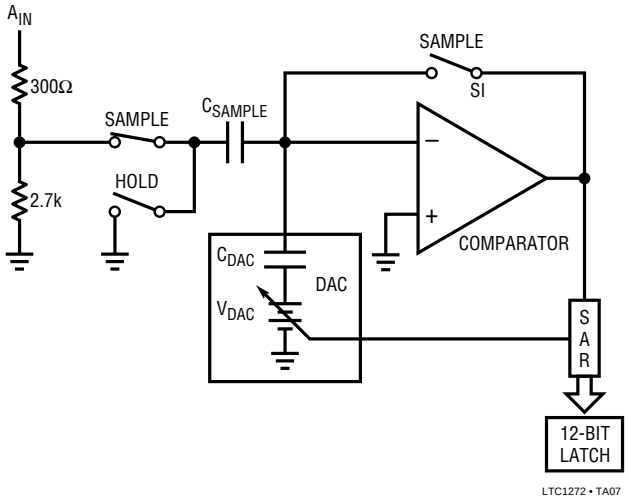


Figure 1. A_{IN} Input

These specs alone are not adequate to fully specify the LTC1272 because of its high speed sampling ability. FFT (Fast Fourrier Transform) test techniques are used to characterize the LTC1272's frequency response, distortion and noise at the rated throughput.

By applying a low distortion sine wave and analyzing the digital output using a FFT algorithm, the LTC1272's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1272 FFT plot.

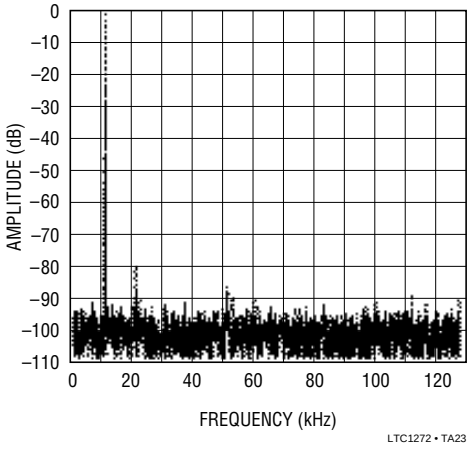


Figure 2. LTC1272 Non-Averaged, 1024 Point FFT Plot. f_S = 250kHz, f_{IN} = 10kHz

APPLICATIONS INFORMATION

Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. This includes distortion as well as noise products and for this reason it is sometimes referred to as Signal-to-Noise + Distortion [S/(N + D)]. The output is band limited to frequencies from DC to one half the sampling frequency. Figure 2 shows spectral content from DC to 125kHz which is 1/2 the 250kHz sampling rate.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an A/D and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02,$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 250kHz the LTC1272 maintains 11.5 ENOBs or better to 20kHz. Above 20kHz the ENOBs gradually decline, as shown in Figure 3, due to increasing second harmonic distortion. The noise floor remains approximately 90dB. The dynamic differential nonlinearity remains good out to 120kHz as shown in Figure 4.

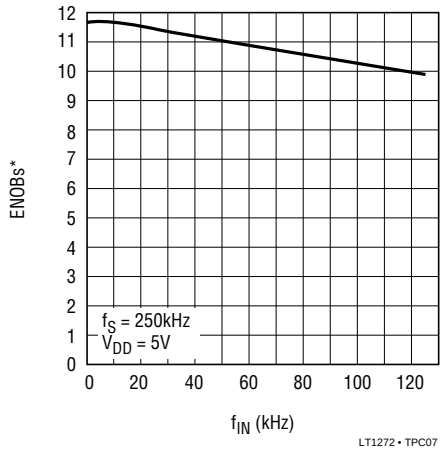


Figure 3. LTC1272 Effective Number of Bits (ENOBs) vs Input Frequency. f_S = 250kHz

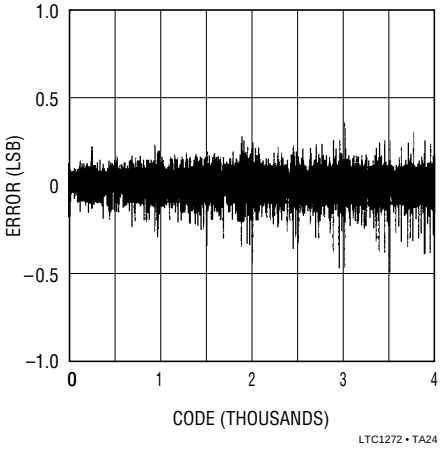


Figure 4. LTC1272 Dynamic DNL. f_{CLK} = 4MHz, f_S = 250kHz, f_{IN} = 122.25342kHz, V_{CC} = 5V

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The harmonics are limited to the frequency band between DC and one half the sampling frequency. THD is expressed as: 20 LOG $[\sqrt{V_2^2 + V_3^2 + ... + V_N^2} / V_1]$ where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Clock and Control Synchronization

For best analog performance, the LTC1272 clock should be synchronized to the $\overline{CS}$ and $\overline{RD}$ control inputs as shown in Figure 5, with at least 40ns separating convert start from the nearest CLK IN edge. This ensures that transitions at CLK IN and CLK OUT do not couple to the analog input and get sampled by the sample-and-hold. The magnitude of this feedthrough is only a few millivolts, but if CLK and convert start ($\overline{CS}$ and $\overline{RD}$) are asynchronous, frequency components caused by mixing the clock and convert signals may increase the apparent input noise.

When the clock and convert signals are synchronized, small endpoint errors (offset and full-scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be eliminated by ensuring that the start of a conversion ($\overline{CS}$ and $\overline{RD}$'s falling edge) does not occur within 40ns of a clock edge, as in

APPLICATIONS INFORMATION

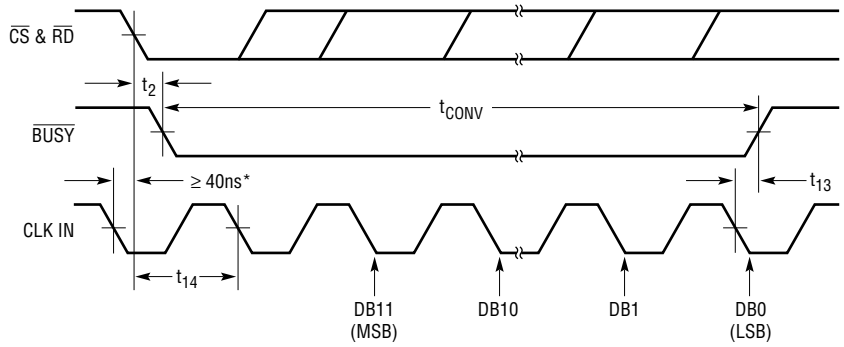


Figure 5. $\overline{RD}$ and CLK IN for Synchronous Operation

Figure 5. Nevertheless, even without observing this guideline, the LTC1272 is still compatible with AD7572 synchronization modes, with no increase in linearity error. This means that either the falling or rising edge of CLK IN may be near $\overline{RD}$'s falling edge.

Driving the Analog Input

The analog input of the LTC1272 is much easier to drive than that of the AD7572. The input current is not modulated by the DAC as in the AD7572. It has only one small current spike from charging the sample-and-hold capacitor at the end of the conversion. During the conversion the analog input draws only DC current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion is started. Any op amp that settles in 1μs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the LTC1272 A_{IN} input include the LT1006 and LT1007 op amps.

Internal Clock Oscillator

Figure 6 shows the LTC1272 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for ADC timing. Alternatively the crystal/resonator may be omitted and an external clock source may be

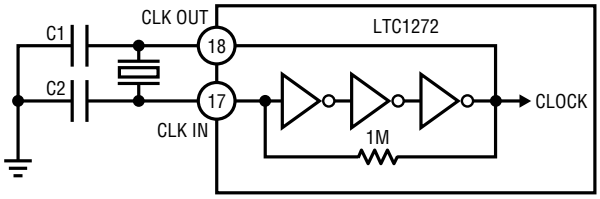


Figure 6. LTC1272 Internal Clock Circuit

connected to CLK IN. For an external clock the duty cycle is not critical. An inverted CLK IN signal will appear at the CLK OUT pin as shown in the operating waveforms of Figure 7. Capacitance on the CLK OUT pin should be minimized for best analog performance.

Internal Reference

The LTC1272 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V ±1%. It is internally connected to the DAC and is also available at pin 2 to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10μF tantalum in parallel with a 0.1μF ceramic). A simplified schematic of the reference with its recommended decoupling is shown in Figure 8.

APPLICATIONS INFORMATION

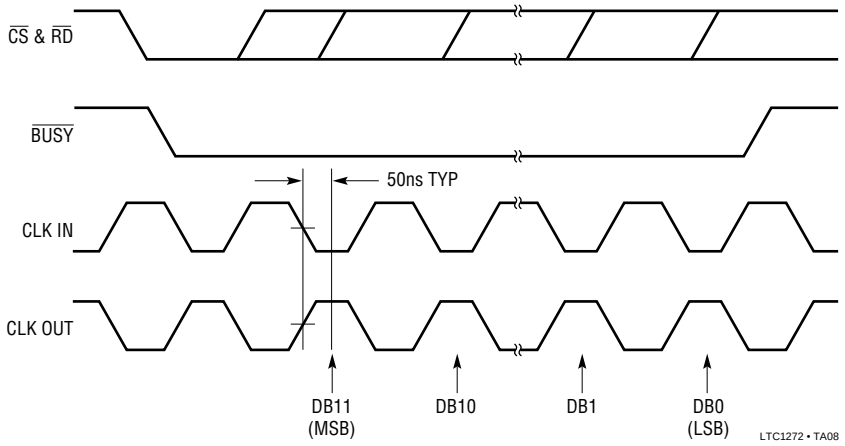


Figure 7. Operating Waveforms Using an External Clock Source for CLK IN

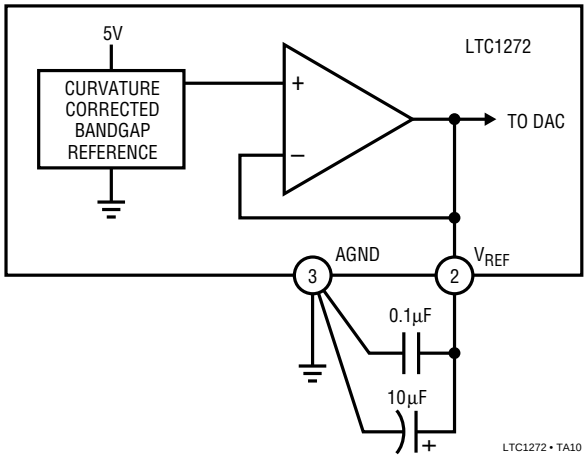


Figure 8. LTC1272 Internal 2.42V Reference

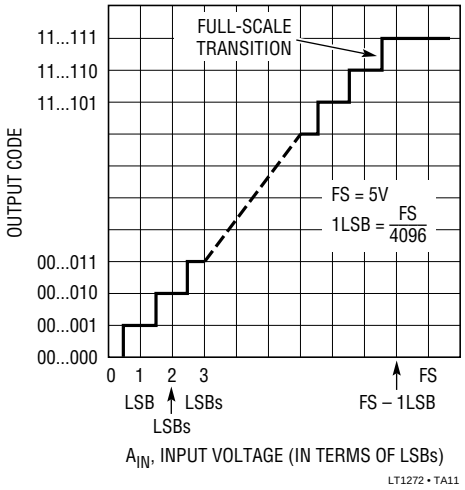


Figure 9. LTC1272 Ideal Input/Output Transfer Characteristic

Unipolar Operation

Figure 9 shows the ideal input/output characteristic for the 0V to 5V input range of the LTC1272. The code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . . FS – 3/2LSBs). The output code is natural binary with 1 LSB = FS/4096 = (5/4096)V = 1.22mV.

Unipolar Offset and Full-Scale Error Adjustment

In applications where absolute accuracy is important, then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving A_{IN} (i.e., A1 in Figure 10). For zero offset error apply 0.61mV (i.e., 1/2LBS) at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817V (i.e., FS – 3/2LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS INFORMATION

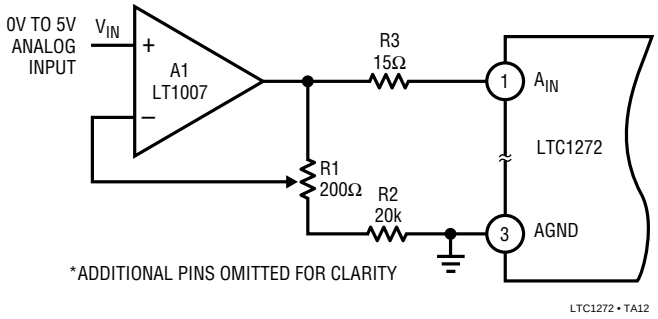


Figure 10. Unipolar 0V to 5V Operation with Gain Error Adjust

Application Hints

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1272 a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the LTC1272. The analog input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the LTC1272, as shown in Figure 11. Pin 12 (LTC1272 DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to A_{IN} and signal return leads from AGND (pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the LTC1272 data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the LTC1272 data bus.

Timing and Control

Conversion start and data read operations are controlled by three LTC1272 digital inputs; HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 12 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

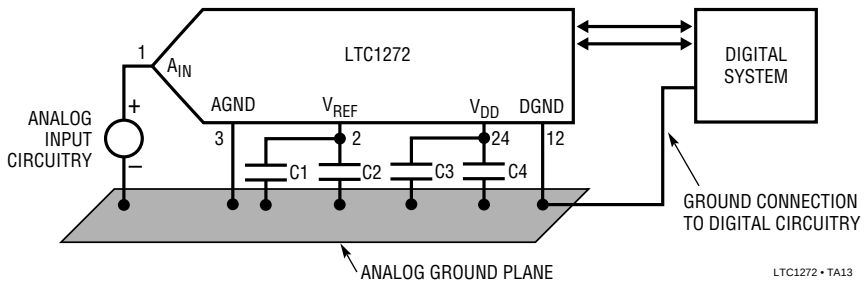


Figure 11. Power Supply Grounding Practice

APPLICATIONS INFORMATION

There are two modes of operation as outlined by the timing diagrams of Figures 13 to 17. Slow Memory Mode is designed for microprocessors which can be driven into a Wait state, a Read operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete.

The second is the ROM Mode which does not require microprocessor Wait states. A Read operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

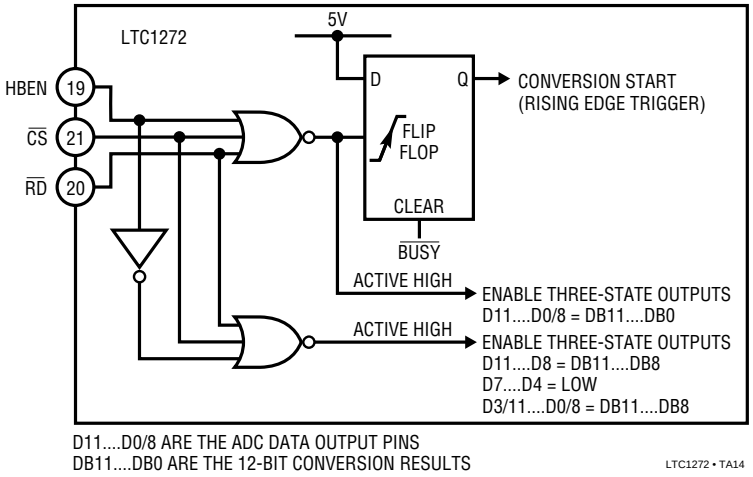


Figure 12. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

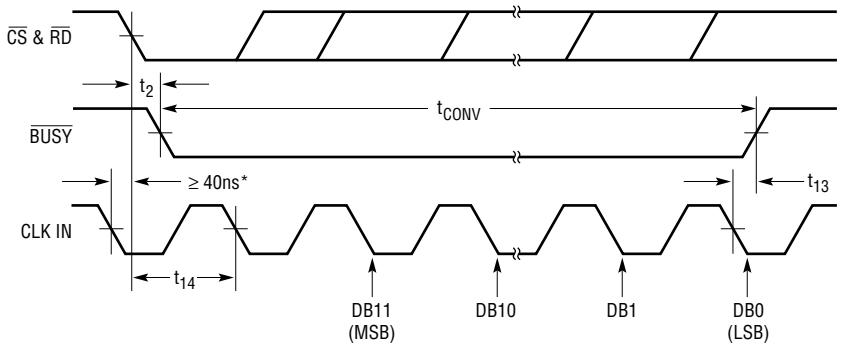


Figure 13. $\overline{RD}$ and CLK IN for Synchronous Operation

Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = Low

	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 13	PIN 14	PIN 15	PIN 16
Data Outputs*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = Low	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = High	DB11	DB10	DB9	DB8	Low	Low	Low	Low	DB11	DB10	DB9	DB8

Note: *D11 . . . D0/8 are the ADC data output pins
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB

APPLICATIONS INFORMATION

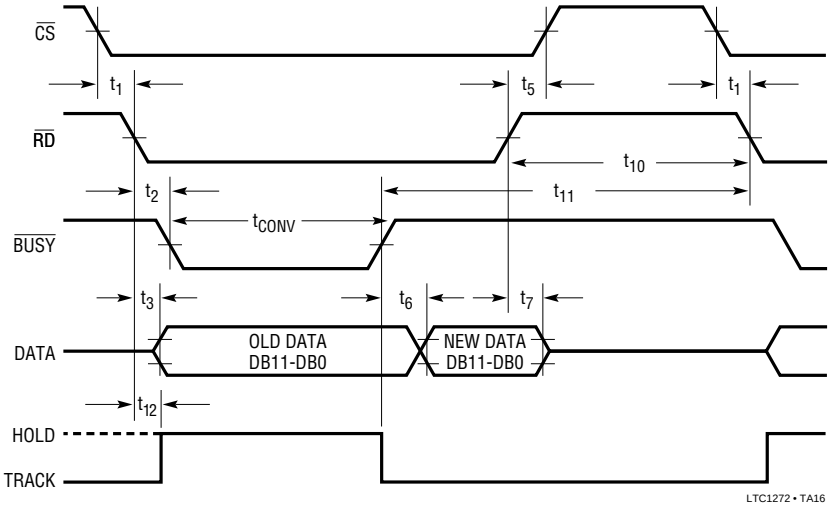


Figure 14. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Data Format

The output data format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7. . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12 bits of conversion data onto the lower D7. . . D0/8 outputs (4MSBs or 8LSBs) where it can be read in two read cycles. The 4MSBs always appear on D11 . . . D8 whenever the three-state output drives are turned on.

Slow Memory Mode, Parallel Read (HBEN = Low)

Figure 14 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the LTC1272 acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11 . . . D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Slow Memory Mode, Parallel Read. See Figure 15 timing diagram and Table 3 data bus status. At the end of conversion the low data byte (DB7 . . . DB0) is read from the ADC. A second Read operation with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4MSBs appear on data outputs D11 . . . D8 during the two Read operations above.

ROM Mode, Parallel Read (HBEN = Low)

The ROM Mode avoids placing a microprocessor into a Wait state. A conversion is started with a Read operation and the 12 bits of data from the previous conversion is available on data outputs D11 . . . D0/8 (see Figure 16 and Table 4). This data may be disregarded if not required. A second Read operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the LTC1272 conversion time plus the 1µs minimum delay between conversions must be allowed between Read operations.

APPLICATIONS INFORMATION

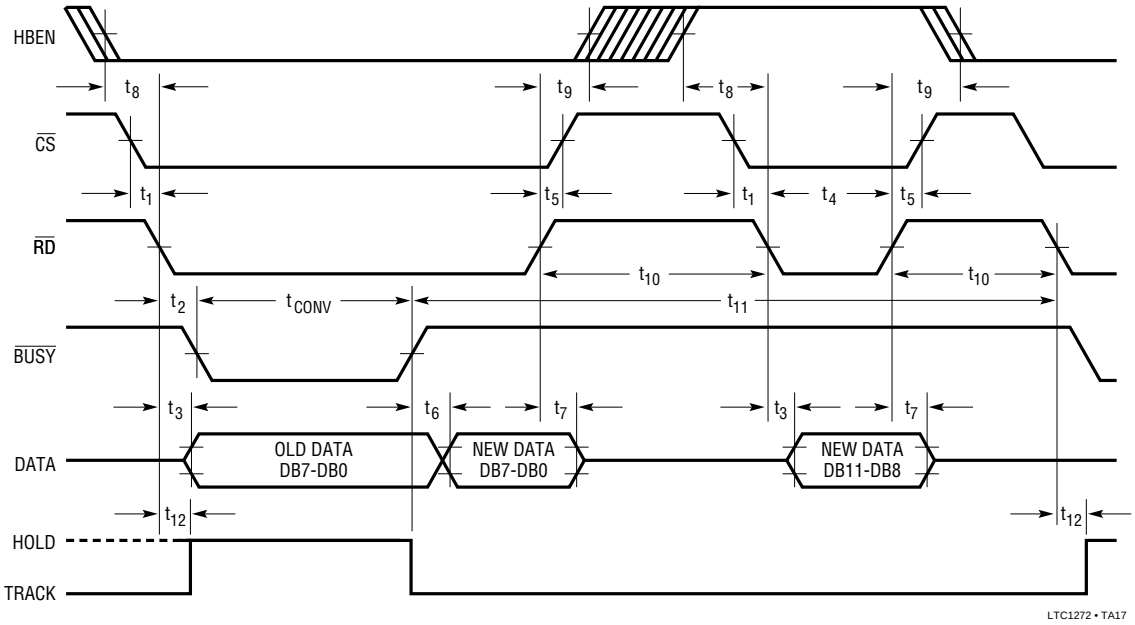


Figure 15. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

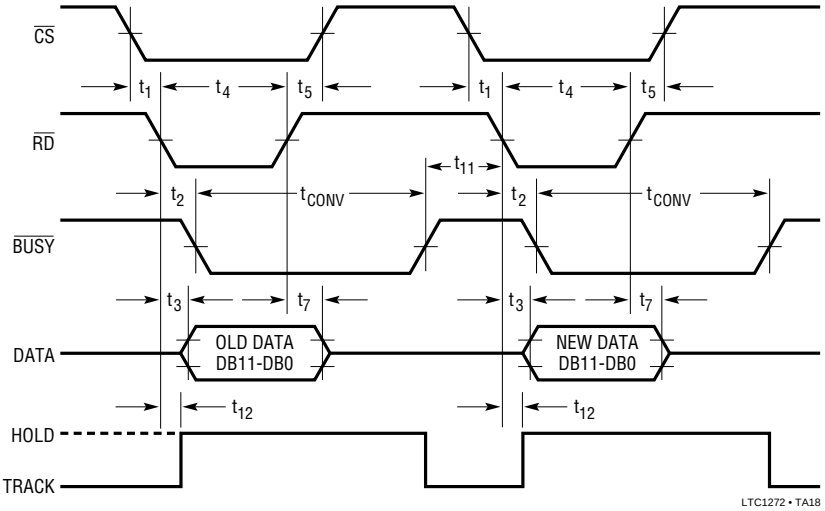


Figure 16. ROM Mode, Parallel Read Timing Diagram

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

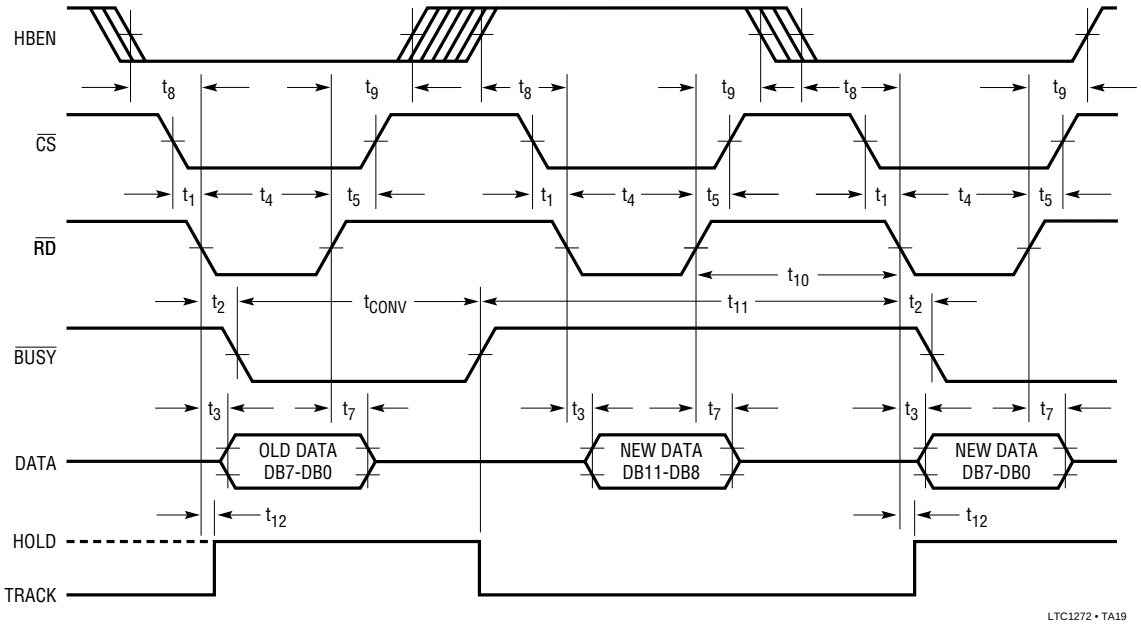


Figure 17. ROM Mode, Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

ROM Mode, Two Byte READ

As previously mentioned for a two byte read, only data outputs D7 . . . D0/8 are used. Conversion is started in the normal way with a Read operation and the data output status is the same as the ROM Mode, Parallel Read. See Figure 17 timing diagram and Table 5 data bus status. Two more Read operations are required to access the new conversion result. A delay equal to the LTC1272 conversion time must be allowed between conversion start and the second data Read operation. The second Read operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11 . . . DO18. A third read operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4 MSB's appear on data outputs D11 . . . D8 during all three read operations above.

Microprocessor Interfacing

The LTC1272 is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally connected to the microprocessor address bus.

MC68000 Microprocessor

Figure 18 shows a typical interface for the MC68000. The LTC1272 is operating in the Slow Memory Mode. Assuming the LTC1272 is located at address C000, then the following single 16-bit Move instruction both starts a conversion and reads the conversion result:

```
Move.W $C000,D0
```

APPLICATIONS INFORMATION

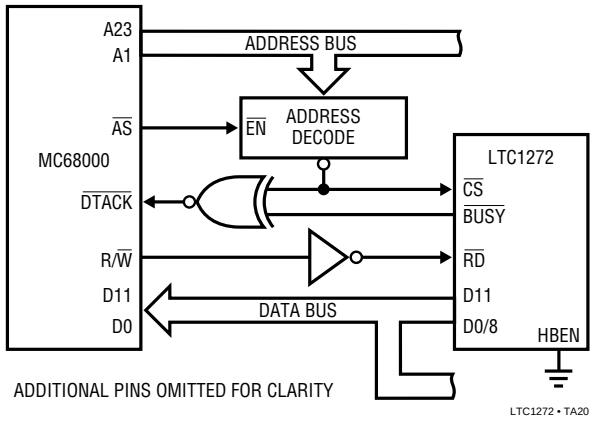


Figure 18. LTC1272 MC68000 Interface

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the MC68000 is forced into a Wait state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the microprocessor.

8085A, Z80 Microprocessor

Figure 19 shows a LTC1272 interface for the Z80 and 8085A. The LTC1272 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN, so that an even address (HBEN = LOW) to the LTC1272 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit Load instruction below.

For the 8085A	LHLD (B000)
For the Z80	LDHL, (B000)

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to Wait for the LTC1272 conversion. No Wait states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 20 shows an LTC1272 TMS32010 interface. The LTC1272 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The LTC1272 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

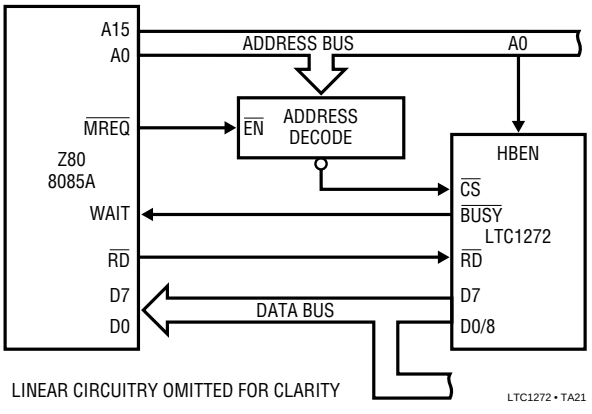


Figure 19. LTC1272 8085A/Z80 Interface

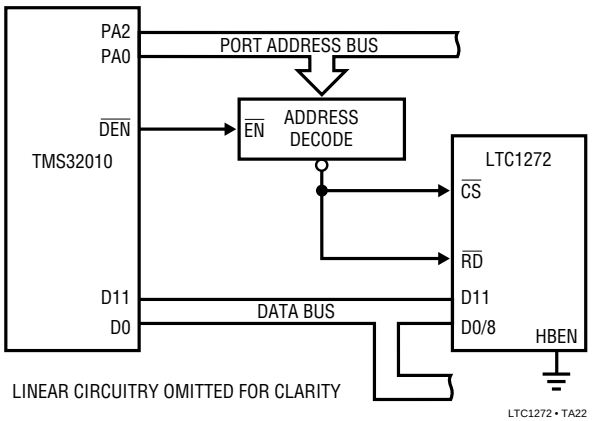


Figure 20. LTC1272 TMS32010 Interface

APPLICATIONS INFORMATION

Compatibility with the AD7572

Figure 21 shows the simple, single 5V configuration recommended for new designs with the LTC1272. If an AD7572 replacement or upgrade is desired, the LTC1272 can be plugged into an AD7572 socket with minor modifications. It can be used as a replacement or to upgrade with sample-and-hold, single supply operation and reduced power consumption.

The LTC1272, while consuming less power overall than the AD7572, draws more current from the 5V supply (it draws no power from the –15V supply). Also, a 1µs minimum time between conversions must be provided to allow the sample-and-hold to reacquire the analog input. Figure 22 shows that if the clock is synchronous with $\overline{CS}$ and $\overline{RD}$, it is only necessary to short out the 10Ω series resistor and reverse the polarity of the 10µF bypass capacitor on the V_{REF} pin. The –15V supply is not required and can be removed, or, because there is no internal connection to pin 23, it can remain unmodified. The clock can be considered synchronous with $\overline{CS}$ and $\overline{RD}$ in cases where the LTC1272 CLK IN signal is derived from the same clock as the microprocessor reading the LTC1272.

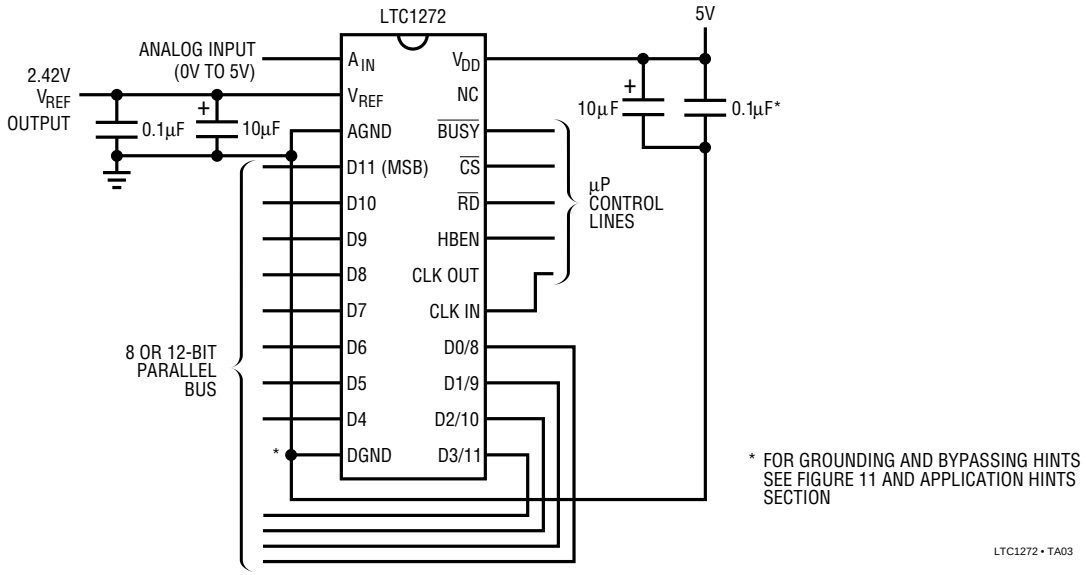


Figure 21. Single 5V Supply, 3µs, 12-Bit Sampling ADC

APPLICATIONS INFORMATION

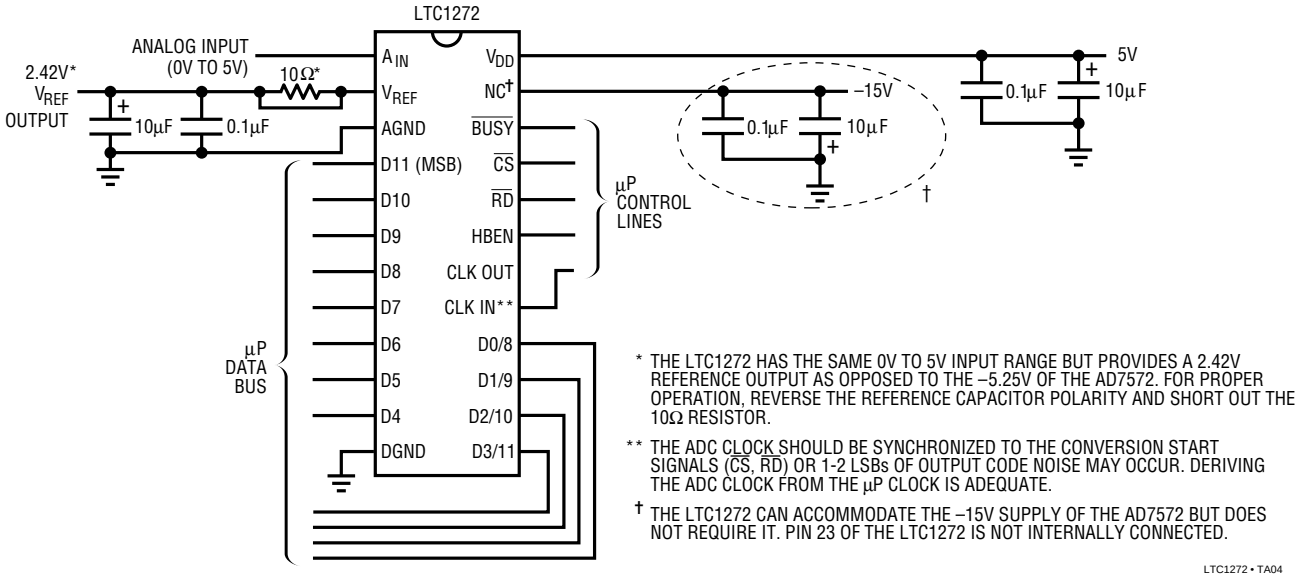
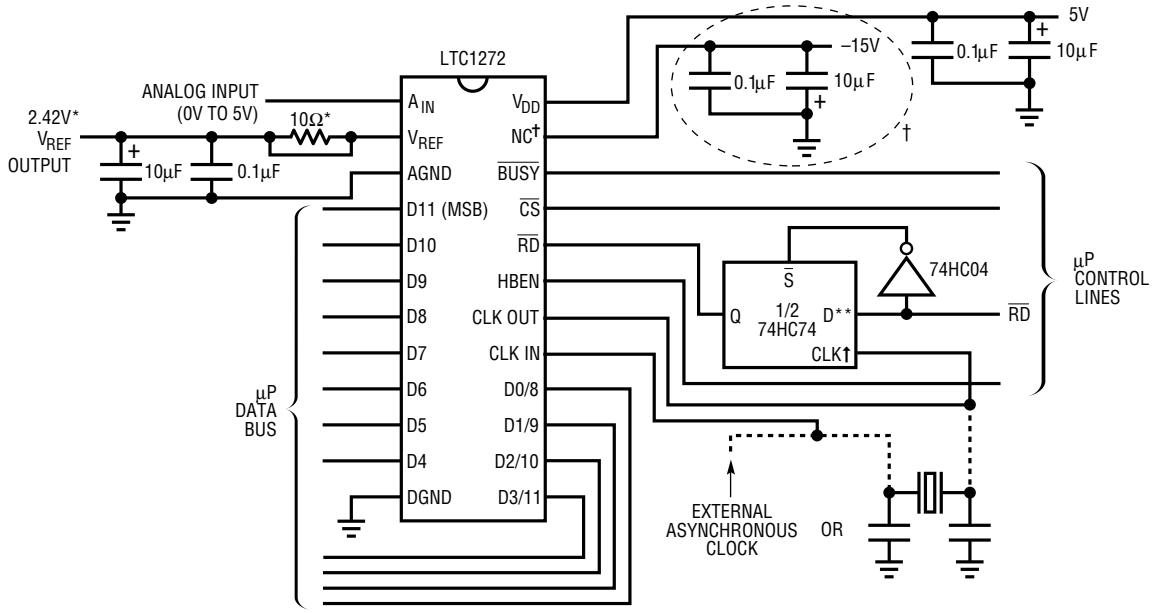


Figure 22. Plugging the LTC1272 into an AD7572 Socket
Case 1: Clock Synchronous with $\overline{CS}$ and $\overline{RD}$

If the clock signal for the AD7572 is derived from a separate crystal or other signal which is not synchronous with the microprocessor clock, then the signals need to be synchronized for the LTC1272 to achieve best analog performance (see Clock and Control Synchronization). The best way to synchronize these signals is to drive the CLK IN pin of the LTC1272 with a derivative of the processor clock, as mentioned above and shown in Figure 22. Another way, shown in Figure 23, is to use a flip-flop to synchronize the $\overline{RD}$ to the LTC1272 with the CLK IN signal. This method will work but has two disavantages over the first: because the $\overline{RD}$ is delayed by the flip-flop, the actual conversion start and the enabling of the LTC1272's $\overline{BUSY}$ and data outputs can take up to one CLK IN cycle to respond to a $\overline{RD}\downarrow$ convert command from the processor. The sampling of the analog input no longer occurs at the processor's falling $\overline{RD}$ edge but may be delayed as much as one CLK IN cycle. Although the LTC1272 will still exhibit excellent DC performance, the flip-flop will introduce jitter into the sampling which may reduce the usefulness of this method for AC systems.

APPLICATIONS INFORMATION



* THE LTC1272 HAS THE SAME 0V TO 5V INPUT RANGE BUT PROVIDES A 2.42V REFERENCE OUTPUT AS OPPOSED TO THE –5.25V OF THE AD7572. FOR PROPER OPERATION, REVERSE THE REFERENCE CAPACITOR POLARITY AND SHORT OUT THE 10Ω RESISTOR.

** THE D FLIP-FLOP SYNCHRONIZES THE CONVERSION START SIGNAL ($\overline{RD}$↓) TO THE ADC CLK_{OUT} SIGNAL TO PREVENT OUTPUT CODE NOISE WHICH OCCURS WITH AN ASYNCHRONOUS CLOCK.

† THE LTC1272 CAN ACCOMMODATE THE –15V SUPPLY OF THE AD7572 BUT DOES NOT REQUIRE IT. PIN 23 OF THE LTC1272 IS NOT INTERNALLY CONNECTED.

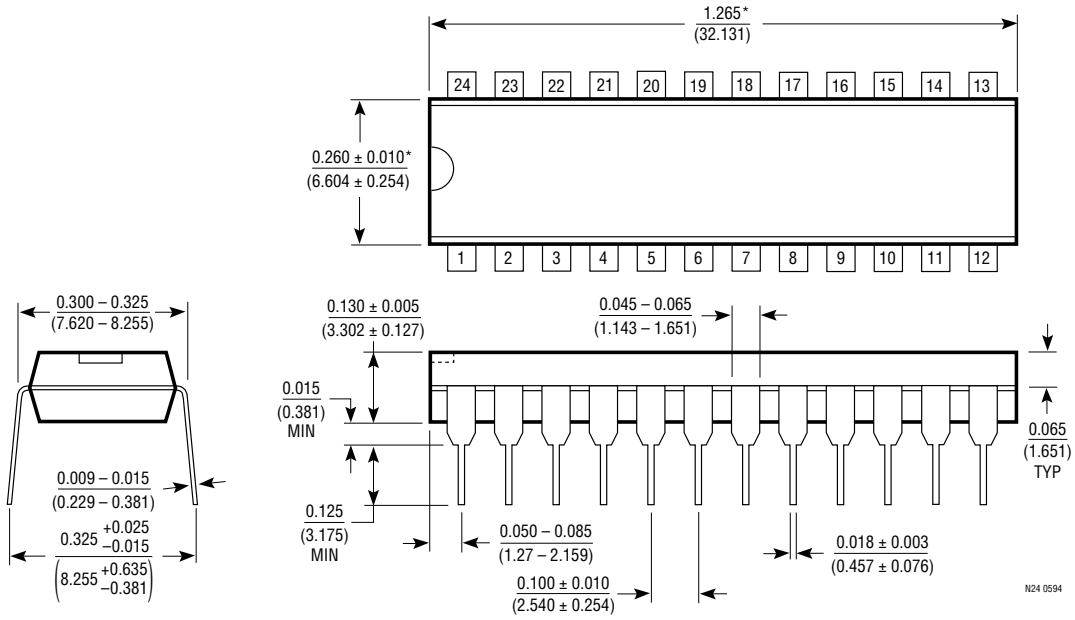
LTC1272 • TA05

Figure 23. Plugging the LTC1272 into an AD7572 Socket Case 2: Clock Not Synchronous with $\overline{CS}$ and $\overline{RD}$

PACKAGE DESCRIPTION

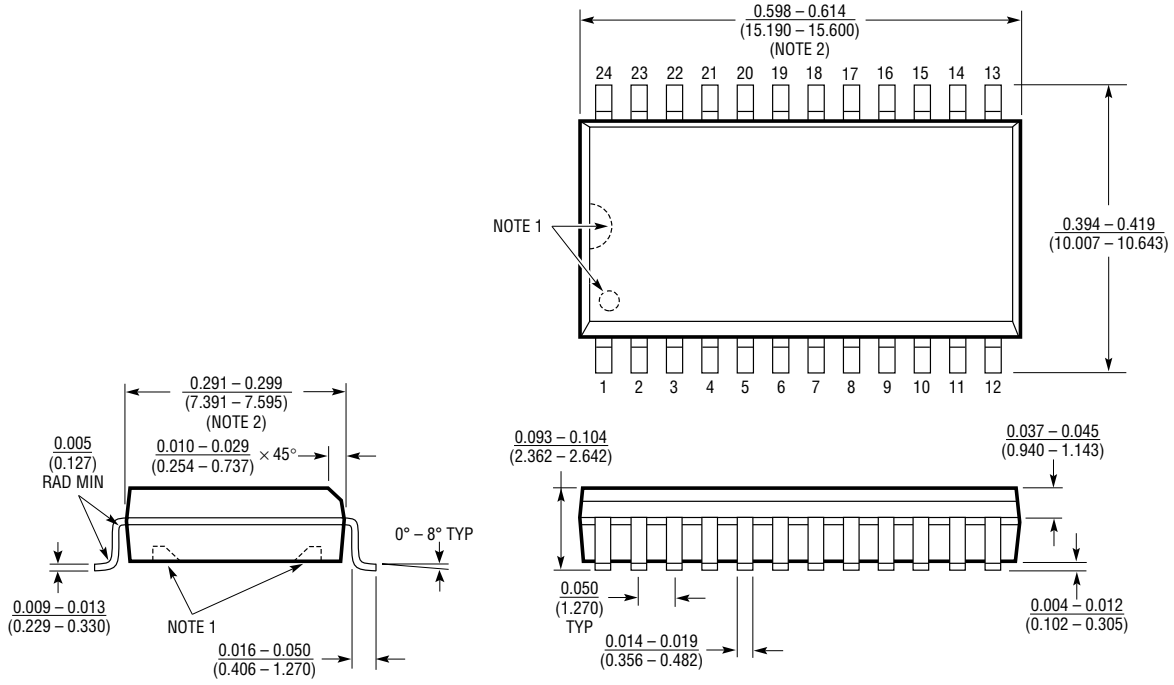
Dimensions in inches (millimeters) unless otherwise noted.

N Package
24-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

SO Package
24-Lead Plastic SOL



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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