Fermilab

Particle Physics Division/CDF Upgrade Project

Specification for TRigger And Clock + Event Readout Module (TRACER)

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1.0 Introduction

The ***TR****igger* ***A****nd* ***C****lock* + ***E****vent* ***R****eadout* Module (TRACER) performs the role of system interface for the front end crates to the rest of the upgraded CDF system. It will be assumed that the reader is familiar with the readout system described in CDF/DOC/TRIGGER/CDFR/2288 “A Standard Front-End and Trigger VMEbus Based Readout Crate for the CDF Upgrade - The CDF Readout Crate”.

One of the TRACER's functions is to provide an interface to the Master Clock. The TRACER is used to fanout the precision 132ns clock and three clocking gates: Beam Zero, Beam Crossing, and Abort. The TRACER does this by driving the signals it receives onto the CDF custom backplane (see CDF/DOC/TRIGGER/CDFR/2388) where they are then readily available to all modules plugged into the crate. No timing adjustment is done to any signals from the Master Clock. Any custom tuning of the arrival of the signals will be done in the Clock Fanout Modules.

A second TRACER function is to provide an interface to the Trigger System Interface (TSI). The TRACER is used to fanout all trigger and control information received from the TSI. The TRACER receives encoded information from an optical link, decodes it and passes it onto the CDF custom backplane. These signals are used by the ADMEMs and other front-end modules to either pass an event fragment into one of four Level 2 readout buffers or to throw it away.

The TRACER also provides a path for sending the event data to the VMEbus Readout Boards (VRBs). Event data may be transmitted in two ways: the TRACER may act as a "spy" on the backplane and place backplane data into its Event FIFO, or it can receive data written directly into its Event FIFO from the VRC (VME Readout Controller). Once data exists in the Event FIFO, a sequencer onboard the TRACER will readout the event data, serialize it and then transmit the data to the VRB modules over fiber optic cables. The VRB will transmit the signal VRB_BUSY back to the TRACER if at any time the VRB cannot accept the next event. If VRB_BUSY is detected by the TRACER, data transmission will be held off until the condition clears.

Finally, the TRACER provides a means by which to issue a crate reset. The VMEbus signal SYSRESET* will be pulsed low on the backplane if a reset pulse is detected from the CDF Reset Crate. An RS-422 signal is sent from the Reset Crate to a TRACER front panel connection if a crate reset is desired. A crate reset ability is required in the event of a CPU board hanging. NOTE that this reset ability is separate from the TSI CDF_RECOVER~ signal which serves to reset L1 pipeline pointers.

Figure 1 provides a system overview and shows where the TRACER fits in. Figure 2 provides a block diagram of the TRACER.

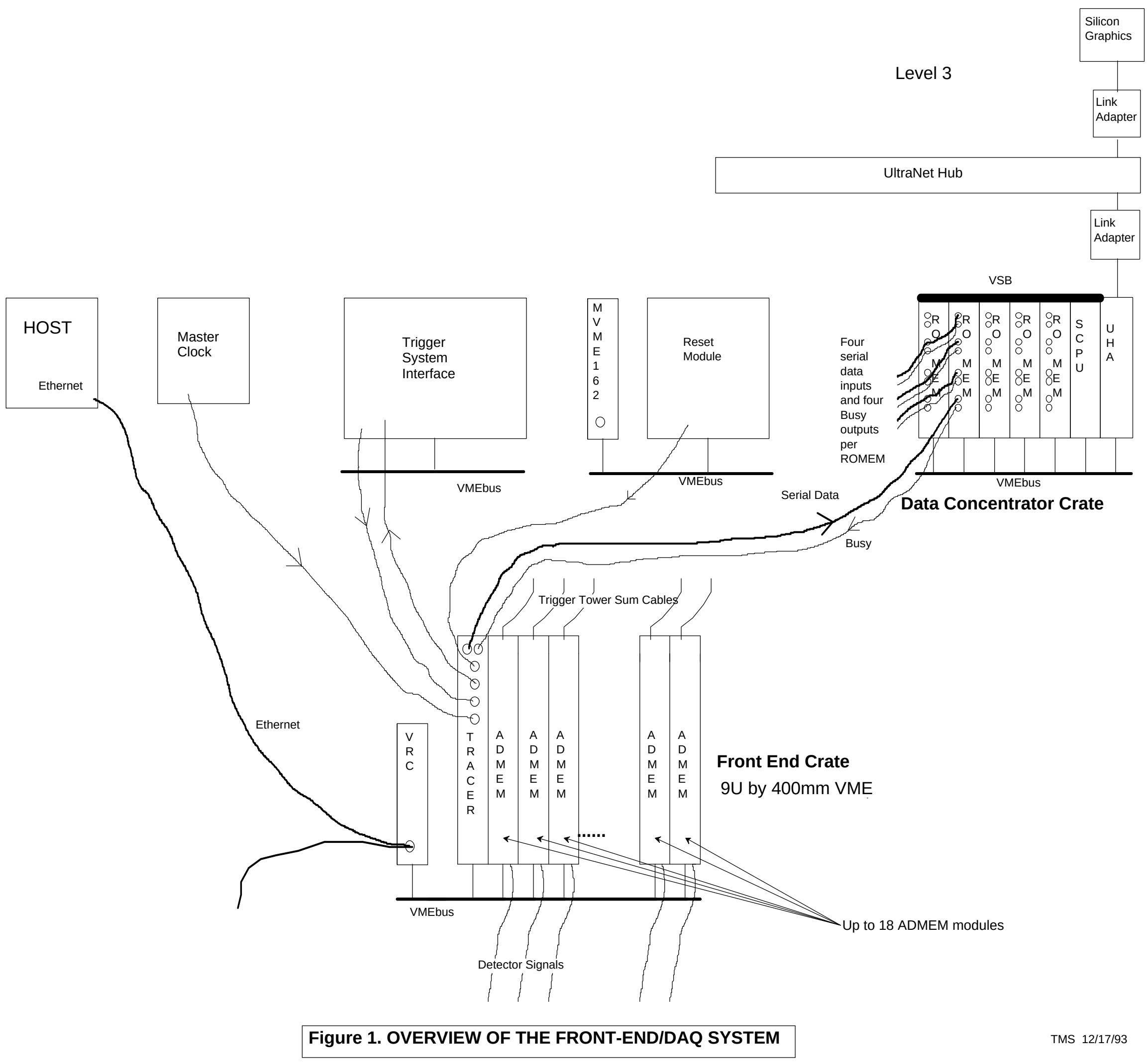


Figure 1. Block Diagram of Calorimetry DAQ System

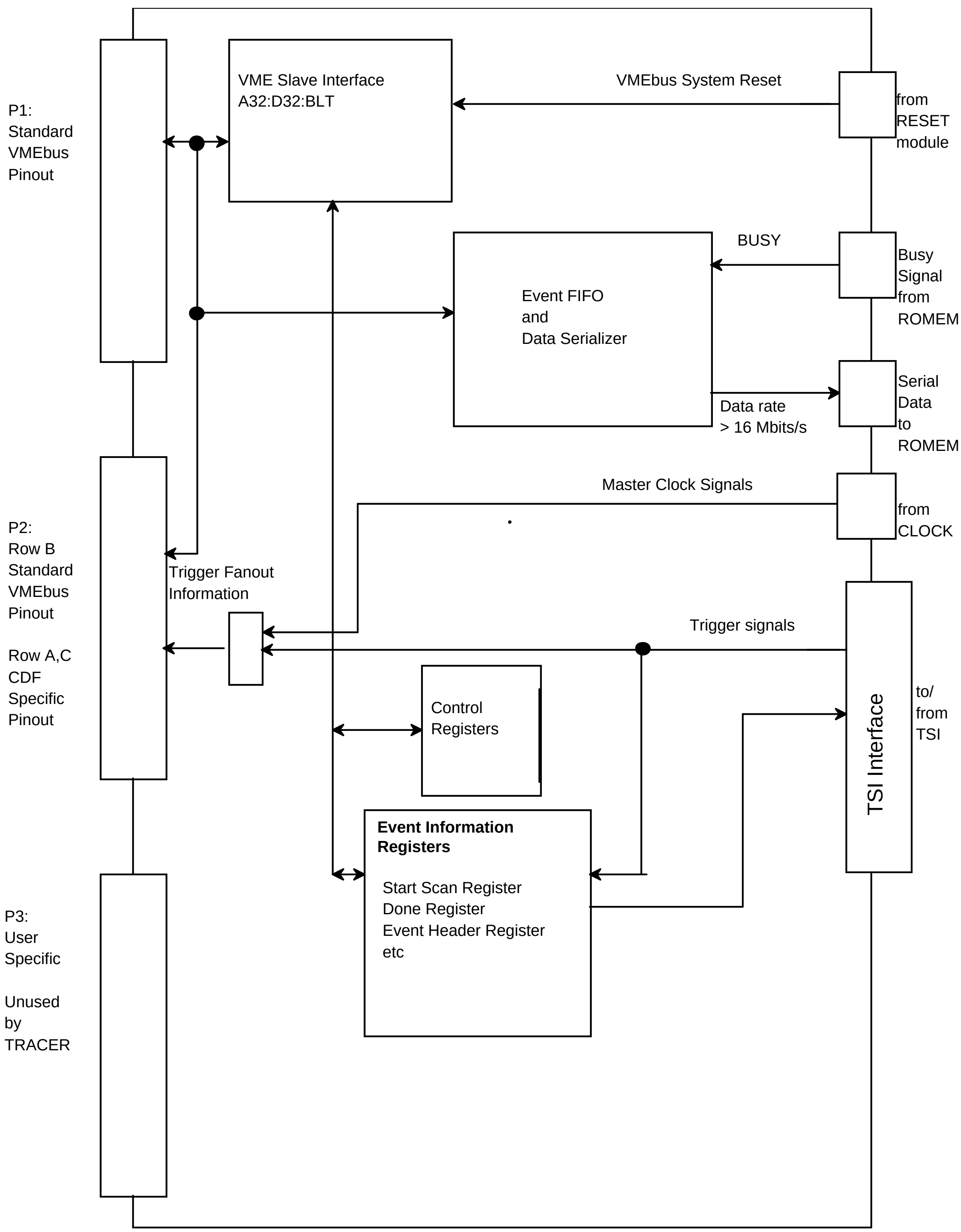


Figure 2 Block Diagram of Trigger Fanout/Crate Monitor/Spy Module

2.0 Interface to the Master Clock

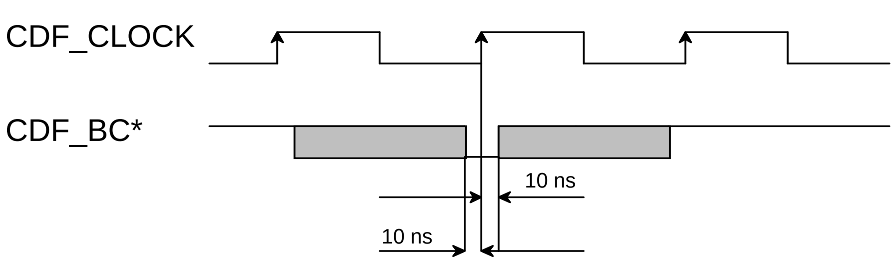
The TRACER provides a front panel connection to receive a cable from the Master Clock. The Master Clock will provide the precisely timed 132 ns clock signal as well as gates which indicate the Beam Zero Crossing, Beam Crossing and Abort Gaps. The Master Clock signals are received as differential LVDS signals. The TRACER will provide a 100 ohm terminating input resistor for each of the signals. A 8-pin Shielded Data Link style connector will be provided to receive the cable from the Master Clock (see Appendix C). The front panel connector pinout will be as follows:

Pin	**Signal**	
1	Master_Clock	(132 ns clock)
2	Master_Clock*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

The TRACER will receive these signals and drive the following backplane signals:

CDF_CLK
CDF_CLK* - 132 ns clock; accurately timed *differential PECL* signal delivered by the Master Clock. CDF_CLK is the only precisely timed signal. All other signals are considered gates to the rising edge of CDF _CLK. All CDF backplane signals are guaranteed to be valid for 10ns on either side of the rising edge of CDF_CLK.
CDF_BC* - Beam Crossing (TTL)
CDF_B0* - Bunch 0 (TTL)
CDF_ABORT* - Abort Gap (TTL)

The TRACER will simply buffer these signals to the backplane - No timing adjustments will be done. CDF_B0~, CDF_BC~ and CDF_ABORT~ are gates to the rising edge of the CDF_CLK signal. They are guaranteed to have at least a 10 ns setup and hold time with respect to the clock edge.



Backplane Timing Example of CDF_CLOCK and a Clock Gate

3.0 Interface to Trigger System Interface(TSI)

3.1 TSI <-> TRACER Optic Link

The TRACER will provide an interface to the TSI. An optical link using TAXIchip (AM7969-175JC) protocol, AMP optical receivers (AMP 269050-1), and operating at two times the CDF_CLK, provides a means for the TSI to issue commands. The TRACER will take the signals that it receives from the TSI, decode them and drive the appropriate trigger signals out onto the custom CDF VMEbus backplane. The TSI <-> TRACER protocol is described in the note "**Trigger Supervisor Protocols for Run II**" written by the CDF Group of Yale University.

The following backplane trigger signals will be driven by the TRACER as the result of TSI commands:

FROM TSI		**Backplane Signal driven by TRACER**	
L1 Word	bit 2	CDF_L1A*	- Level 1 Accept
	bit 3	CDF_L1R*	- Level 1 Reject
	bit 4	CDF_L2B0*	- Level 1 Accept Buffer Address 0
	bit 5	CDF_L2B1*	- Level 1 Accept Buffer Address 1
	bit 6	CDF_GLIVE*	- Level 1 Accept corresponds to live Beam Crossing
	bit 7	RSVD_L1W1*	- TSI reserved L1 word bit(7)
	bit 8	RSVD_L1W2*	- TSI reserved L1 word bit(8)
L2 Word	bit 2	CDF_L2DB0*	- Level 2 Accept Decision Buffer Address 0
	bit 3	CDF_L2DB1*	- Level 2 Accept Decision Buffer Address 1
	bit 4	CDF_L2A_EN*	- Level 2 Accept Enable signal
	bit (8:5)	CDF_EVID(3:0)*	- Event Identifier(0)
Calib Word	bit (8:2)	CDF_CALIB(6:0)*	- Calibration bits which may be sent by TSI; these currently have no definition
Control Word	bit 2	CDF_STOP*	- Set Halt Condition
	bit 3	CDF_RECOVER*	- Reset FIFOs/pipelines
	bit 4	CDF_TEST*	- Diagnostic bit which will cause TRACER to capture TAXI link (TSI <-> TRACER) data
	bit 5	CDF_RUN*	- Clear Halt Condition
	bit (8:6)	CDF_RL(2:0)*	- Readout List Identifier

(the following signals are generated by TRACER using above TSI info)

CDF_HALT*	- Halt filling L1 FIFO/pipelines - the HALT condition is set by CDF_STOP* and cleared by CDF_RUN*
CDF_CALIBEN*	- Calibration Enable - this is set whenever a TSI Calibration Word is received
CDF_L2A*	- Level 2 Accept - this is set whenever a TSI L2 Word is recieved and CDF_L2A_EN* is true

All of the above signals are gates to the rising edge of the CDF_CLK signal. They are guaranteed to have at least a 10 ns setup and hold time with respect to the clock edge.

3.2 The Start Scan and Done Registers

The TRACER will also provide Start Scan and Done Registers which will be used in communications protocol with the TSI. When the TSI indicates it is time to read out an event (Start Event Scan), a bit will be set in the TRACER's Start Scan Register.

The VMEbus Readout Controller (VRC) can poll this register and begin readout when it sees the Start Scan bit set, or an interrupt mode may be enabled which causes the TRACER to initiate an Interrupt cycle upon the reception of Start Scan. When the VRC has finished its readout cycle, it will write to the Done Register and set the Done bit.

Start Scan Register

Description: data for this register comes from the TSI "Level 2" word.

The Start Scan bit is set when a L2 Accept is indicated, and cleared when the DONE bit is set in the Done Register.

Bit 16 reflects the state of the open-collector backplane signal CDF_TDC_DONE

Bit	Function
0-15	Undefined
16	CDF_TDC_DONE
19-17	Undefined
20	Readout List 0
21	Readout List 1
22	Readout List 3
23	Undefined
24	Start Scan
25	L2 Decision Buffer Address 0
26	L2 Decision Buffer Address 1
27	Undefined
28	Event ID 0
29	Event ID 1
30	Event ID 2
31	Event ID 3

Done Register

Description: The Done bit can be set to a logic high by the VRC, over VMEbus, when readout is complete. The VMEbus path does not allow the bit to be set to a logic low. The Done bit will also be set to a logic high by the "recover" command in the event of a Halt-Recover-Run sequence.

The Done bit will be set to a logic low with the issuance of a new Start Event Scan command by the TSI.

The End of Block maker may be written over VMEbus. When it is set, it will cause an EOB to be appended to the data in the Event FIFO. It is a self-clearing bit and cannot be read back. The EOB marker is an optional feature - its usage it not necessarily required.

Done and EOB have been placed in the same register in order to reduce the number of VMEbus cycles which the VRC must do at the end of a readout cycle. Typical usage would have the VRC set both Done and EOB at the end of a readout cycle. However, if an "early" done is sent to the TSI, the EOB marker could be sent later, after the data has been transferred to the Event FIFO.

Bit	Function
23-0	Undefined
24	Done (VMEbus can set DONE when bit 24 equals "1", no reset capability over VMEbus)
30-25	Undefined
31	End of Block (EOB) (write only - self clearing bit)

3.3 DONE, ERROR and BUSY Signals

TSI <-> TRACER protocol also relies on a parallel copper link which will allow the TRACER to drive the signals DONE, ERROR and BUSY to the TSI.

The DONE signal is simply the buffered Done bit in the Done Register. The Done bit is set through a write over VMEbus, and cleared upon the reception of a Start Scan. The Done bit will also be set by the "recover" command in the event of a Halt-Recover-Run sequence.

The ERROR signal will be asserted whenever some module in the CDF Crate is asserting CDF_ERROR~ on the open-collector backplane signal. The assertion of ERROR is meant to occur only in the case of a catastrophic error. Additionally, it is possible to mask ERROR with a bit in the control register.

The BUSY signal is asserted whenever the buffer space in the VRB (CDF's VMEbus Readout Board) becomes full. A direct optical link between the VRB and the TRACER, informs the TRACER when the higher level DAQ readout has become clogged. This bit will not be cleared with a Halt-Recover-Run sequence. In order to clear BUSY, the problem with the clogged VRB readout buffers must be fixed.

An eight pin Shielded Modular Data Link Connectors (see Appendix C) will be provided on the TRACER's Front Panel, with the following pinout:

Pin	**Signal**
1	DONE
2	DONE~
3	ERROR
4	ERROR~
5	BUSY
6	BUSY~
7	NC
8	NC

3.4 TEST Mode

It is possible for the TSI to turn on input to the TSI Diagnostic FIFO by sending the "TEST" bit in the TSI Control Word. When "TEST" is sent, the FIFO is flushed and the next 8K data words received from the TSI to be clocked into a FIFO. In its this operating mode, once the FIFO is full, no further data recording will be done. In order to repeat the test, the original "TEST" state must be cleared by toggling the "reset tsi test" bit in the Control Register.

A second diagnostic mode possible - it will, however, be overriden by any "TEST" message written from the TSI. In the second mode, it is possible to save the last ~8K of TSI commands by setting the "tsi_save_mode" bit of the Control Register. When this bit is set the TSI Diagnostic FIFO will be filled by incoming TSI commands. As the FIFO limit is approached, automatic readout is begun to clear space for new commands. If at any time a CDF_ERROR* condition occurs, the state of the FIFO will be frozen. Hopefully, this will aid in determining what was going on in the crate at the time of the error.

4.0 Data Transmission

The TRACER has an optical data link to the VRB. This link uses the TAXIchip (AM7968-175JC) protocol and AMP optical driver (AMP 269049-1). It operates at two times the CDF_CLK.

An 8K by 32 bit Event FIFO feeds this data link. It is possible to fill this Event FIFO in two ways. One way is to simply do a VMEbus write into the FIFO. If the VRC is used to do zero suppression and data formatting, this method would be used. The VRC would first read in raw event data, do the formatting and then write the formatted data to the Event FIFO.

A second method for getting event data to the VRB would involve using the TRACER's Spy capability. The TRACER will have the capability to spy on the data as the VMEbus Readout Controller (VRC) reads it out. During event readout, the TRACER has the ability to clock data into the Event FIFO. The data which gets clocked into the event FIFO includes any VMEbus reads of data in the L2 Buffer Space (specified in CDF/DOC/TRIGGER/CDFR/2288), and any write to the Done Register which sets the EOB marker. This Spy mode would be used only if there is no need for the VRC to do data formatting.

A sequencer on the TRACER would detect when data is present in the FIFO, serialize the data through the use of a TAXIchip, and transmit it upstairs to the Readout Memory (VRB) module via an optical link. The data can be transmitted to the VRB at a rate of up to one byte every 66 ns (twice the CDF clock). A Taxi Sync signal is sent up at least every 5 bytes; thus, a data rate of 4 Bytes/(5 x66ns), or 12.1 MB/s is achievable out of the crate.

It is possible to append set an End of Block (EOB) marker on the transmitted data stream. This is done by writing to the EOB bit in the Done register. Whenever a logic high is written to this bit, the equivalent of a 33 bit word will be clocked into the Event FIFO. The MSB will be set high and will indicate the EOB. This EOB bit will be passed to the TaxiChip as the 9th data bit, which can then be decoded as EOB by the VRB.

5.0 Event Data Header Information

The TRACER will have registers to hold header information which should be applied to all event fragments which are transmitted to the VRB. The following header information should mark all events:

Word Count	(32 bits)	;downloaded from system or calculated by VRC
Partition ID	(3 bits)	;downloaded from system
Crate ID	(8 bits)	;downloaded from system
Event ID	(4 bits)	;obtained from TSI
L2 Buffer Address	(2 bits)	;obtained from TSI
Readout List #	(3 bits)	;obtained from TSI

The Word Count will be used by the VRB as a way of identifying Event fragments as they pass through it.

This header information can get into the Event FIFO in two ways. If the VRC is doing event formatting and transmitting the formatted event to the TRACER's Event FIFO, the VRC should apply the header to the formatted data. In this case, the VRC would need to be told the Partition ID and Crate ID at start-up. The rest of the header information would be available to the VRC through (1) reading the Start Scan register which is being polled in order to know when to initiate Event readout or (2) reading the Start Scan register upon receiving a Start Scan interrupt if interrupt mode is enabled.

In the case where the TRACER is in spy mode, and directly stores the raw event data into its Event FIFO, it is necessary to include the TRACER word count and header Registers in the beginning of the readout list. As they are read out, they will be written into the Event FIFO like all other Event data.

Word Count Register

Description: this register contains the number of 32 bit words (inclusive) which make up the event fragment. It must be downloaded if "Spy" mode is used.

Bit	Function
31-0	Word Count(31:0)

Event Header Register

Description: this register contains the minimum amount of information which must be applied as a header to all event fragments read out into L3.

Bit	Function
7-0	Crate ID(7:0)
10-8	Partition ID(2:0)
15-11	Undefined
19-16	Event ID(3:0)
21-20	L2 Decision Buffer Address(1:0)
22-23	Undefined
24-26	Scan List #
27-31	Undefined

It may also be desirable to mark the end of an event. To do this we could repeat the Word Count and Event Header information. Two possible pattern words of A's and 5's will also be available as tags to be added to these words to aid in the descrambling of event blocks.

6.0 Reset Function

It is necessary to provide a remote reset capability for front end VMEbus crates. The main purpose of the reset will be to reboot a CPU which has hung. This will be done through the use of a dedicated reset line which will come in through a front panel connector and be driven by the CDF Reset Crate.

The reset signal will be driven and received as an RS-422 signal. When the reset line is pulsed low it will drive the SYSRESET* line low on the VMEbus backplane. This will cause all boards to do a reset.

7.0 TRACER TDC Calibration Features

Standard CDF Calibration Signals

The standard method of performing a calibration with the CDF system involves having the Trigger System Interface (TSI) send down a Calibration word which causes the CDF signal CDF_CALIBEN* to be asserted on the backplane. At some number of programmable (for example, 42) CDF clock cycles later, a L1 Accept will be issued. The data is then available in the L2 Decision Buffers for readout. A Start Event Scan message would be generated by the TSI to cause the event to be readout into the event stream.

Additional Features Required for TDC Calibration

Additional calibration signals are required for the TDCs. These signals consist of three backplane signals called CDF_TDC_CAL(2:0)*, as well as a precision differential PECL signal called CDF_TDC_CALIB*. All of these signals are active low.

CDF_TDC_CAL(2:0)* will be derived from the TSI Calibration word with the additional programmability that the pulses will not fire unless they have been enabled, and then not until two delay requirements are fulfilled. The TDC calibration pulses are enabled via the TDC Calibration Pulses Enable Register.

TDC Calibration Pulses Enable (r/w)

Bit	Function
28-0	Undefined
29	Enable CDF_TDC_CAL0*
30	Enable CDF_TDC_CAL1*
31	Enable CDF_TDC_CAL2*

The first programmable delay required is the number of CDF clock cycles which should occur prior to firing. This delay will range from 0-255. This delay will be set via a register on the Tracer and each of the four TDC calibration pulses will be independently programmable. Course delay values are set in the TDC Calibration Course Delay Register.

TDC Calibration Course Delay Register (r/w)

Bit	Function
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

The second delay requirement will be a finer delay which will be set off the edge of CDF clock. This delay will be provided through an Analog Devices AD9501. The AD9501 can be set for a full scale range of 132ns with 255 delay steps for an adjustment step of ~.5 ns. Fine delay values are set in the TDC Calibration Fine Delay Register.

TDC Calibration Fine Delay Register (r/w)

Bit	Function
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

There is an inherent propagation delay of 25-30 ns through the AD9501 - this will not be taken out, so it be necessary to have the ability to have L1 Accepts issued on up to two consecutive events to cover the full 132ns CDF cycle.

A final value of some concern is the pulse widths of CDF_TDC_CAL(2:0)*. The pulse width will be controlled via a programmable delay. The minimum pulse width will be 20ns and can grow in 5ns intervals up to 55ns. The pulse width will be controlled via the TDC Calibration Pulse Width Register. The pulse width will be 20ns + (5ns x value of Width Count).

TDC Calibration Pulse Width Register (r/w)

Bit	Function
21-0	Undefined
22-20	Width Count (2:0) for CDF_TDC_CAL0*
23	Undefined
26-24	Width Count (2:0) for CDF_TDC_CAL1*
24	Undefined
30-28	Width Count (2:0) for CDF_TDC_CAL2*
31	Undefined

Again, in normal operating mode, in order for any data to be included in the readout stream, the TSI must know to send a L1 Accept and a Start Event Scan. Therefore, any delays programmed into the first delay requirement would need to be communicated back to the TSI. Also, note that the TSI cannot change this number on the fly and it may/will conflict with other systems. This should not be a problem in a stand-alone TDC calibration run.

Front Panel Input

CDF_TDC_CALIB* can be driven through a twinax Front Panel bulkhead which expects differential PECL levels. It will be re-driven as a differential PECL signal to the backplane. Driver and Receiver chips will make use of ECLPS logic.

8.0 Local Test Stand Calibration

8.1 Introduction to test stand calibration

A need to perform in-crate calibration of the QIEs without control from the TSI exists. The timing and "quiet time" requirements make the calibrations difficult to fit into run-time protocol between the TSI and the TRACER. Calibration constants are most easily determined within the crate, using the local computing power of the VRC.

The VRC will determine the gains and offsets for each of the four QIE capacitors over ten QIE scales. This results in 80 constants to be determined. These constants will then be used by the VRC to calculate values for a lookup table which will linearize the raw QIE output.

Similiarly, it will be possible to have the TRACER logic trigger the special TDC calibration signals which were described in the previous section.

8.2 The Calibration flow

8.2.1 Calorimety Test Stand Flow

Calibration of the calorimetry is accomplished in the following manner:

- Set up the calibration reference by writing to a register on the ADMEM board.
- Set ADMEM look-up tables to pass-through mode (raw data will not be changed).
- Wait.
- Issue a Calibration command by writing to the TRACER Calibration Register.
- Tracer will wait programmed time, determined by the TRACER Start Delay Register.
- Tracer will issue Halt - Reset - Run sequence.
- Admem boards will begin filling pipeline with Beam Zero Crossing.
- Tracer will wait programmed time, determined by the TRACER Calibration Enable Delay Register.
- Tracer will issue Calibration Enable.
- Tracer will issue four successive L1 Accepts at a programmed number of crossings (set in the Calibration Delay Register) after calibration enable. The successive L1 Accepts will fill buffers 0, 1, 2 and 3 in that order.

- Tracer will will wait a programmed delay, determined by the TRACER Halt Delay Register.

- Tracer will issue Halt (if halt mode enabled).

- Tracer will set a bit in a register to indicate process is done.

  VRC will see calibration is complete, and will read out L2 buffer.

8.2.2 TDC Test Stand Flow

Calibration of the TDCs is accomplished in the following manner:

- Set up the TDC Calibration Control Registers described in the previous section.

- Issue a Calibration command by writing to the TRACER Calibration Register.

- Tracer will wait programmed time, determined by the TRACER Start Delay Register.

- Tracer will issue Halt - Recover - Run sequence.

- TDC boards will begin filling pipeline with Beam Zero Crossing.

- Tracer will wait programmed time, determined by the TRACER Calibration Enable Delay Register.

- Tracer will issue Calibration Enable.

- The Calibration Enable will trigger the TDC Calibration circuitry.

- TDC Calibration signals CDF_TDC_CAL(2:0)* will fire according to the constraints set in the TDC Calibration Pulses Enable Register, the TDC Calibration Course Delay Register and the TDC Calibration Fine Delay Register.

- Tracer will issue four successive L1 Accepts at a programmed number of crossings (set in the Calibration Delay Register) after calibration enable. The successive L1 Accepts will fill buffers 0, 1, 2 and 3 in that order.

- Tracer will will wait a programmed delay, determined by the TRACER Halt Delay Register.

- Tracer will issue Halt (if halt mode enabled).

- Tracer will set a bit in a register to indicate process is done.

  VRC will see calibration is complete, and will read out L2 buffer.

8.3 Setting up the Tracer

The Tracer must provide control over the following CDF backplane signals in order for the calibartion to take place:

CDF_L1A~	(L1 Accept)
CDF_L1R~	(L1 Reject)
CDF_L2B0~	(L2 Buffer Address 0)
CDF_L2B1~	(L2 Buffer Address 1)
CDF_HALT~	(Halt L1 Buffer fill)
CDF_RESET~	(Reset all pipeline pointers)
CDF_CALIB0~	(Calibration enable 0)
CDF_CALIB1~	(Calibration enable 1)
CDF_CALIB2~	(Calibration enable 2)
CDF_CALIB3~	(Calibration enable 3)
CDF_CALIB4~	(Calibration enable 4)
CDF_CALIB5~	(Calibration enable 5)
CDF_CALIB6~	(Calibration enable 6)
CDF_CALEN~	(Calibration enable)
CDF_TDC_CAL(2:0)~	(TDC Calibration signals)

The timing of when these signals take place is critical to the calibration. The Tracer will provide a high degree of control over when these signals are asserted.

8.4 Tracer Calibration Registers

Calibration Register

Description: writing a one to the Local Calibration Enable bit, will atomatically begin a teststand type calibration (assuming local teststand calibration mode has been previously enabled in general CSR register).

Bit	Function	
15-0	Undefined	
16	Local Calibration Enable	
23-17	Undefined	
24	Calibrate Enable 0~	
25	Calibrate Enable 1~	
26	Calibrate Enable 2~	
27	Calibrate Enable 3~	
28	Calibrate Enable 4~	
29	Calibrate Enable 5~	
30	Calibrate Enable 6~	
31	Enable Halt Mode	; this bit will cause the Tracer to issue a halt, a pre-programmed number of clock cycles after a L1 Accept

Start Delay Register

Description: this register will contain the value reflecting the number of 132ns clock cycles to wait before asserting the Halt - Reset - Run sequence following a write to the Calibration Register.

Bit	Function
15-0	Undefined
31-16	(MSB:LSB) count of 132ns waiting periods

Calibration Delay Register

Description: this register contains the value, bits (15:0), reflecting the number of 132ns clock cycles to wait before asserting the Calibration Enable gate as well as the number of 132ns clock cycles, bits (31:16), to wait follwing the issuance of L1 Accept.

For a calorimetry local test stand run, the value of bits (31:16) would be set to 42, the pipeline depth. For a TDC calibration type, bits (31:16)

Bit	Function
15-0	Calen* Delay Value (MSB:LSB) count of 132ns waiting periods, following the Halt-Recover-Run sequence, before issuing Calibration Enable
31-16	L1A* Delay Value (MSB:LSB) count of 132ns waiting periods, after issuing Calibration Enable, before asserting L1A

Halt Delay Register

Description: this register will contain a value reflecting the number of 132ns clock cycles to wait following the issuance of a L1 Accept before asserting a CDF_HALT~. CDF_HALT~ will be asserted only if the Enable Halt Mode bit is set in the Calibration Register.

Bit	Function
15-0	Undefined
31-16	(MSB:LSB) count of 132ns waiting periods

Calibration Done Register

Description: this is a read-only register which will contain a bit to indicate that the teststand calibration is done. It will be cleared with a write to the Calibration register and set at the end of the teststand calibration cycle.

Bit	Function
30-0	Undefined
31	Teststand Calibration Done

9.0 TRACER Interrupt Mode

The TRACER has an interrupt feature which may be used to indicate that a Start Event Scan message has been received. The enabling of this interrupt mode is controlled via the Control Register. The interrupt feature is provided as an alternative method to the polling of the Start Event Scan Register.

The Interrupt Level is settable via switches on board, and the set level is readable through the Control Register.

A separate Interrupt Return Vector Register will allow the user to set the interrupt return vector.

10.0 TRACER Transition Module Port

A sixteen bit read/write port to a possible transition module has been included on the TRACER. The port is written to and read from via the Transition Port Read/Write Register on the TRACER. A four bit address to the port is set via the Transition Port Address Register. The port also receives positive logic read and write control signals.

The user defined pins of the P0 connector are used to implement the port.

PIN #	Row a	**Row b**	**Row c**	**Row d**	Row e
1	+5V	+5V	+5V	+5V	+5V
2	Ret_WX	Reserved	+5V	TBUS 1+	TBUS 1-
3	Ret_WX	Reserved	Reserved	TBUS 2+	TBUS 2-
4	Vw	Reserved	tran_port_a(0)	tran_port_d(0)	tran_port_d(1)
5	Vw	Reserved	tran_port_a(1)	tran_port_d(2)	tran_port_d(3)
6	Ret_WX	Reserved	tran_port_a(2)	tran_port_d(4)	tran_port_d(5)
7	AREF_WX	Reserved	tran_port_a(3)	tran_port_d(6)	tran_port_d(7)
8	Ret_WX	Reserved	tran_port_read	tran_port_d(8)	tran_port_d(9)
9	Vx	Reserved	tran_port_write	tran_port_d(10)	tran_port_d(11)
10	Vx	Reserved	USER I/O	tran_port_d(12)	tran_port_d(13)
11	Vy	Reserved	USER I/O	tran_port_d(14)	tran_port_d(15)
12	Vy	Reserved	USER I/O	USER I/O	USER I/O
13	Ret_YZ	Reserved	USER I/O	USER I/O	USER I/O
14	AREF_YZ	Reserved	USER I/O	USER I/O	USER I/O
15	Ret_YZ	Reserved	USER I/O	USER I/O	USER I/O
16	Vz	Reserved	USER I/O	USER I/O	USER I/O
17	Vz	Reserved	Reserved	TBUS 3+	TBUS 3-
18	Ret_YZ	Reserved	Reserved	TBUS 4+	TBUS 4-
19	Ret_YZ	Reserved	Reserved	TBUS OC1	TBUS OC2

11.0 TRACER Front Panel

The TRACER Front Panel will contain the following LED indicators:

+5V	**;LED (red) on when module is powered**
Module Select	**;LED (green) on during VMEbus access**
CDF_Clock	**;LED (yellow) on when CDF_Clock is being received**
TSI_DONE	**;LED (green) on when DONE is being returned to TSI**
TSI_ERROR	**;LED (red) on when ERROR is being returned to TSI**
TSI_BUSY	**;LED (yellow) on when BUSY is being returned to TSI**

The TRACER Front Panel will also hold

8-pin Shielded Data Link connector for TSI return signals
8-pin Shielded Data Link connector to receive Master Clock Signals
An optical cable receiver for TSI TAXI-protocol data
An optical cable driver for data link to VRB
An optical cable receiver for the Busy signal from the VRB
An 8-pin module jack to receive a reset signal from the CDF RESET Crate
Two 34 pin headers to spy on the special CDF backplane signals (see next page)

TDC calibration Twinax Bulkhead; LVDS input

Pinout of the Front Panel Headers to allow spying on J2, rows A and C. These will all be buffered so that a bent front panel pin will not effect the operation of the board or the backplane.

PIN #	Signal Name	PIN #	Signal Name
1	**GND**	**2**	**GND**
3	J2-A1	**4**	CDF_TDC_CAL0*
5	J2-A2	**6**	CDF_TDC_CAL1*
7	J2-A3	**8**	CDF_TDC_CAL2*
9	J2-A4	**10**	CDF_TDC_CALIB
11	J2-A5	**12**	CDF_TDC_CALIB
13	**CDF_CLK**	**14**	J2-C6
15	**CDF_CLK**	**16**	J2-C7
17	J2-A8	**18**	J2-C8
19	**CDF_BC***	**20**	J2-C9
21	**CDF_B0***	**22**	J2-C10
23	J2-A11	**24**	J2-C11
25	**CDF_L1A***	**26**	**CDF_GLIVE***
27	**CDF_L1R***	**28**	**RSVD_L1W1***
29	**CDF_L2B0***	**30**	**RSVD_L1W2***
31	**CDF_L2B1***	**32**	**CDF_STOP***
33	**CDF_HALT***	**34**	**CDF_TEST***

PIN #	Signal Name	PIN #	Signal Name
1	**GND**	**2**	**GND**
3	J2-A17	**4**	**CDF_RUN***
5	**CDF_RECOVER***	**6**	**CDF_RL0***
7	J2-A19	**8**	**CDF_RL1***
9	**CDF_ABORT***	**10**	**CDF_RL2***
11	**CDF_CALIB0***	**12**	**CDF_CALIB3***
13	J2-A22	**14**	**CDF_CALIB4***
15	**CDF_CALIB1***	**16**	**CDF_CALIB5***
17	**CDF_CALIB2***	**18**	**CDF_CALIB6***
19	J2-A25	**20**	**CDF_CALEN*CDF_CALEN***
21	**CDF_ERROR***	**22**	J2-C26
23	**CDF_L2A***	**24**	J2-C27
25	**CDF_L2BD0***	**26**	**CDF_L2A_EN***
27	J2-A29	**28**	**CDF_EVID0***
29	**CDF_L2BD1***	**30**	**CDF_EVID1***
31	**CDF_RSVD0***	**32**	**CDF_EVID2***
33	**CDF_RSVD1***	**34**	**CDF_EVID3***

12.0 VMEbus Slave Interface

The TRACER will implement a modified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may be either single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. All boards will be assigned a unique geographical address through use of backplane pins on the CDF Custom J2 backplane. The TRACER will respond to all address spaces. Therefore, TRACER modules will respond to the following address modifier codes: 09, and 0B.

Memory Map

YY00 0000 Diagnostic Register (32 bit Read/Write) (r/w)

YY00 0004 Control Register

Bit **Function**

3-0 Undefined

6-4 Interrupt Level (2:0) (r)
allows readback of the Jumper settings of the interrupt level

7 Error (r)
reflects the state of CDF_ERROR on the backplane*

8 VRB Busy (r)
reflects the state of VRB_Busy signal coming from the VRB

9 TSI Diagnostic FIFO PAFE~ (r)

10 TSI Diagnostic FIFO E/F~ (r)

11 TSI Diagnostic FIFO HF~ (r)

HF*	E/F*	PAFE*	State
1	0	0	Empty
1	1	0	Almost Empty
1	1	1	Less Than Half Full
0	1	1	Greater Than Half Full
0	1	0	Almost Full
0	0	0	Full

12 TSI Taxi Error (r)
TaxiChip violation has been detected

13 Event FIFO PAFE~ (r)

14 Event FIFO E/F~ (r)

15 Event FIFO HF~ (r)

20-16 Undefined

21 Enable TSI Diagnostic FIFO Save Mode (r/w)
when set, TSI Diagnostic FIFO will save last 8K TSI commands

22 Reset TSI Diagnostic FIFO “TEST” mode (r/w)
toggle hi-lo to reset “TEST” message from TSI

23 Reset TSI Diagnostic FIFO (r/w)
toggle hi-lo to reset the TSI Diagnostic FIFO
24 Reset TSI Taxi Error (r/w)
toggle hi-lo to clear TSI Taxi violation error state, and reset the TSI TAXI Violation Counter Register
25 Enable CDF Trigger Signals to backplane (r/w)
when set, will cause CDF Trigger signals to be driven to the backplane
26 Select CDF Trigger Signal source (r/w)
0 - TSI Interface
1 - Local Calibration Sequencer
27 Interrupt Mode Enable (r/w)
when set, enables interrupts when Start Event Scan received from TSI
28 Mask CDF_ERROR (r/w)
when set, will mask out any errors being sent to the TSI
29 Event Data Taxi Enable (r/w)
when set, the onboard sequencer will begin reading out the Event FIFO and streaming the data to the VRB
30 Spy Mode Enable (r/w)
when set, L2 buffer space data will be captured from the backplane and put into the Event FIFO
31 Software Reset (r/w)

YY00 0008 Start Scan Register (r)

Bit	**Function**
0-15	Undefined
16	CDF_TDC_DONE
19-17	Undefined
20	Readout List 0
21	Readout List 1
22	Readout List 3
23	Undefined
24	Start Scan
25	L2 Decision Buffer Address 0
26	L2 Decision Buffer Address 1
27	Undefined
28	Event ID 0
29	Event ID 1
30	Event ID 2
31	Event ID 3

YY00 000C Done Register (r/w)

Bit	**Function**
23-0	Undefined
24	Done (VMEbus can set DONE when bit 24 equals “1”, no reset capability over VMEbus)
30-25	Undefined
31	End of Block (EOB) (write only - self clearing bit)

YY00 0010 Calibration Register (r/w)

Bit	**Function**	
15-0	Undefined	
16	Local Calibration Enable	
23-17	Undefined	
24	Calibrate Enable 0~	
25	Calibrate Enable 1~	
26	Calibrate Enable 2~	
27	Calibrate Enable 3~	
28	Calibrate Enable 4~	
29	Calibrate Enable 5~	
30	Calibrate Enable 6~	
31	Enable Halt Mode	; this bit will cause the Tracer to issue a halt, a pre-programmed number of clock cycles after a L1 Accept

YY00 0014 Start Delay Register (r/w)

Bit	**Function**
15-0	Undefined
31-16	(MSB:LSB) count of 132ns waiting periods

YY00 0018 Calibration Delay Register (r/w)

Bit	**Function**
15-0	(MSB:LSB) count of 132ns waiting periods, following the Halt-Recover-Run sequence, before issuing Calibration Enable
31-16	(MSB:LSB) count of 132ns waiting periods, after issuing Calibration Enable, before asserting L1A

YY00 001C Halt Delay Register (r/w)

Bit	**Function**
23-0	Undefined
31-24	(MSB:LSB) count of 132ns waiting periods

YY00 0020 Calibration Done Register (r)
(cleared with any write to the Calibration Register)

Bit	Function
30-0	Undefined
31	Teststand Calibration Done

YY00 0024 Interrupt Return Vector Register (32 bit Read/Write) (r/w)

YY00 0028 TDC Calibration Pulses Enable (r/w)

Bit	Function
28-0	Undefined
29	Enable CDF_TDC_CAL0*
30	Enable CDF_TDC_CAL1*
31	Enable CDF_TDC_CAL2*

YY00 002C TDC Calibration Course Delay Register(r/w)

Bit	Function
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

YY00 0030 TDC Calibration Fine Delay Register(r/w)

Bit	Function
7-0	Undefined
15-8	Delay for CDF_TDC_CAL0*
23-16	Delay for CDF_TDC_CAL1*
31-24	Delay for CDF_TDC_CAL2*

YY00 0034 TDC Calibration Pulse Width Register(r/w)

Bit	Function
21-0	Undefined
22-20	Width Count (2:0) for CDF_TDC_CAL0*
23	Undefined
26-24	Width Count (2:0) for CDF_TDC_CAL1*
24	Undefined
30-28	Width Count (2:0) for CDF_TDC_CAL2*
31	Undefined

YY00 0038 Transition Port Read/Write Register (r/w)

Bit	Function
15-0	Undefined
31-16	Data(15:0)

YY00 003C Transition Port Address Register (r/w)

Bit	**Function**
27-0	Undefined
31-28	Address(3:0)

YY10 0000 - YY10 007C ID PROM (upper 8 bits) (r)

YY40 XXXX TSI_Diagnostic FIFO (r)
(holds first 8K data words sent down TSI optic link after the receipt of the TEST signal)

YY50 XXXX Event Data FIFO (r/w)

YY80 0000 Word Count Register (r/w)

Bit	**Function**
31-0	Count of 32 bit Words in Event Record

YY80 0004 Event Header Register

Bit	**Function**
7-0	Crate ID(7:0) (r/w)
10-8	Partition ID(2:0) (r/w)
11-15	Undefined
19-16	Event ID(3:0) (r)
21-20	L2 Buffer Address(1:0) (r)
23-22	Undefined
26-24	Scan List #(2:0) (r)
27-31	Undefined

YY80 0008 TSI TAXI Violation Counter Register

YY80 000C A's Pattern Register (r)
This word will contain (hex)AAAAAAAA

YY80 0010 5's Pattern Register (r)
This word will contain (hex)55555555

APPENDIX A

Bill Of Materials

```
01/27/97 13:30:26             Electronics Design System                 Page: 0001
                                  Bill of Materials
       <<<From Job:  E:\EES_JOBS\TRACER_V6\tracer_version6\vbdc\tracer.prj>>>

                             Fermi National Accelerator
                     Particle Physics Division/CDF Upgrade Project
```

Item	QTY	vendor part number	Description	Cost
1	3	AD9501JP	Dig Prog Delay Gen,	20.00
2	2	AMP 1-520459-3	AMP Modular Jack Con	2.25
3	1	AMP 226968-1 DIGI A1126-ND	Twinax Bulkhead	24.58
4	1	AMP 269050-1	AMP Optronic Data Li	76.47
5	1	AMP 352009-1 PLUS SHIELDS .	AMP 5x19 Z-PACK 2mm	25.00
6	1	AMP269049-1	200 Mb/s 1300 nm opt	20.00
7	1	AM27S19SAPC	32x8 PROM	1.25
8	1	AM7968-175JC	Taxi xmtr	20.00
9	1	AM7969-175JC	TAXI RCVR	25.00
10	1	C&K P8121 1160-1890	Mom. Push button Pan	2.48
11	1	CY7B991-7JC	ROBOCLOCK	21.85
12	4	CY7C470-15JC	Cypress 8K x 9 FIFO	22.00
13	1	CY7C470-15PC	Cypress 8K x 9 FIFO	22.00
14	3	CY74FCT16500TTSSOP	18-bit Registered Tr	5.78
15	5	CY74FCT162244TTSSOP	16-Bit Buffers/Line	3.95
16	1	DS26C32ATN RS-422 recvr Nation	Diff Line RCVR	3.50
17	1	DS90C031 National	Differential Line Dr	2.23
18	2	DS90C032 National	Differential Line Re	2.23
19	1	ERIE 8121-050-651-103M 1415-30	Bypass Cap .01UF	0.07
20	3	ERIE 8131-100-651-104M 1415-31	Bypass Cap .1UF	0.05
21	1	ERIE 8131-100-651-153M 1415-30	Bypass Cap .015UF	0.07
22	5	ERJ-6ENF47.5 Digi P47.5CBK-ND	1/10W 1% 47.5 ohm	0.061
23	3	ERJ-8ENF1.87K Digi P1.87KFBK-N	1/8W 1% 1.0K ohm	0.0542
24	5	ERJ-8ENF100 Digi P100FBK-ND	1/8W 1% 100 ohm	0.0542
25	1	ERJ-8ENF115 Digi P115FBK-ND	1/8W 1% 115 ohm	0.0542
26	2	ERJ-8ENF158 Digi P158FBK-ND	1/8W 1% 158 ohm	0.0542
27	2	ERJ-8ENF267 Digi P267FBK-ND	1/8W 1% 267 ohm	0.0542
28	3	HARTING-male	VME64 Card Connector	25.00
29	1	HIROSE TM5RJ1-66 DIG H9083-ND	Modular Jack 6pos 6c	2.30
30	1	HP HFBR-2412	Fiber Optic RCVR	18.15
31	4	HP HLMP-1301 1445-0475	Red LED	0.24
32	1	HP HLMP-1401 1445-0495	Yellow LED	0.24
33	1	IDT 74FCT244DTP	8 bit Tri-state buff	3.40
34	21	KEMET T340B106K015AS	10UF 15V Bullet	.80
35	3	KEMET T354H336K016AS	33UF 16V RADIAL Dip	.85
36	2	LITTLEFUSE 251010 Newark 20F60	10 AMP PCB Fuse	0.74
37	1	MACH 110-12JC	AMD PLD 44 Pin PLCC	7.00
38	1	MC10H350	PECL Receiver	10.00
39	2	MOTOROLA 1N5908	Transient Suppressor	1.24
40	3	PALCE22V10H-7PC	Programmable Logic D	5.00
41	5	PAN ECS-H1CC106R DIG PCT3106	SMT CAP 10.0UF	0.9765
42	2	PAN ECS-H1CY105R DIG PCT3105	SMT CAP 1.0UF	0.3955
43	3	PAN ECU-V1H100DCM DIG PCC100CC	SMT CAP 10PF	0.168
44	8	PAN ECU-V1H103KBG DIG PCC103BN	SMT CAP 0.01UF	0.168
45	2	PAN ECU-V1H103KBM DIG PCC103BC	SMT CAP 0.01UF	0.168
46	148	PAN ECU-V1H104KBW DIG PCC104B	SMT CAP 0.1UF	0.5914
47	4	PAN ECU-V1H270JCG DIG PCC270CG	SMT CAP 27pF	0.133
48	1	PAN ECU-V1H270JCM DIG PCC270CC	SMT CAP 27pF	0.133
49	20	PN32	test point	
50	5	RC05-270 1487-0290	270 ohm 1/8W 5%	0.19
51	1	RC05-820K 1487-0497	1/8W 820Kohm 5%	0.18
52	4	RC05-1000 1487-0325	1000 ohm	0.18
53	1	RC07-1.5M 1487-1125	1/4W, 5PCT, THRU	0.14
54	1	RC07-5.6 Digi 5.6QBK-ND	1/4W, 5PCT, THRU	0.06
55	2	RC07-4700 1487-0825	1/4W, 5PCT, THRU	0.08
56	1	RN55C-13K	1/8W 1PCT Thru	0.04
57	3	RN55C-27K	1/8W 1PCT Thru	0.04
58	2	RN55C-84.5	1/8W 1PCT Thru 249 O	.04
59	1	RN55C-100K	1/8W 1PCT Thru	0.04
60	2	RN55C-169	1/8W 1PCT Thru 169 O	.04
61	3	RN55C-249 1487-4365	1/8W 1PCT Thru 249 O	.04
62	14	SN74ABTE16245SSOP	16 Bit Incident Tran	5.60
63	1	SN74ABTE16246SSOP	11 Bit Incident Tran	7.50
64	6	Samtec TSW-12-07-L-D 2pin sip	2 pin jumper - mates	0.16
65	8	Spare-IC 24DIP3	Spare 24 pin DIP	0.00
66	47	TEST_PIN	.025 x .025 square p	.01
67	1	TIBPAL16L8-5C	Programmable Logic D	5.00
68	1	XC3130A-1PQ100C	Xilinx XC3130A Logic	35.00
69	1	XC4013E-3PQ240C	Xilinx FPGA	250.00
70	2	XC17256-PD8C	XILINX PROM	13.00
71	2	mc10h351l	Quad TTL to PECL tra	10.00

72	1	1N5817	Scottky Diode	.80
73	1	3 pin jump 3SIP60 TSW-12-07-L-	3 pin jumper	0.30
74	2	3m3431-5302 1435-7110	3M 34 pin 100X100 so	1.66
75	1	10x-2-102	10 pin 1K SIP, pin 1	1.50
76	1	74F04N	hex inverter	0.53
77	1	74F38N	Open collector nand	0.53
78	1	74LS14N 1455-8014	schmitt trigger inve	0.31
79	1	74LS123N 1455-8123	Multivibrator	0.35
80	7	2743021446 PSC ELECTRONICS	SMT FERRITE BEAD 10U	1.30

Total Parts Used: 416
Total Parts Cost: 1133.88
Board Cost ~ $300
Board Assemble ~$150

TOTAL ~ $1582

APPENDIX B

TRACER PCB VIEW

APPENDIX C

Master Clock and TSI Cabling Note

T_M_SHAW 060396
Revised 6/14/96

Proposal for Master Clock Fanout Cable and TSI Return Cable

A set of proposals were made at the end of the CDF infrastructure meeting on May 22, 1996 on how to cable the TSI return signals and the Master Clock. What follows is the result after feedback from all (we hope) systems.

Master Clock Fanout Cabling

- Assume the use of National's LVDS differential line drivers and receivers. P/Ns are DS90C032 and DS90C32. Testing done by Steve Chappa has verified that there are no problems with these devices.

- Cable Termination at the Receiver end should consist of a SMT resistor (100 ohms) across the differential inputs which matches the cable impedence.

- While most systems require 4 signals, at least one system (SVX) has identified the need for five signals. It was decided at the clock meeting on 6/13/96 to simply run an additional "CABLE B" to such systems. CABLE B will contain the 53Mhz clock required by SVX.

  This decision allows us to continue to use the high quality Category 5 cable we have tested (4 pair limit), as well as the connectors. CABLE A and CABLE B will have different keys to prevent them from being switched at front panels.

CABLE PINOUT for CDF Readout Crate with TRACER

CABLE A

Pin	Signal	
1	Master_Clock	(132 ns clock)
2	Master_Clock*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

CABLE B

Not Required

CABLE PINOUT for "SVX-like" Readout Crate

CABLE A

Pin	Signal	
1	Sync	(one tick every 132 ns clock)
2	Sync*	
3	Beam_Crossing	
4	Beam_Crossing*	
5	Beam_Zero	(once around marker)
6	Beam_Zero*	
7	Abort_Gap	
8	Abort_Gap*	

CABLE B

Pin	Signal	
1	53MHz_Beam_Clk	(one tick every 132 ns clock)
2	53MHz_Beam_Clk*	
3	N/C	
4	N/C	
5	N/C	
6	N/C	
7	N/C	
8	N/C	

BOARD MOUNT CONNECTORS

(AMP Catalog 82101)

CABLE A

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry Panel and PCB Ground
Part # 3-520459-3
(Note: this part uses the **"C"** key to distinguish it from the TSI return cable)

CABLE B

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry Panel and PCB Ground
Part # 5-520459-3
(Note: this part uses the **"E"** key to distinguish it from the TSI return cable)

CABLE CONNECTORS

Cable - Plug Assemblies for Round Cable (order 1 part each per cable end)

Sub- assembly	Part # 3-520424-3	**"C" key**
Sub- assembly	Part # 5-520424-3	**"E" key**
Top Shield	Part # 520464-1	
Bottom Shield	Part # 520465-1	
Ferrule	Part # 520437-1	
Boot	Part # 520853-1	

Trigger System Interface - DONE, BUSY, ERROR cable

- The proposal is to use the same differential line drivers, National's LVDS DS90C032 and DS90C32 as we are using for the clock fanout.

- The same PCB board mount and cable connectors will be used, with the exception that these will have **"A"** key coding. This is being done to prevent someone from mixing the TSI return cables with the clock fanout cables.

Board Mount Connectors:

AMP Shielded Data Link Connectors, 8 Conductor, Side Entry PCB Ground
Part # 1-520459-3 **"A"** Key

Cable - Plug Assemblies for Round Cable (order 1 part each per cable end)

Sub- assembly	Part # 1-520424-3 "A" Key
Top Shield	Part # 520464-1
Bottom Shield	Part # 520465-1
Ferrule	Part # 520437-1
Boot	Part # 520853-1

PINOUT

Pin	**Signal**	
1	DONE	
2	DONE*	
3	ERROR	
4	ERROR*	
5	BUSY	
6	BUSY*	
7	L1_DONE	(This signal is unique to SVX)
8	L1_DONE*	

Other Useful Part Numbers

Hand Tools required for Cable assembly

Connector Hand Tool Frame	Part # 58194-1
Die Sets for Connectors	Part # 58195-3
Ferrule Hand Tool Frame	Part # 69710-1
Die Sets for Ferrules	Part # 1-58166-2

Cable
Teststand use:
Category 5, PVC jacketed Cables/overall Bedfoil Shield, 4 Pair Part # 1633A
Available Now

Category 5, Plenum-Paired Cables/overall Bedfoil Shield, 4 Pair Part # 1646A
Available 1/97
(Beldon Wire and Cable Catalog)