# SLIC Numbers

- **I/O (Cypress Hotlinks) @ 160 MHz or Mbit/s**
- **Internal data links 39 bits wide, @ 40 MHz**
- **5 DSP's (integer), 16 registers, @ 160 MHz**

  **Memory = 64K(prog)+64K(data)+128K(ext)**
- **Event Sizes; ~100 Bytes per input channel**

  **input = 1KB output = 50B**

# SLIC Status

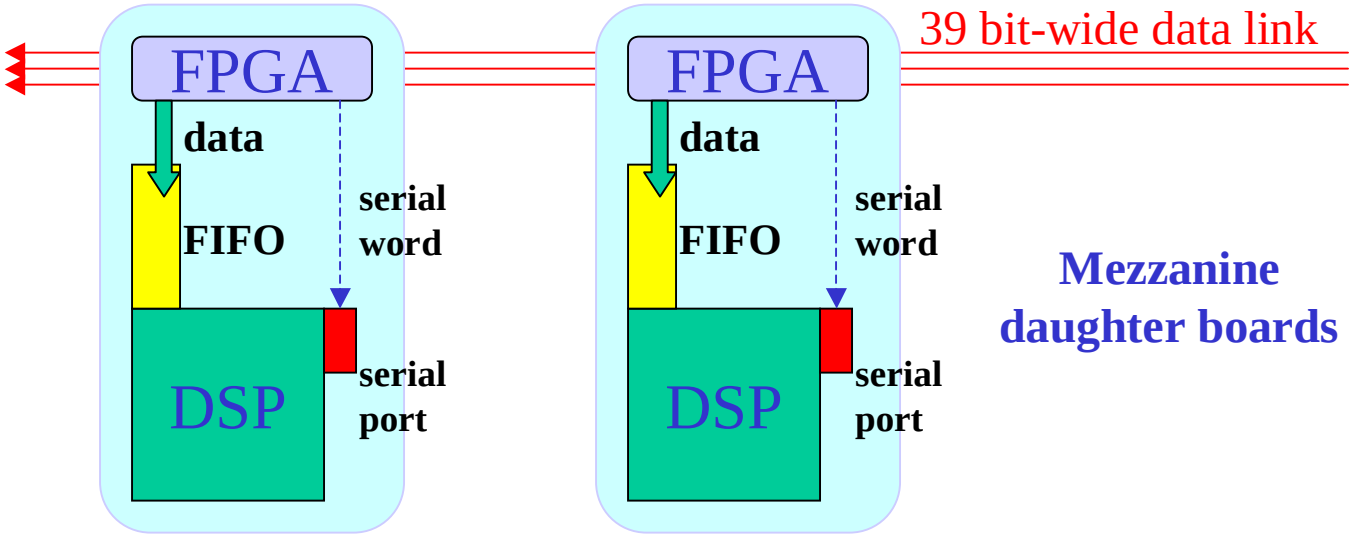
- Production (20 units) completed
- Single board tests successful
- Data transfer to/from other L2 boards
- BIST from FE crates w/ real cable path
- Robustness tests and Systems integration;
  - UAZ tester board for multiple SLIC tests and downstream integration
  - DSPs currently boot with "echo data"

# Central A-Layer East Slic

(one DSP per octant)

| Channel | Data Source | Source Index | Routing Bits |
|---|---|---|---|
| 0 | SCL | | 11111 |
| 1 | idle | | |
| 2 | side scint | 050 | 00110 |
| 3 | idle | | |
| 4 | top scint | 051 | 00001 |
| 5 | bottom scint | 056 | 01000 |
| 6 | PDT | 010 | 00010 |
| 7 | PDT | 020 | 00110 |
| 8 | PDT | 030 | 00100 |
| 9 | PDT | 011 | 00001 |
| 10 | PDT | 021 | 00001 |
| 11 | PDT | 031 | 00001 |
| 12 | PDT | 016 | 01000 |
| 13 | PDT | 026 | 01000 |
| 14 | PDT | 036 | 01000 |
| 15 | idle | | |

# DSP Input Memory Management



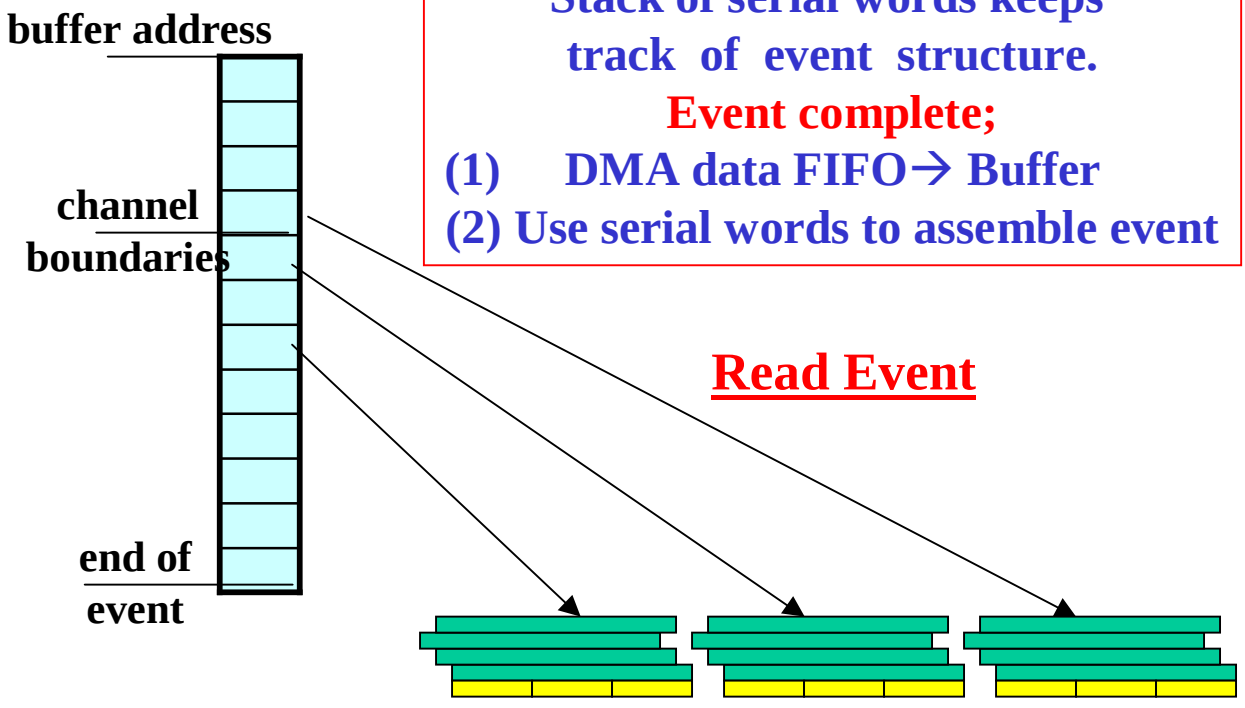

**Inside DSP;**

Stack of serial words keeps track of event structure.

Event complete;

(1) DMA data FIFO → Buffer

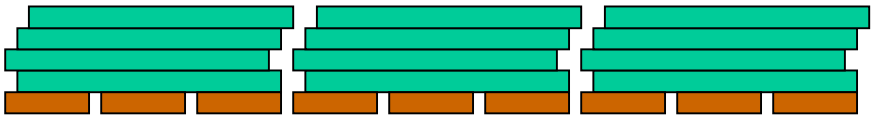
(2) Use serial words to assemble event



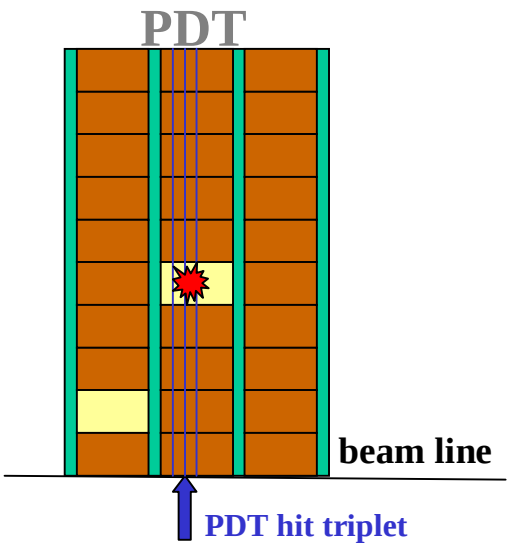

Algorithm-dedicated detector structures.
Example; central A-Layer , one octant

# Detector Structure Associated with Central A Layer DSP Algorithm

3(barrels) x 4(decks) of PDT's



3(barrels) x 3(z-rows) x 10(phi) APhi tiles



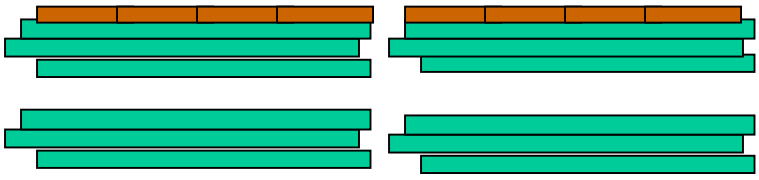

obs: wire-only or scint-only
stubs are not being considered

# Detector Structure Associated with Central BC Layer DSP Algorithm

2(barrels) x 4(z-rows) x 2(phi) Cosm. tiles

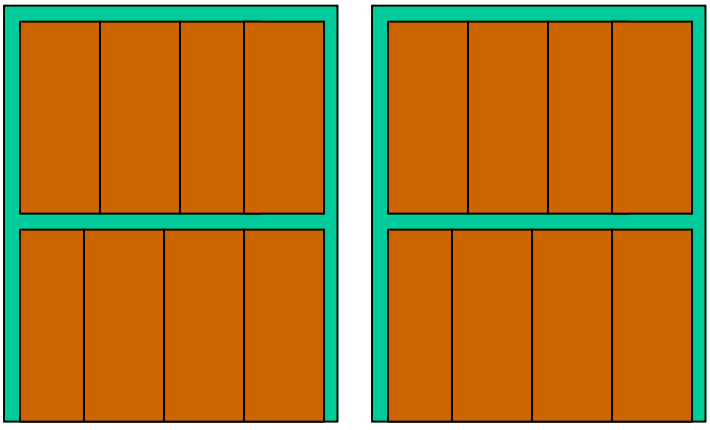
3 (barrels) x 2(layers) PDT's

Side View



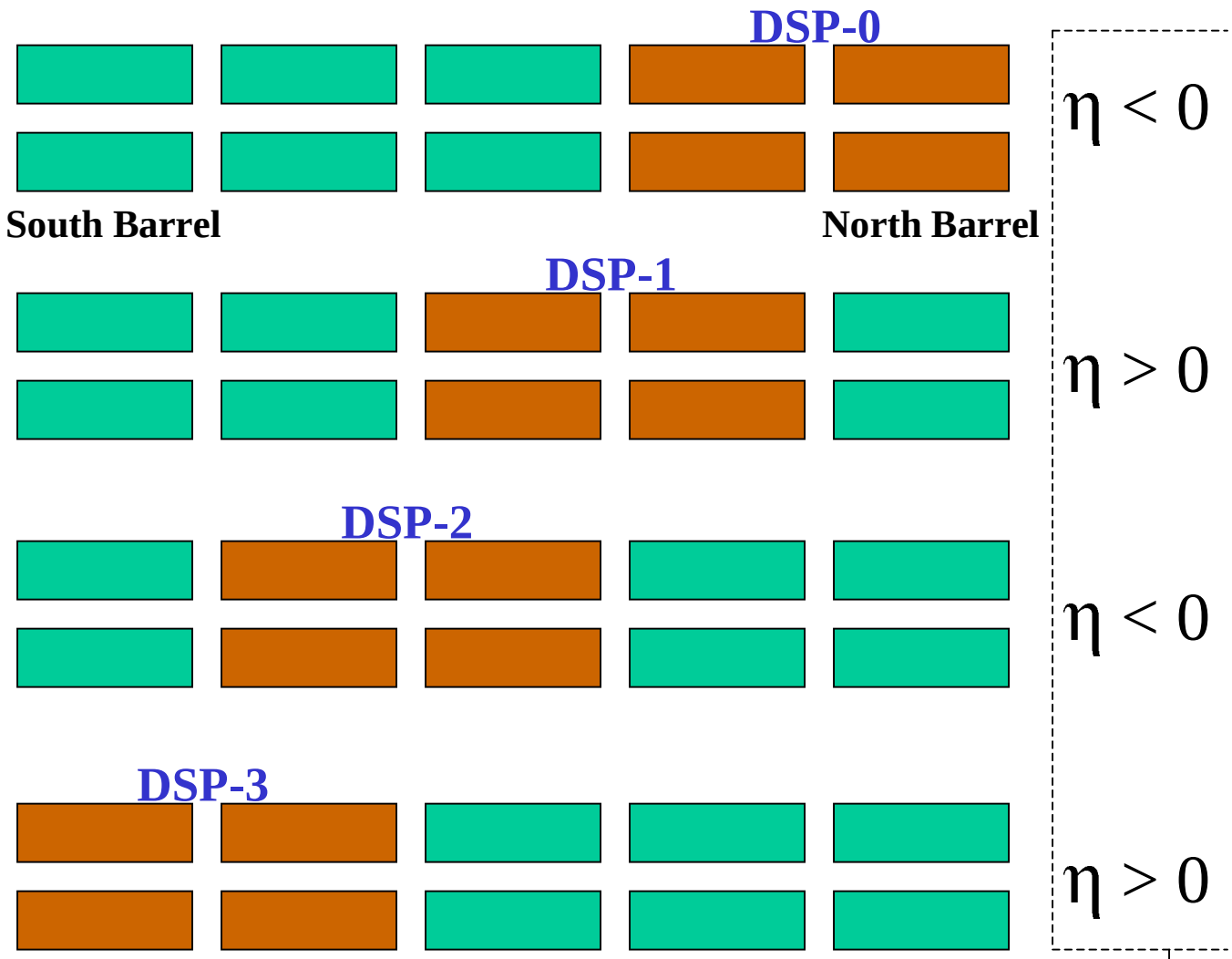
beam line

Top View



# Central BC-Layers DSP Split

**(one SLIC - 4DSP's - per octant)**




- DSP's do tracking on a 6-deck "hyper chamber"
- Tables are such as to prevent track duplicates
- Segment finding requires 3 hits out of 6. Accept single chamber triplets only at geometry gaps
- Four or more hits on track, waive residual test

# DSP Algorithms

**Central-A**

- **~done (Sergey + AM)**
- **Needs fine tuning**
- **Bottom A-layer**

**Central-BC**

Sergey U. (ITEP)

**Forwd-A**

**Forwd-BC**

**Raimund S. and Tim C.**
**(& the U. Munich team)**

**DSP-L1**

simple, design ~done
needed for simulator

**DSP-5**

**Monitoring**

coupled with hard-
ware development