Chapter 5

Pixel R&D

5.1 Introduction

The BTeV pixel detector is central to the capability of the BTeV experiment. At the same time, it stretches the technical frontier beyond what has so far been achieved in other experiments. In these circumstances, the plan has been to gain experience in the various required technologies and to demonstrate the necessary component capabilities that will be needed for the final device. In following this plan, as much as possible we have collaborated with industry and with groups working on LHC experiments developing similar detectors.

The major components for the pixel detector system are the sensor, readout chip, sensor-to-readout-chip connection, mechanical support and cooling, high-density interconnection between the readout chips and the control chips on the detector plane peripheries, and the multiplexing and data transmission to the first-level trigger. Details on the current state of R&D on these areas from various groups and industry can be found in [1]. For some components, we have demonstrated capability beyond that required for the baseline BTeV detector (e.g., 30μm-pitch bump bonding for sensor-to-readout-chip connection, while the baseline calls for 50μm pitch). For others we have demonstrated capability which meets the tough BTeV specifications (e.g., front-end amplifier of the FPIXi designs). For yet other components, we can make straightforward extensions to devices already tested which, when modified, will meet the BTeV needs (e.g., readout architecture). Finally, there are areas where additional work will be needed to get to the final Technical Design Report level (e.g., higher-level integration of components and radiation-hard implementation of the ASIC design). One choice that we will have to make in implementing a radiation-hard front-end is between deep sub-micron CMOS processes and more traditional radiation-hard technologies. We are just beginning to gain experience with yields for our readout chip designs, and have started a program to test yields at the component level too (e.g., for bump bonding).

On the road to gaining local experience and demonstrating necessary components, we have an active program of work in the MT test beam. We are ready to test two versions of Fermilab readout ASICs bump bonded to sensors (with pixel size of 50μm by 400μm). By the time of the TDR, we should have gained experience in assembling and operating multichip modules which will be the basic building block of the final BTeV pixel detector. We also have a physical simulator of the electrical noise from the Tevatron beam for testing electronic components and their shielding inside the beam vacuum-pipe. We are also preparing to place devices into the Tevatron in borrowed Roman Pots as a test of the designs which grow out of the simulator experience.

Finally, we have begun to develop industrial contacts and joint efforts with other experiments on the remaining areas. We have ordered test components for high-density interconnects (HDIs), fiber-optic data transmission, support structures, and cooling channel prototypes. Test stands for these are in various stages of construction, and making rapid progress.

5.2 Sensor development

5.2.1 Introduction

The sensor unit cell size is closely related to the achievable spatial resolution and to the occupancy in the system. The sensor thickness affects the signal-to-noise ratio achievable in the course of the detector lifetime, the overall material budget and the power dissipation of the system, in particular after large irradiation doses. The overall material budget is determined not only by the active elements (sensor and readout electronics), but also by our ability to design a low mass mechanical support and cooling system.

One of the key elements driving our design is the necessity to put these detectors as close to the beam line as possible, in order to optimize the vertex resolution. In our baseline geometry, the inner detector edge is located 6 mm from the beam line. As a consequence, the inner portion of our detector will be exposed to radiation levels comparable to the ones expected for the LHC experiments. One of the effects produced by high-energy particles on semiconductor devices is displacements. These are dislocations of atoms from their normal sites in the lattice, producing defects and trapping sites. Displacements determine the degradation of the bulk material. In detectors, they cause changes of the internal electric field due to the modified doping concentration. For very-high-dosage irradiation, this will eventually lead to inversion of the conduction type of the bulk material (type-inversion), increases in leakage current and depletion voltage, changes in capacitance and resistivity, and charge collection losses. The key to ensure that the sensor could still provide useful signal after high radiation dosage is to be able to operate the detector at high voltage. In order to do this, the breakdown point must be increased and controlled. A common solution to this problem is to use multiple guard rings [2].

In order to increase the useful operating time of the silicon sensors, running with partial depletion has to be considered. This is more suitable for n-type pixel readout, since the depleted region will grow from the n^+ side of the junction after type inversion. Thus, the sensor technology preferred is the so-called "$\mathrm{n}^+/\mathrm{n}/\mathrm{p}^+$" adopted by both ATLAS and CMS pixel systems [3, 4], where the collection electrodes are n^+ pixels and the p^+ implant biases the back of the detector.

Results from PSI for CMS showed that for a fluence of $6 \times 10^{14} \pi/cm^2$, a depletion depth of 150 μm is obtained for 300 volts. At high bias voltages, charge trapping in the depleted region is below the 10% level. [4].

For an n^+/n pixel detector, the charge-collecting pixels are defined by n^+ implants. Due to the oxide-charge-induced electron accumulation layer between the silicon and silicon oxide, neighboring n^+ implants will be shorted together unless they are isolated from one another. There are two techniques to implement the isolation: p-stop and p-spray. In the p-stop isolation, a high dose p-implant surrounds the n^+ implant. In the p-spray isolation, a medium dose p-implant covers the whole n-side and the collecting n^+ pixels are done by overcompensation with the high dose of n^+ implant [5]. The ideal design for the p-stop (single, common or multiple, width and spacing of the p-implants) needs to be determined. It will have a significant impact on the minimum pixel pitch, the noise, charge collection, and capacitance of the sensor. Recent studies by both ATLAS and CMS also showed that in order to keep the field low for non-connected pixels (failed bump bonding) so as to avoid stochastic discharges, the p-stop has to be designed carefully to create a high resistivity accumulation path between neighboring pixels. The advantages of the p-spray technique is that one or two mask steps and the risk of overlapping implants will be eliminated. A finer pitch will also be possible. A further advantage of the p-sray is that the electric field in the region between the p-spray and the n^+ implant decreases with increasing irradiation, minimizing the risk of micro-discharge.

The use of p^+/n detectors in a high radiation environment also needs to be studied. One interesting option in this case is to go to thinner detectors (say 200 to 250 μm) and lower resistivity silicon(say around 1K ohms-cm). Simulations show that such detectors can be fully depleted at a voltage no higher than 300V up to a fluence of a few times 10^{14} particles/cm^2.

There is a new development on radiation hardened silicon reported by the CERN RD48 (Rose) collaboration. Radiation hardness of silicon detectors can be significantly improved by using oxygen-diffused silicon. Various silicon detector manufacturers, working in collaboration with RD48, have started on a program of optimization of the oxygen diffusion process. We plan to get some pixel detectors made from oxygenated silicon wafers.

5.2.2 Sensor simulation

A detailed understanding of the factors affecting the sensor performance is crucial to its design. We have studied a number of issues through simulation.

In a n^+/n detector the charge carriers collected at the pixel electrode are electrons. We have studied these n^+/n sensors , as well as the conventional choice of p$^+$/n pixel devices, which have holes as the collected charge. In addition, we have considered radiation damage effects. These include the deterioration of the noise performance due to the increased leakage current and the change in detector response induced by the change in the effective donor concentration.

Other factors that affect the ultimate resolution achievable in this system are related more closely to the design approach and the performance of the readout electronics. In particular, the electronic noise, and the threshold that determines the minimal charge deposition that will be recorded as a signal hit, are important. The sensitivity to these parameters has been studied, as well as the tradeoff between analog and digital readout.

In order to understand these effects, we have developed a stand-alone simulation, based on a two-dimensional model of the signal formation in silicon. This program has been interfaced with the Monte Carlo software used to study our physics reach. This integration allows us to have a more realistic model of the detector occupancy, crucial in trigger simulations, and also provides a more realistic implementation of the hit resolution achievable for different track angles of incidence.

While this simulation program has lead us to a much better understanding of the interplay between hit resolution, occupancy and physics reach of our experiment, an additional effort is under way to develop a more accurate model of the static and dynamic properties of the pixel sensors, taking into account the true three-dimensional nature of the electric field distribution and signal charge-flow to the collection electrode. These studies will be crucial to determine our final sensor choice.

5.2.2.1 Spatial resolution studies

We have developed a program to evaluate the spatial resolution achievable with different sensor and readout electronics specifications[6]. Our approach is similar to several other studies performed for silicon microstrip detectors [7], [8]. We have investigated the interdependence of charge diffusion, magnetic field effects, electronic noise, discriminator threshold and number of bits in the back-end electronics.

The ability to achieve a spatial resolution better than the nominal 'digital' resolution (σ=width $/\sqrt{12}$) is closely related to how accurately we can interpolate between the location of the centers of individual pixels, using the information of the reconstructed charge collected at each sensor in a cluster.

We have modeled the charge produced by the minimum ionizing track traversing silicon using a Landau probability distribution. Electrons and holes produced by the energy deposited by the track drift along the electric field lines ($\vec{E}$) in the detector. The equations describing this drift motion are:

$$\vec{J_n} = q\rho_n\mu_n\vec{E} \tag{5.1}$$

$$\vec{J_h} = q\rho_h\mu_h\vec{E} \tag{5.2}$$

where q is the electron charge, μ_n and μ_h are the mobility of electrons and holes respectively, ρ_n is the number of free electrons per unit volume, and ρ_h is number of free holes per unit volume.

In parallel, the charge cloud spreads laterally due to diffusion. The parameters characterizing the drift in the electric field (μ_h, μ_e) are related to the parameter describing the diffusion of the charge cloud (D_h,D_e) by the Einstein equation:

$$D_{h(e)} = \frac{kT}{q}\mu_{h(e)} \tag{5.3}$$

where D_h and D_e are the diffusion coefficients, q is the electron charge and kT is the product of the Boltzmann constant and the absolute temperature of silicon. The average square deviation with respect of the trajectory of the collected charge without diffusion is $< \Delta r^2 >= 2D\Delta t$. In our study we have used $\mu_h = 400\ cm^2/Vs,\ \mu_e = 1450\ cm^2/Vs$.

When the silicon detector is located inside a magnetic field, there is an additional source of charge spreading: the lateral motion induced on electrons and holes by the magnetic field. This effect shifts the centroid of the detection point of the charged cloud and also widens it, because the amount of drift is proportional to the path length of the detected electrons (holes). This so called "$E \times B$ effect" depends on a parameter called the Hall mobility μ_H, proportional to the charge carrier mobility discussed above. In order to take into account the effect of the magnetic field in the bend plane, the following values of the Hall mobility have been taken from experimental data quoted in [9]:

$$\mu_{H,h} = 0.72\mu_h, \tag{5.4}$$
$$\mu_{H,e} = 1.15\mu_e. \tag{5.5}$$

The charge-cloud image appears on more pixels when the incident track crosses the detector at an angle, as the generation point of the electron-hole pair spreads out along the track path length. These various effects are illustrated in Fig. 5.1, which shows the charge broadening due to diffusion, the magnetic field and the combination of the these two effects together with track inclination with respect to the normal to the detector.

An analog readout improves the spatial accuracy by charge weighting. A low intrinsic noise is obviously a key element in this approach, together with a low and uniform threshold. These features are important, not only to maintain the advantages of an analog readout, but also to minimize problems in data flow related to excessive data transfer. Finally, the achievable digitization resolution and the knowledge of the gain of the analog front-end are additional issues that should not be overlooked. We will address the interdependence among these parameters.

Two assumptions are common to all the configurations discussed in this study. We have considered a 300 μm thick Si detector biased in over-depleted mode (200 V for a detector that is fully depleted at 120 V). In this first stage we have assumed full charge collection and we have assumed negligible capacitive cross talk between adjacent pixels. These assumptions will be relaxed in subsequent studies.

5.2.2.2 Factors affecting the spatial resolution

We have carefully examined the different factors affecting the hit resolution in the small pixel direction, both in the bend plane and in the direction orthogonal to it, with reference to a pixel geometry of 50μm $\times$ 300μm, using several track orientations.

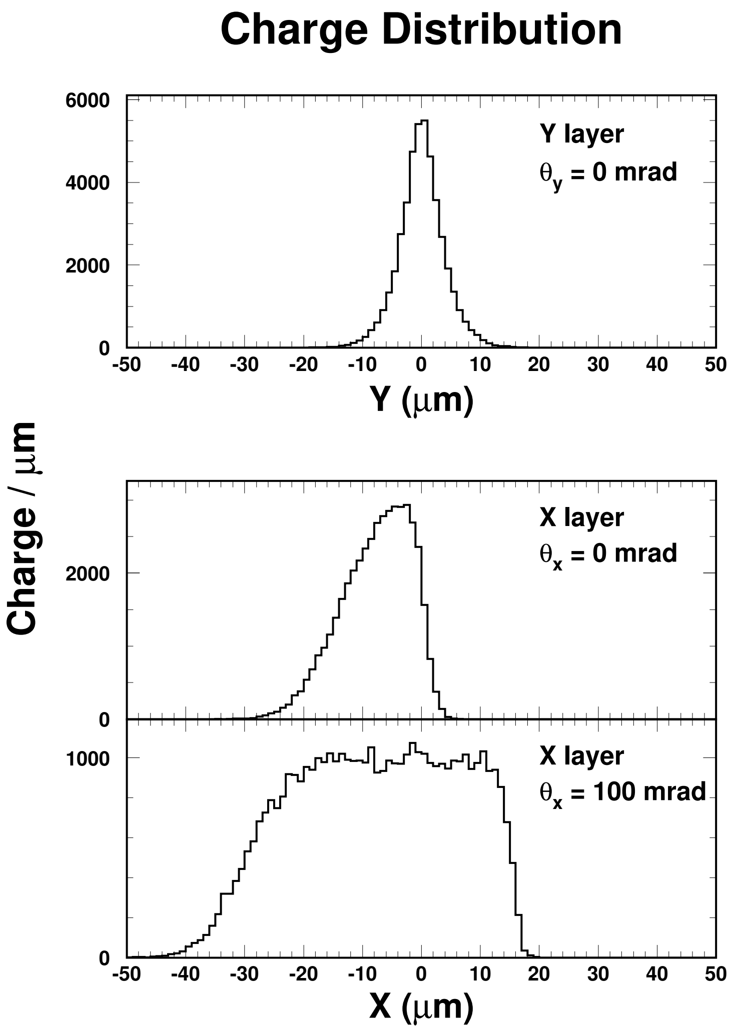

Figure 5.1: Collected charge spreading in a 300 μm silicon detector a) produced by diffusion, b) produced by the interplay of diffusion and the magnetic field for B=1.6T, and c) produced by diffusion and magnetic field effects when the charged track is incident at an angle of 100 mr in the bend plane.

Fig. 5.2 shows the relationship between the position of incidence at the pixel plane and the reconstructed coordinate for tracks at normal incidence on the pixel detector, whereas Fig. 5.3 assumes a track inclined at an angle $\theta_x = 300mr$. We have started our study assuming a readout scheme with the intrinsic electronic noise switched off, and we consider both a binary and an analog readout (with 6-bit ADC resolution). We can see that if the electronics noise is negligible, a digital readout actually can achieve a better resolution than the naive expectation of the width of the cell divided by $\sqrt{12}$. This is due to the fact that when the charge is shared between two or more pixels it is possible to do a digital charge weighting algorithm that provides some interpolation between the position of individual pixels. This improvement is constant, on the average, for different angles.

Let us start our discussion on analog readout with tracks at normal incidence. Fig. 5.2 shows that, in presence of the magnetic field, the charge is actually 'focused' inside the pixel instead of spread out by virtue of the magnetic field. This makes the analog and digital readout equivalent, because there is not a second pixel helping to interpolate the track position using charge sharing. On the other hand, tracks incident on the pixel region where the magnetic field spreads the charge further with respect to diffusion, are helped significantly by analog readout. In order to take full advantage of the analog information, it is necessary to adopt an optimal choice of the charge weighting algorithm that reflects the expected distribution of the charge profile. In particular, the center-of-gravity linear weighting algorithm is suitable only for relatively large angle tracks, where enough charge sharing is produced by the track inclination. For tracks at normal incidence, it is necessary to perform a non-linear weighting [8].

An additional important constraint in the achievable resolution is the discriminator threshold. In this study we have assumed that only the pixels having a signal above threshold are read out, and we have varied the threshold for analog and binary readout. Fig. 5.4.a shows the effect of increasing the threshold for an incident angle $\Theta_x = 300$ mr, for analog and digital readout respectively. Fig. 5.4.b shows the corresponding pixel occupancy. Each curve shows the fraction of events having N pixels hit for a given threshold. For instance, for a threshold of 1000 electrons, less than 5% of the events have 4 or more pixels hit, 45% have 3 pixels hit, and about 50% have two pixels hit. The resolution achievable for binary readout shows a characteristic oscillatory behavior as we change the threshold. The worst resolution is always at the thresholds for which most of the events have clusters with the same size, corresponding to less interpolation power. In the analog readout case, the higher the threshold is, the coarser the charge sharing process is. In several of the results presented below, we have assumed a threshold of 1000 electrons, a somewhat optimistic assumption, supported by promising initial test results on the FPIX0 pixel readout chip [10]. The slope of the threshold dependence of the resolution is not very high below 3000 electrons, as illustrated by Fig. 5.4, so the results are largely unaffected if we use less restrictive conditions.

Each readout circuit features some intrinsic noise, most commonly the series noise associated with the input transistor of the charge-sensitive preamplifier integrating the charge collected from the pixel sensor. In addition, at very high radiation damage, a contribution from the parallel noise produced by the excess leakage current may become non-negligible

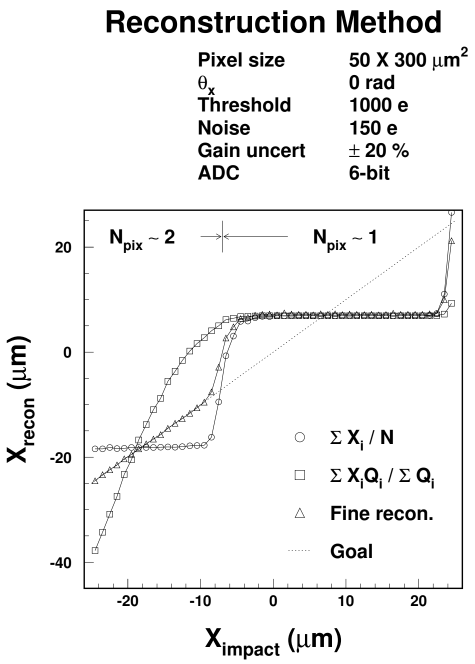

Figure 5.2: The reconstructed x coordinate as a function of the charged track impact point on the pixel cell for a pixel size of 50x300 μm^2 and normal incidence.

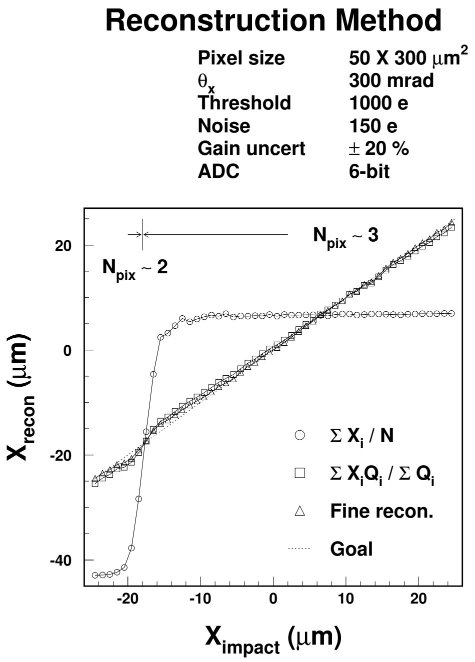

Figure 5.3: The reconstructed x coordinate as a function of the charged track impact point on the pixel cell for a pixel size of 50x300 μm^2 and incidence angle in the bend plane $\theta_X = 300$ mr.

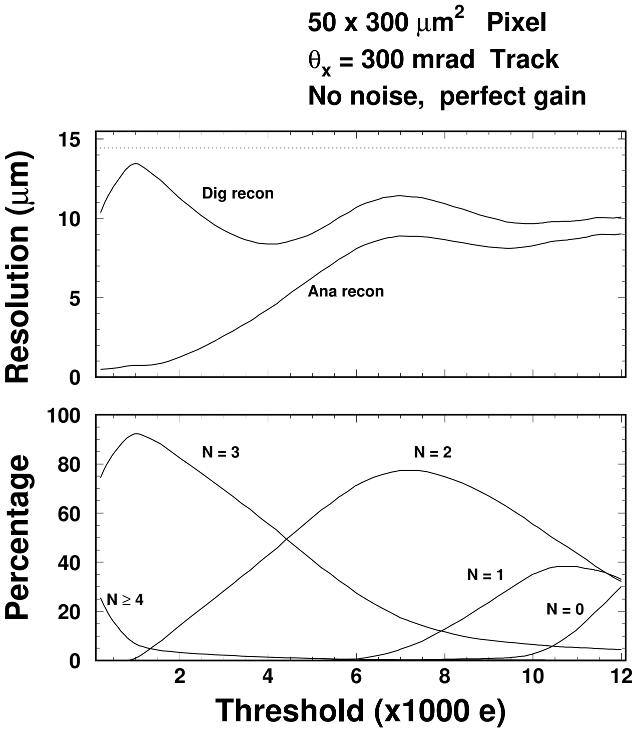

Figure 5.4: a) Spatial resolution in the reconstructed x coordinate as a function of the threshold for a pixel size of 50x300 μm^2 and incidence angle in the bend plane $\theta_X = 300$ mr. b) percentage of events having N pixels hit as a function of the threshold for the same configuration.

or even the dominant effect. A pixel detector has the potential for being a very low noise system, as the capacitive load at the input of the charge sensitive preamplifier is quite negligible. The recent results achieved at Fermilab in the prototype development of the front-end electronics for our pixel system are quite promising, and lead us to assume that an equivalent noise charge of about 150 electrons is an achievable goal. However to take full advantage of the low noise, the minimum threshold spread among channels needs to be comparable, otherwise either our assumption on the threshold needs to be modified or the effective noise is higher than assumed.

Fig. 5.5 shows the number of pixels hit as a function of the track angle for electron and hole collection. Fig. 5.6 shows the resolution as a function of the angle in the bending plane (θ_x), and in the non-bend plane (θ_y) expected with digital readout and with a 4 bit ADC respectively. At angles above ± 50 mr the resolution achieved with analog readout is significantly better.

One of the questions that we have addressed in this study is the interplay between maximum dynamic range and ADC resolution. The known shape of the Landau distribution, with a long tail above the most probable energy loss for a minimum ionizing particle in 300 μm silicon (24,000 electrons), suggests a dynamic range at least of 48,000 electrons. However, the goal of measuring the charge collected in the pixel with the maximum pulse height more accurately obviously conflicts with the accuracy of the charge measurement in the neighboring pixels at any given bit resolution. It is interesting to see the interplay of these two factors. We have studied this issue at two different angles in the non-bend plane: $\theta_x = 100$ mrad and $\theta_x = 200$ mrad. Fig. 5.7 shows the study at $\theta = 100$ mrad and Fig. 5.8 the corresponding results at $\theta = 200$ mrad. In both cases the solid line defines binary readout, quite insensitive to the dynamic range of the front-end electronics. However it can be seen that for the quite limited resolution provided by a 2 bit ADC, there is actually an optimum in the dynamic range at about 25,000 electrons. For higher resolution, this optimum appears to have a threshold, above which there is not much improvement in resolution achieved by increasing the dynamic range. At a larger angle (200 mrad), where the ratio between the maximum pixel charge signal and the signal in its neighbors becomes progressively lower, the results are consistent, but are even more favorable to the lower dynamic range.

Another effect that we have studied is the sensitivity of the hit resolution to the digitization accuracy of the ADC chosen. Fig. 5.9 shows a comparison of the performance of different ADC's for a threshold choice of 2000 electrons. There is a definite difference between the region within 100 mr of normal incidence and the rest of the solid angle. The angle θ_x is the track angle in the non-bend plane and the angle θ_y is the angle in the bend plane. In the former region the resolution improves smoothly from 10 to about 5 μm as the angle increases. The higher number of bits is helpful at larger angles, where a resolution of about 3 μm is achievable with a 4 bit ADC. Finally, a non linear response flattens the resolution achievable in the region of larger angles. Fig. 5.10 shows the effects of adding 450 electron rms threshold spread between different channels and of raising the threshold to 3000 electrons. We can see that it is quite valuable to be able to maintain a low threshold and try to achieve a 4 bit resolution in the ADC.

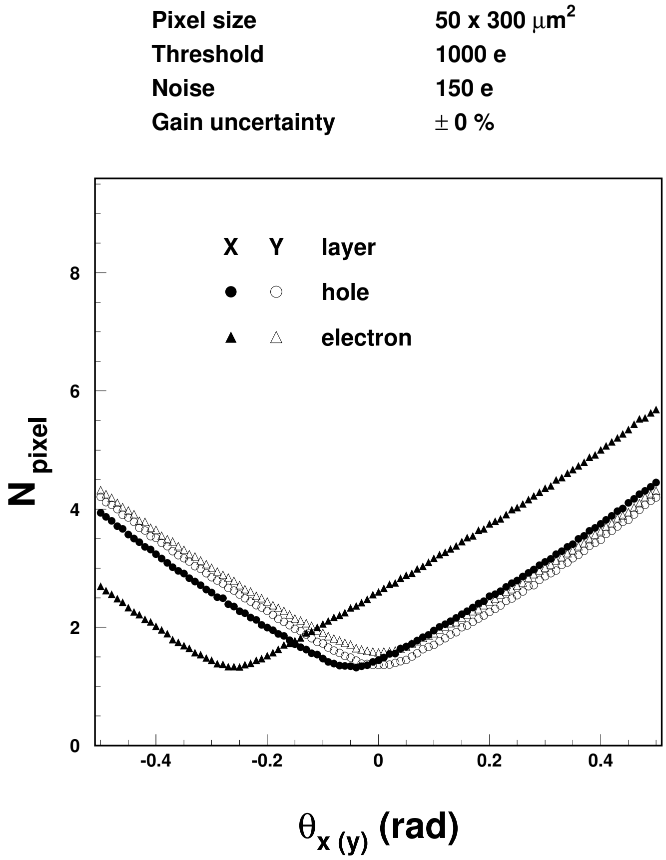

Figure 5.5: Number of pixels hit for a 50 μm pixel small dimension as a function of the track orientation.

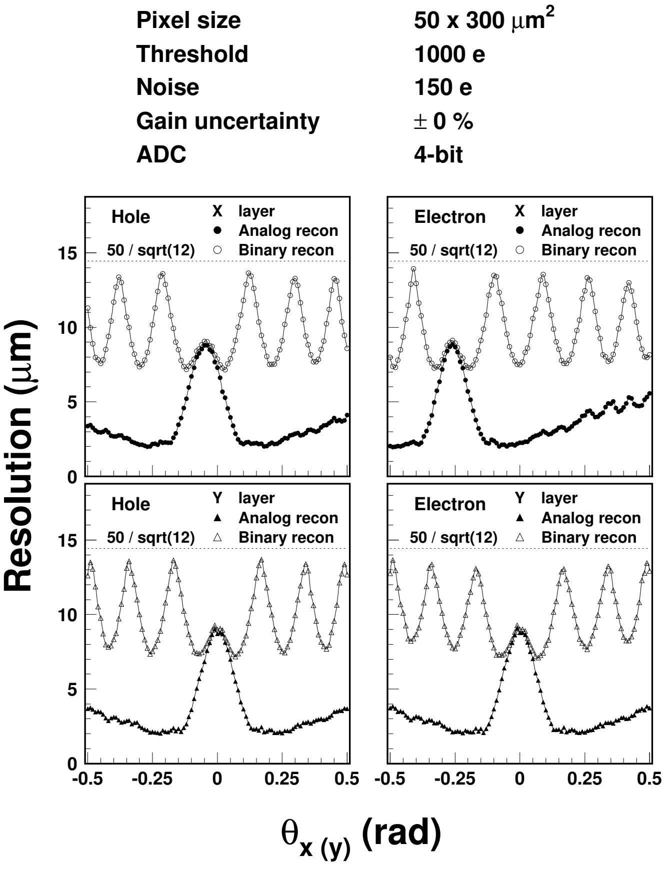

Figure 5.6: Resolution for binary readout and 4-bit ADC readout for 50 μm pixel small dimension.

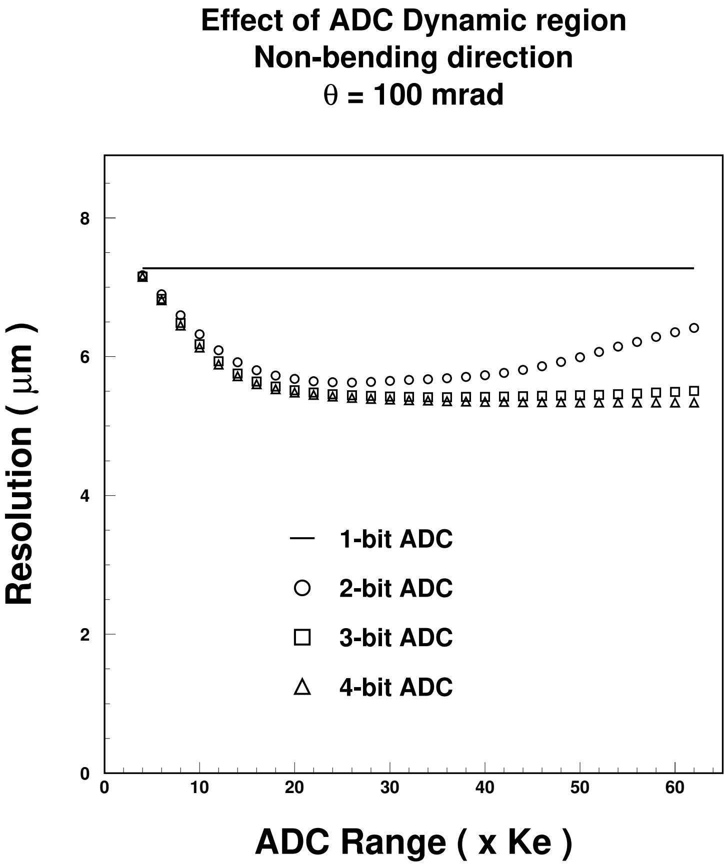

Figure 5.7: Effect of dynamic range of the ADC for different number of bits, for tracks incident at 100 mrad.

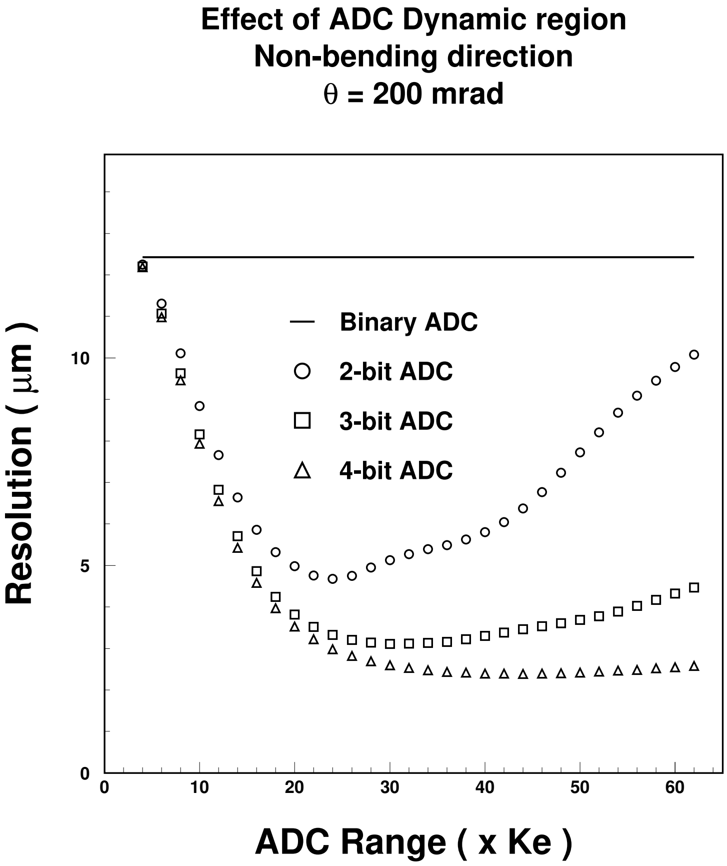

Figure 5.8: Effect of dynamic range of the ADC for different number of bits, for tracks incident at 200 mrad.

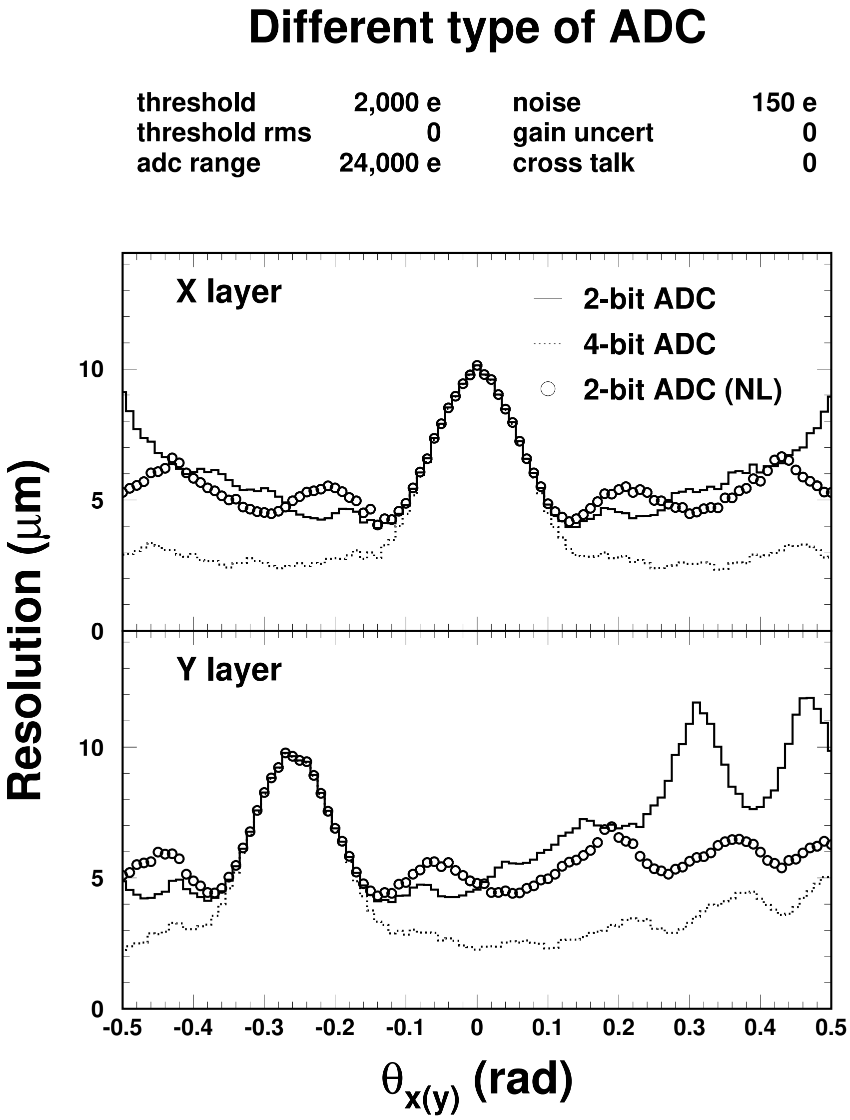

Figure 5.9: Comparison between different ADC resolution, with a nominal threshold of 2000 electrons and no threshold spread.

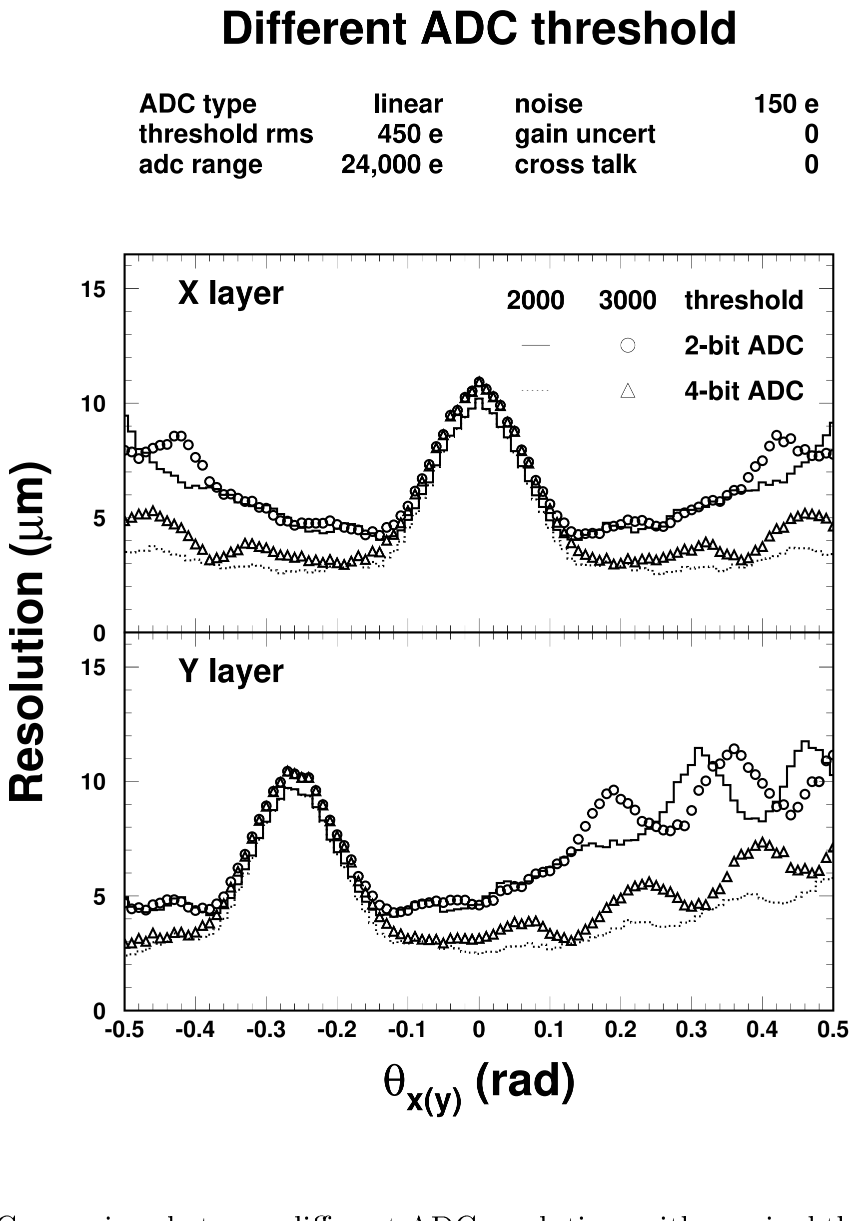

Figure 5.10: Comparison between different ADC resolution, with nominal thresholds of 2000 and 3000 electrons and a threshold spread of 450 electrons.

Table 5.1: Pixel occupancy for electron collection for different cell geometries and event type. One interaction per crossing is assumed.

	(30 μm x 500 μm)		(50 μm x 300 μm)	
	Light Quark Evt	B evt	Light Quark Evt	B Evt
npix/chip	0.87	1.76	0.65	1.30
ntrk/chip	0.26	0.51	0.25	0.52
ncol/chip	0.25	0.50	0.26	0.53
npix/trk	3.5	3.55	2.65	2.59
ncol/trk	1.03	1.03	1.06	1.06

Table 5.2: Pixel occupancy for hole collection for different cell geometries and event type. One interaction per crossing is assumed.

	(30 μm x 500 μm)		(50 μm x 300 μm)	
	Light Quark Evt	B evt	Light Quark Evt	B Evt
npix/chip	0.52	1.11	0.40	0.90
ntrk/chip	0.25	0.51	0.25	0.52
ncol/chip	0.24	0.50	0.25	0.53
npix/trk	2.16	2.24	1.69	1.79
ncol/trk	1.03	1.04	1.05	1.06

5.2.2.3 Study of the correlation between hit resolution and B decay time resolution for different detector configurations

The studies discussed above have allowed us to map the achievable hit resolution for any given geometry as a function of the track incidence angle. They have also provided us with more accurate information on the hit multiplicity associated with a given track angle. We have used this more realistic information to achieve a better understanding of several key features of our detector performance.

We have investigated[11] the occupancy in the inner portion of our detector for different event classes and different assumptions on the interaction rate. This study has been a crucial input for the engineering group responsible for the design of the pixel readout chip and to test the readout architecture and identify possible bottlenecks in the data throughput. The pixel occupancy has been studied for a chip located with its inner edge 6mm from the beam pipe. The chip has been modeled as an 8x8 mm^2 square. Two different cell geometries have been studied, 30x500 μm^2 and 50x300 μm^2: they correspond to two different choices of the pixel small dimension with the same unit cell area. The results of this study are summarized in Tables 5.1 and 5.2 for electron and hole collection respectively.

In light quark events, it can be seen that the average number of tracks per chip in this "hot" region is only 0.25: thus 75% of the events do not produce any tracks crossing any given chip located near the beam. This study also provides data samples for the readout architecture simulation and the trigger processor generator. Initial studies have shown that, assuming a pixel size of 50 μm x 400 μm and 2 or 3 bit flash ADC's digitizing the pixel cell signal, the proposed column-based data-driven architecture should be capable of achieving the hit readout rate required by the BTeV experiment [12].

The crucial parameter to determine the physics reach of BTeV is the vertex resolution, or equivalently, the resolution in the proper decay time. The time resolution is affected not only by the hit resolution in the pixel sensor and extrapolation distances, but also by the material in the pixel system, including the sensor, the readout electronics and the material used for mechanical support and cooling. The study of the effect of increasing the material budget in the detector system is currently under way [13]. The importance of keeping the material budget to a minimum is illustrated by a comparison of the time resolution achieved for the decay $B_s \to D_s K$ under two assumptions shown in Fig. 5.11. The top plot shows the resolution achieved with a pixel small dimension of 50 μm and pixel planes organized in stations containing 3 detectors whose material budget was described by three layers of thickness 0.6, 0.5 and 0.6 mm of silicon equivalent respectively. The bottom plot corresponds to the same geometry but with an increased equivalent Si thickness (1.1, 1.0, 1.1 mm). The time resolution degrades from 42 to 50 fs. This study illustrates the importance of keeping the material budget to a minimum.

The simulation included in the original EOI was based on an assumed hit resolution that was uniform throughout the sensor. However we have shown that the resolution improves substantially for angled tracks due to the increased charge sharing that allows a better interpolation. This more realistic mapping of the effective hit resolution has been introduced in our simulation and has shown that this improvement is quite important and compensates the adverse effects of having taken a more conservative model of the material included in our detector.

5.2.2.4 Non-Gaussian Resolution Functions

All previous discussions of the physics reach of BTeV, contained the approximation that the measurements produced by the pixel detectors had a Gaussian shape. With the simulation tools now available it is possible to remove this approximation and to demonstrate that a realistic shape for the resolution function does not significantly degrade the physics reach.

The information in the preceding sections was used to implement several different models of the pixel resolution in the MCFast. These models are discussed in detail in section 10.3. The third of these models, the fast clustering model, is the one of interest; it involves the generation of digitized pulse heights and the extraction of a measured coordinate from the pulse height distribution. The shapes of the resolution functions for this model can be seen in Fig. 10.2 parts c) and d). Both of these have significant non-Gaussian components. For reference, two other models will be considered, both of which have Gaussian resolution functions. In the first model the Gaussian has a constant $\sigma = \text{pitch}/\sqrt{12}$, while in the second model σ varies with angle of incidence. The resolution functions for the variable σ model can be see in Fig. 10.1; over the entire parameter space the resolution for the short dimension is better than pitch divided by $\sqrt{12}$. Also, careful inspection will show that resolution function

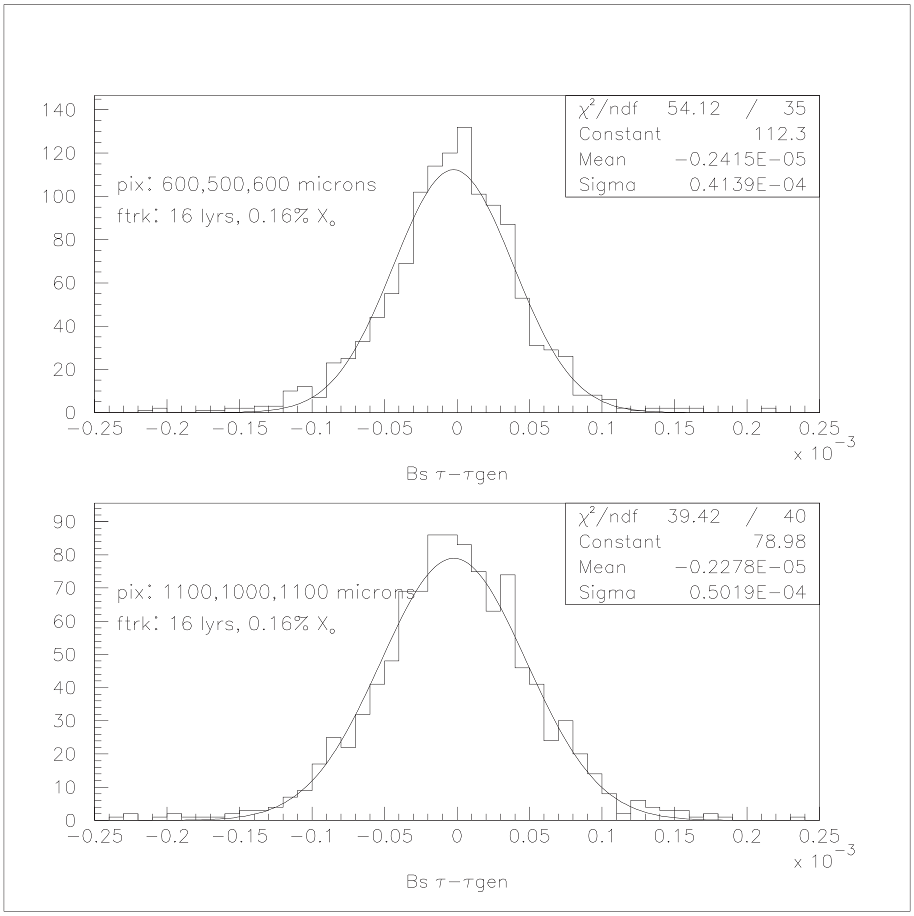

Figure 5.11: Comparison between the time resolution for two different assumptions of the material budget in a triplet station. The decay mode considered is $B_s \to D_s K$.

for the fast cluster model is slightly poorer than the resolution function for the variable σ model; the reasons are discussed in section 10.3.

In order to investigate the physics consequences of these different spatial resolution functions, the decay chain $B_s \to \psi \bar{K}^{*0}$, $\psi \to \mu^+\mu^-$, $\bar{K}^{*0} \to K^-\pi^+$ was considered. After all analysis cuts and background suppression cuts, the resolution on the proper decay time of each B_s candidate was computed. This quantity, in this decay mode, makes one of the most severe demands on the spatial resolution of the pixel detectors. The histograms in Fig. 5.12 show the distribution of this resolution over many reconstructed B_s candidates. In part a), the distribution is shown for the constant σ model of the pixel spatial resolution. In part b) the distribution is shown for the variable σ model and, in part c) the distribution is shown for the fast clustering model. The most prominent feature in these plots is that there is a large improvement in resolution going from constant σ to variable σ. This is expected because the variable σ model, as discussed above, has better resolution than the constant σ model. There is also an increase in yield, which comes from the improvement in detachment and isolation cuts which derives from improved spatial resolution. A third observation is that, when going from the variable σ model to the fast clustering model, only minor changes are seen, consistent with the small differences between the two models. The conclusion of this study is that the expected resolution is not significantly degraded when using a model with explicit pulse height generation.

Part a) of Fig. 5.13 shows the distribution of the quantity $(t_{\mathrm{measured}} - t_{\mathrm{generated}})/\sigma_t$ for the variable σ model of the pixel spatial resolution. Here t is the proper decay time of a B_s candidate and σ_t is its error, computed on a candidate by candidate basis. Notice that the distribution is very close to a unit Gaussian and that there are few outliers. This is expected because the underlying resolution model is Gaussian; the outliers come from the small number of cases in which fit seeds are outside the radius of convergence of the fitter and from the few cases in which the first order error propagation formulae do not work. All entries in these plots are for true signal combinations. Now compare this to part b), which contains the same plot for the fast clustering model, in which the underlying resolution functions are not Gaussian. The core of this plot remains consistent with a unit Gaussian but the number of outliers has clearly increased. The increased number of outliers are attributable to the tails of the pixel spatial resolution functions. The clear conclusion is that the increased number of outliers is small enough to be of no concern.

Parts c) and d) of Fig. 5.13 compare the confidence level of the fit of the $\mu^+\mu^-K^-\pi^+$ system to a common vertex. Again all entries are for true signal combinations. Part c) is for the variable σ model, in which the pixel resolution function is explicitly Gaussian; in this case the confidence level distribution is flat, as expected. Part d) shows the distribution for the fast clustering model which contains two sorts of non-Gaussian contributions, a box-like component in the core and long tails. The combined effect of these non-Gaussian components is the spike in the few bins near a confidence level of zero and a slight downwards slope in the body of the plot. The area in the spike is about 4% of the total area of the plot. Again the clear conclusion is that the introduction of non-Gaussian resolution functions does not raise significant concerns about the physics reach of BTeV.

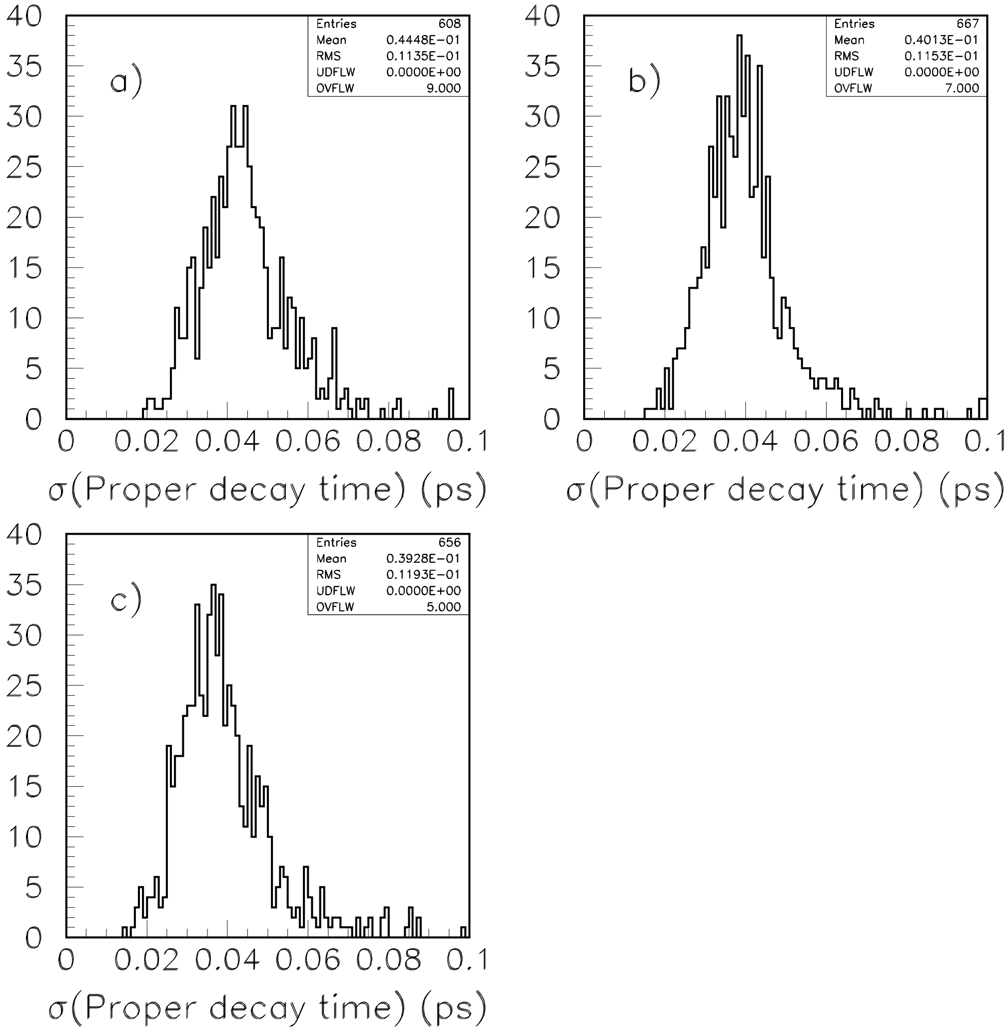

Figure 5.12: The expected resolution on the proper decay time for the decay chain $B_s \to \psi \bar{K}^{*0}$, $\psi \to \mu^+\mu^-$, $\bar{K}^{*0} \to K^-\pi^+$: a) for the constant σ model of the pixel spatial resolution; b) for the variable σ model; and c) for the fast clustering model. All entries are for true signal combinations. These models are described in section 10.3.

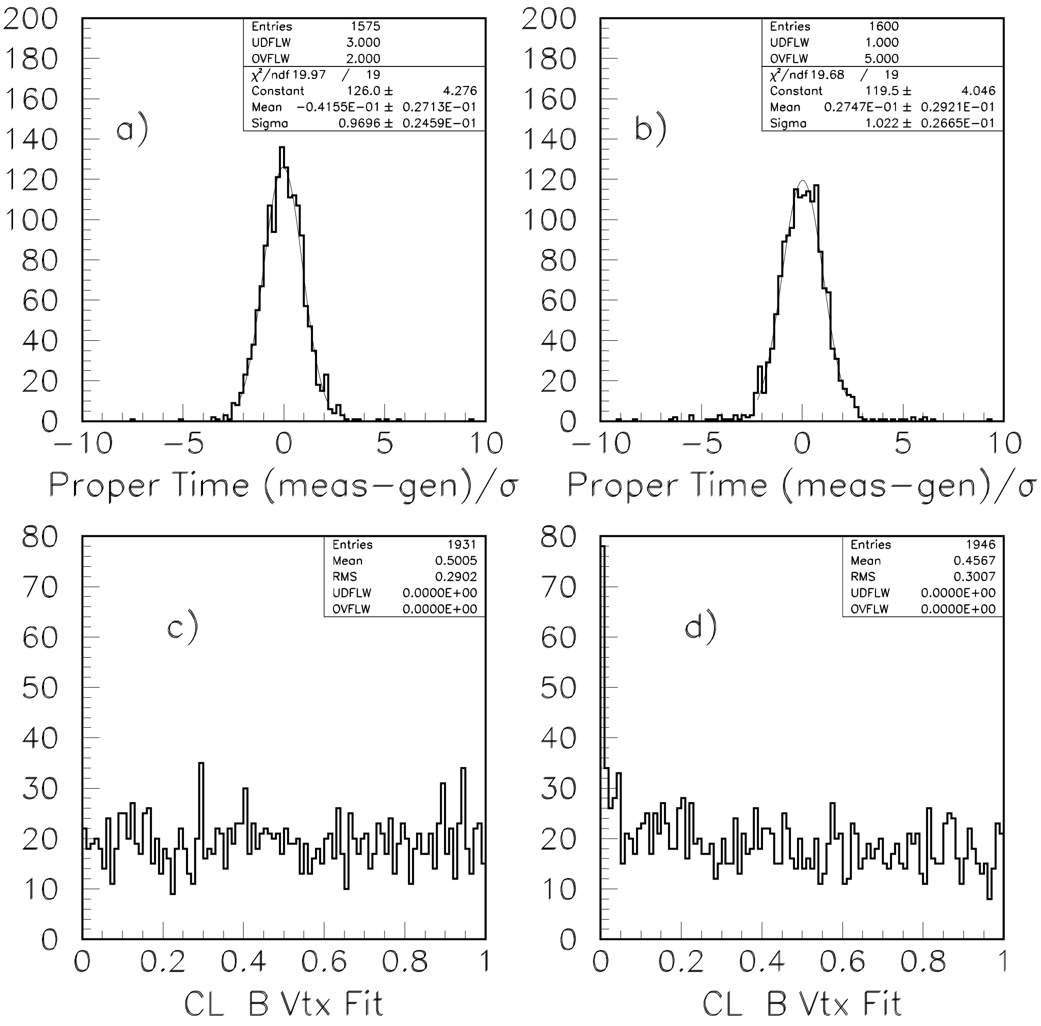

Figure 5.13: Parts a) and c) show quantities computed using the variable σ model of the spatial resolution of the pixels, in which the resolution function is explicitly Gaussian. Part a) shows the normalized residual on the proper decay time of a B_s candidate, while part c) shows the confidence level of the fit four tracks to a common vertex. All entries are for true signal combinations. Part a) is expected to be a unit Gaussian while part c) is expected to be flat. The reasons for the few outliers in a) are discussed in the text. Parts b) and d) show the same quantities for the fast clustering model, which does have non-Gaussian contributions; in these cases the deviations from the ideal behavior present but are small enough not to raise significant concerns.

5.2.2.5 Future sensor simulations

There are several other issues affecting the sensor performance that we would like to investigate. Some of them determine the optimal performance throughout the lifetime of the sensor while radiation damage effects accumulate. Other studies are dynamical in nature and will provide a more realistic model of the charge sharing between adjacent electrodes.

Our baseline sensor has a collection electrode on the ohmic side of the sensor (n^+). This requires a more complex geometry on this side in order to provide electrical insulation between the individual pixels, typically with p-stop or p-spray implants [14], [15]. These structures introduce additional complexity into our modeling of the sensor, by producing a lateral component in the electric field that sometimes has quite dramatic effects in the detector performance. It can introduce local regions of very high field that may determine the break-down voltage. In addition, it can produce modulation of the charge sharing between pixel cells introducing some lateral component to the drift motion that can increase charge sharing when the track crosses the detector at normal incidence [16]. It is intuitive to see that this electric field profile is of true tridimensional nature and thus requires 3-D simulation tools. We have chosen to perform our studies using a very sophisticated simulation program, DaVinci [17]. It has been used successfully by teams at CERN[9] and the University of Hawaii[18] to simulate their pixel sensors. The CERN group has even added an interface to study the charge collection profile in the presence of a magnetic field that we need to implement eventually if we want to model the charge collection in our experiment.

The issues that we are planning to study are:

1- a mapping of the electric field throughout the whole sensor (both inside the active volume and at the periphery for different guard ring configurations). This study is crucial to understand the sensor breakdown voltage and to design sensors that ultimately will withstand high reverse bias. The sensor is likely to be operated at high voltage during some stages of its lifetime. In addition, a detailed mapping of the electric field profile in these regions is an essential input to the the p-isolation design.

2- a study of the profile of the charge pulses in a cluster of neighboring pixels while we change the track impact parameter inside a central pixel. This study is crucial to understand the actual charge sharing between neighboring pixels and the expected pulse height with different sensors and at different irradiation doses. The radiation effects will be modeled with a different space charge density N_{eff} and with a degraded carrier lifetime due to the excess of trapping centers induced by radiation effects. In addition we are planning to introduce a realistic simulation of transport properties in the magnetic field.

These studies will be complemented by the extensive measurement program detailed in other sections of this chapter. In particular, the test beam data and extensive electrical characterization of sensors before and after irradiation will provide crucial tests of our model.

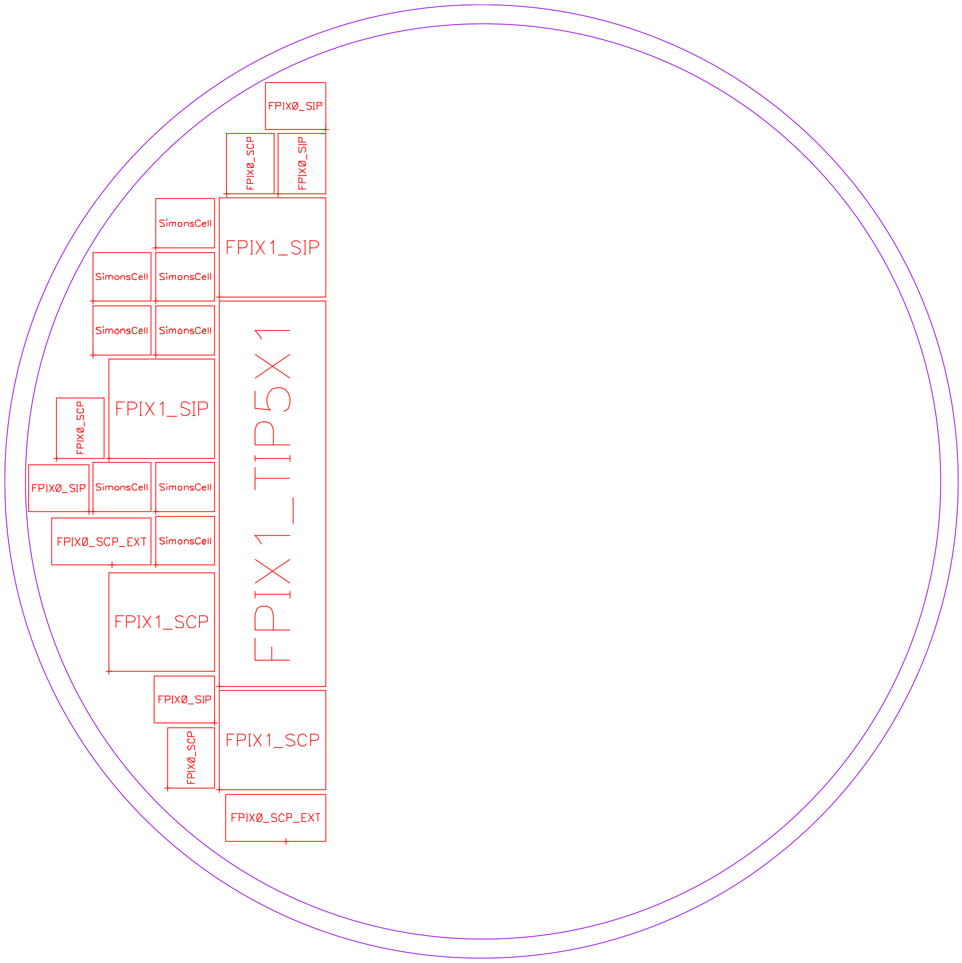

Figure 5.14: Wafer map

5.2.3 Prototype sensor

We have recently sent out for bids to a number of vendors for prototype sensor wafers, jointly with the US-CMS collaboration. The sensors will be n^+ on n with p-stop isolation between n^+ implants on the n-side of the wafer. Fig. 5.14 shows the wafer layout of the BTeV portion.

Our sensor designs are very similar to the p-stop designs of the ATLAS "First Pixel Prototype" [19]. We also borrowed heavily from their experience with the guard-ring design.

The BTeV portion of the wafer contains the following structures:

- FPIX1-SIP: A sensor with individual ("atoll") p-stops - designed to mate to a single FPIX1 readout chip (2 per wafer).
- FPIX1-SCP: A sensor with a single common p-stop - designed to mate to a single FPIX1 readout chip (2 per wafer).
- FPIX0-SIP: A sensor with individual ("atoll") p-stops - designed to mate to a single FPIX0 readout chip (4 per wafer).

- FPIX0-SCP: A sensor with a single (floating) common p-stop - designed to mate to a single FPIX0 readout chip (3 per wafer).
- FPIX0-SCP-EXT: A sensor with a single common p-stop which is extended to one side so that it may be biased - designed to mate to a single FPIX0 readout chip (2 per wafer).
- FPIX1-TIP5X1: A sensor with individual (”atoll”) p-stops - designed to mate to 5 FPIX1 readout chips (1 per wafer).
- SimonsCell: test structures(both diodes and pixels) with a variety of guard ring configurations (9 per wafer). Three different guard ring designs will be tested. These are the ATLAS design, the CMS-strip design [20], and a new design from BNL and Johns Hopkins University (JHU) [21].

Additional test structures will also be present on the wafer to monitor flat band voltages, layer thickness, implant resistivity, aluminum sheet resistance, etching uniformity and alignment. Our plan for this submission is to have enough sensors to be mated to the FPIX0 and FPIX1 chips and to gain experience on multichip-module assembly. We will also use the devices to do systematic studies on guard ring designs, p-stop designs, as well as effects such as surface damage, stability and variation from wafer to wafer and vendor to vendor. Irradiation studies will also be carried out so that dependence of the breakdown voltage, depletion voltage, and leakage current on the fluence can be studied.

A number of wafers will be made from oxygen-diffused silicon.

This round of submissions is focussed on p-stop designs. However, recent tests reported by the ATLAS collaboration show that the use of p-spray will significantly improve the performance of detectors after a radiation dosage exceeding 2x$10^{14} p/cm^2$. We plan to have a separate submission to vendors to study this technology. We will collaborate with the ATLAS collaboration on the submission and study of p-spray detectors.

5.2.4 Collaborative effort with BNL/JHU

Because of the commonalities of the problems faced by BTeV and LHC experiments, a close collaboration amongst various institutes is called for. We have collaborated with BNL and JHU on sensor development. BNL possesses facilities to fabricate high quality prototype detectors. The advantage of this path is cost-effectiveness and fast turn-around. As a result of our collaborative effort, a large number of detectors of various configurations have been fabricated and tested under different processing conditions [22, 23]. BNL can now produce good detectors reliably. Various guard-ring designs have been studied and improved upon. So far, we have demonstrated that n^+/n devices can be operated at 500v without breaking down, both before and after irradiation. Single pixel devices with pixel pitch of 60 and 120 μm with common or atoll p-stops have also been studied. One of the pixel cells in these devices is connected to a large probing pad on the periphery. All the other pixels in the devices are ganged together to another probing pad. During measurement, the ganged pixels were grounded together, and I-V measurements were taken on the single pixel cell. Our results showed that breakdown occured more frequently for devices with atoll p-stop than with the common p-stop. This is even more so for devices with small pitch. We will modify the separation between the n^+ implant and the p-stop in a future fabrication.

5.2.5 Diamond option

In addition to the baseline silicon-sensor plan, some members of BTeV are participating in R&D into diamond pixel detectors as an option for BTeV. Test results on diamond from the CERN RD42 collaboration indicate that diamond detectors have a useful range of operation up to fluences exceeding 10^{15} n/cm^2. Diamond has excellent thermal conductivity and mechanical properties. These, coupled with the fact that diamond detectors have no leakage current, make diamond detectors a very attractive option for the innermost region where the radiation dosage is very high. On the other hand, this is a technology still under development, and has never been used in a real high-energy physics experiment. There are concerns about the quality of the diamonds, collection efficiencies, thickness of the diamond, large scale production, and cost.

Our simulation shows that there are significant gains in resolution by moving the detectors close to the beam. In our baseline design, we have chosen to place the pixel detector no closer than 6 mm from the beam because of radiation damage to silicon. The use of diamond pixel detectors would enable us to operate the vertex detectors closer to the beam.

We plan to test diamond pixel detectors using the FPIX0 readout chip in the MT test beam during the fixed target run at Fermilab.

5.2.6 Goals of sensor development

Our goal is to have a final specification for the sensors by May 2000. To achieve this goal, we have to do studies of guard rings, p-stop designs, and p-spray devices before and after irradiation. Electrical characteristics of devices before and after irradiation also will be simulated using computer models.

At the same time, we will keep in close contact with the CERN RD42 collaboration to investigate the possibility of using diamond detectors in the innermost area of our pixel system.

5.3 Pixel readout chip

5.3.1 Pixel readout chip development at Fermilab

One of the defining characteristics of BTeV is the plan to use a vertex trigger as the primary trigger for the experiment. This means that the pixel readout ASIC must be capable of reading out all hit information from every $p\overline{p}$ interaction. MCFAST simulations have shown that an $8mm \times 7.2mm$ pixel sensor located $6mm$ from the beamline (corresponding to the innermost pixel readout chip, given the baseline BTeV design and the current readout chip size) will be hit by one or more tracks in approximately one bunch crossing out of four at a luminosity of $2 \times 10^{32} cm^{-2} sec^{-1}$. The number of pixel cells hit by a single track depends on the pixel size and the track angle with respect to the pixel sensor. Given a pixel size of $50\mu m \times 400\mu$m and a sensor thickness of 300μm, our simulations indicate that an average of five pixels will be hit in the innermost readout chip in those crossings in which one or more tracks hit the chip. Therefore, this pixel chip has to sustain an average readout rate of 1.25 pixels per BCO (beam crossing). To account for statistical fluctuations and allow for effects not included in the simulations, the chip must be capable of even higher data transfer rates, and must be able to buffer hit information which can not be immediately read out.

The BTeV pixel readout chip should be optimized for the 132 ns time between crossings planned for the Tevatron collider. It must be radiation hard so that it can be used close to the beamline. As described above, the baseline BTeV design calls for n^+ on n silicon sensors with appropriate guard ring structures for high voltage operation. These sensors provide adequate signals after significant radiation exposure, but also have rather large radiation-damage-induced leakage current. The BTeV pixel readout chip must be able to tolerate this leakage current at least up to 25-50 nA per pixel.

An R&D program has begun at Fermilab whose goal is the design of a pixel readout ASIC for BTeV[24][25]. The program envisions a series of prototype pixel readout chips, each with specific engineering goals. The current expectation is that the final design will be implemented using the radiation hard Honeywell 0.5μm CMOS Silicon-On-Insulator (SOI) process. For this reason, the first prototype devices have been made using relatively inexpensive radiation soft CMOS processes using only features (number of metal and polysilicon layers, for example) shared by the Honeywell SOI process.

Significant progress has been made in the development of a pixel readout ASIC. Two prototype circuits have been fabricated and are being tested. The first chip, FPIX0, was designed in early 1997, and received at Fermilab in September, 1997. It has been extensively tested, both alone and bonded to a sensor [26]. FPIX0 chips bonded to pixel sensors will be tested in the Meson test beam, as described below. The second prototype pixel readout chip, FPIX1, was designed during 1998, and received in December, 1998. This circuit, which contains ~ 970000 transistors, is the largest ASIC ever designed at Fermilab. It is currently being bench tested. Beam tests are planned for late summer, 1999.

5.3.2 FPIX0

FPIX0 has achieved both of its primary design goals. These were: 1) To establish a front-end design appropriate for use at the Tevatron collider; and 2) To verify that deadtimeless operation is possible. Deadtimeless operation requires that the analog and digital sections of the chip be isolated from one another, and that readout signals be isolated from the sensor so they are not coupled back to the amplifier inputs. In the FPIX designs, the metal 3 layer is used to isolate the sensor from the readout chip.

The FPIX0 amplifier consists of two folded cascode stages, AC coupled to one another.

The first stage is a charge amplifier that uses a current controlled feedback circuit [27]. The second stage provides additional gain and is DC coupled to the discriminator. The FPIX0 amplifier is a continuous time amplifier which does not require front-end reset signals. The feedback current controls the return-to-baseline time and also compensates for sensor leakage current. The circuit was designed to completely compensate for leakage current up to ~ 25 nA. Tests of the FPIX0 demonstrate that the circuit works as designed, and in fact currents of 100 nA or more can be tolerated with only minor signal degradation. This is essential for operation in BTeV close to the Tevatron beam, where radiation damage will result in large sensor leakage current (pixel sensors can not be AC coupled to the readout electronics because the required capacitor would be larger than the pixel).

One of the primary goals of our test beam activity is to verify the simulation results on resolution as a function of the number of ADC bits. FPIX0 chips (which include an analog output) bonded to ATLAS sensors will be used for this purpose.

5.3.2.1 Test results

Fluorescence x-rays from a number of metal foils have been used to provide an absolute calibration of an FPIX0 bonded to an ATLAS (Seiko ST1) pixel sensor. Figure 5.15 shows the pulse height spectrum collected using a single FPIX0 pixel amplifier while the sensor was being illuminated with terbium x-rays. The $K_{\alpha 1}$ peak (44.5 keV) is easily identified at 407 mV. Since it is known that a 44.5 keV x-ray creates 12300 mobile electron-hole pairs in fully depleted silicon, the scale for this channel is 30.2 input electrons per mV peak output signal. We have verified the linearity of the FPIX0 amplifier response to small input signals using a variety of characteristic x-rays.

Measurements of amplifier noise and discriminator threshold dispersion have been made for a number of FPIX0 chips, and also for a smaller test chip (Pre-FPIX1) which contains a variety of FPIX0-like amplifiers. Two conclusions have been drawn from these measurements. First, there is a trade-off between dynamic range on the one hand, and low noise and small discriminator threshold dispersion on the other. Second, the cells which are bonded to sensor pixels are only slightly noisier than identical unbonded cells. If all of this noise difference is attributed to the difference in input capacitance, then a SPICE simulation indicates that the total input capacitance of the (Seiko ST1) sensor pixel and bump bond is approximately 180 fF, which is very close to the expected value.

No pickup of the digital activity associated with readout has been detected. With the metal 3 shield grounded, there is no significant coupling through the detector. The capacitance between the metal 3 shield and a sensor pixel has been inferred to be approximately 1.8 aF/μ^2. This capacitance was inferred by disconnecting the shield from its ground, injecting a pulse on the shield, and measuring the output voltage from a single pixel unit cell. Finally, we have measured the pixel-to-pixel cross talk to be less than 2%.

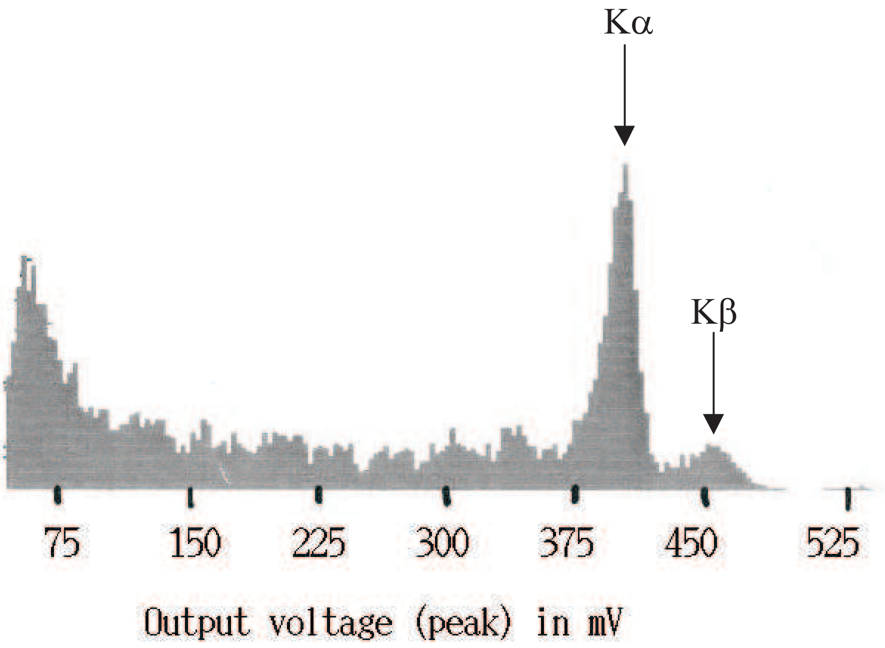

Figure 5.15: Terbium x-ray spectrum recorded by a single FPIX0 channel.

5.3.3 FPIX1

5.3.3.1 Design features and architecture

The FPIX1 readout chip is the first implementation of a new column-based pixel architecture designed to meet the requirements of BTeV. The most stringent requirement is that all pixel hit information from every Tevatron crossing must be digitized and read out so that it may be used to form the primary trigger for the experiment. Simulations indicate that, with a 26.5 MHz readout clock, FPIX1 is capable of reading out an average of more than three pixels per BCO. Relatively straightforward extensions of the FPIX1 architecture should increase the readout bandwidth by a factor of four or more.

In FPIX1, each pixel hit is associated with a six-bit time stamp (the beam crossing number) and the hit information is held in the pixel unit cell until readout. In normal operation for BTeV, the chip itself generates a readout trigger for every beam crossing. The time stamp associated with a hit pixel is held in a register located at the end of the column of pixels containing the hit. All pixels in a given column which are hit in the same 132 ns beam crossing are associated with the same end-of-column timestamp register. Each column in FPIX1 has four timestamp registers.

Figure 5.16 is a photo-micrograph of a single FPIX1 chip. Figure 5.17 is a schematic diagram of the layout. FPIX1 is composed of three building blocks: the pixel unit cell, the end of column logic, and the chip control logic. The active area consists of an array of 160 rows by 18 columns of pixel cells, each 50μm $\times$ 400μm. All "normal" chip I/O is through a double row of pads (shown along the bottom in Figures 5.16 and 5.17). The opposite edge of the chip is used to provide direct access to amplifier and discriminator outputs from one row of pixel cells. These are for diagnostic use during the prototype phase of chip development, and will not exist in the production version of the chip. In addition, one column of pixels is designed to be read out under external control using pads on this “top” edge of the chip.

A block diagram of the FPIX1 pixel unit cell is given in Figure 5.18. The FPIX1 front-end is an optimized version of the FPIX0 front-end described above. The dynamic range of the FPIX1 amplifier is approximately 32000 e^-. FPIX1 was designed with a two bit flash ADC in every pixel cell.

The digital section of the FPIX1 pixel unit cell consists of a command interpreter and a bus controller. Four pairs of lines carry commands from the end-of-column-logic to the pixel unit cells. Each pair of command lines is associated with a particular timestamp register in the end-of-column logic. The commands which control the action of the pixel cells are: “idle,” “reset,” “output,” and “look-for-data.” Commands are presented by the end-of-column logic simultaneously to all pixel cell command interpreters in a column. When a pixel discriminator fires, then if the “look-for-data” command is present on one of the four pairs of command lines, the command interpreter in the hit cell associates the hit with the timestamp register corresponding to the “look- for-data” command. Simultaneously, it alerts the end-of-column logic to the presence of a hit. After the association of a hit pixel with a timestamp register is made, the command interpreter in the hit pixel cell waits for an “output” or “reset” command on the line corresponding to the associated timestamp register, and ignores the other command lines.

In normal operation, the FPIX1 chip control logic generates a readout trigger for every beam crossing after waiting for two crossings to allow hit information to settle. A token passes quickly through columns containing no data associated with the requested crossing number, and stops at the first hit column. Another token is generated by the end of column logic in this hit column, and this token drops down the column through unhit cells until it reaches the first hit pixel. At the next rising readout clock edge, the hit pixel cell loads its data onto the column bus and drives it to the end-of-column logic for one clock cycle. In parallel, the column token is transmitted to the next hit pixel. The time required for the token to pass through unhit columns, and unhit pixel unit cells in a hit column, determines the maximum allowable readout clock frequency. A good deal of effort was spent in the design of a high speed token-passing circuit for FPIX1. The time required to skip an unhit pixel cell has been measured to be $\sim$ 190 ps (greater than 5 GHz skip rate). This allows a 26.5 MHz readout clock to be used with a comfortable safety margin.

5.3.3.2 Preliminary test results

The first measurements of FPIX1 performance are very encouraging. The front-end performance is approximately as expected. Both the amplifier noise and the discriminator threshold rms are $\sim$ 40% smaller than in FPIX0, and acceptable for use in BTeV. The discriminator overdrive required to latch a hit in the proper beam crossing is only $\sim 250e^-$. The two-bit ADCs operate as designed, and all of the readout logic works. An IR drop on the line which

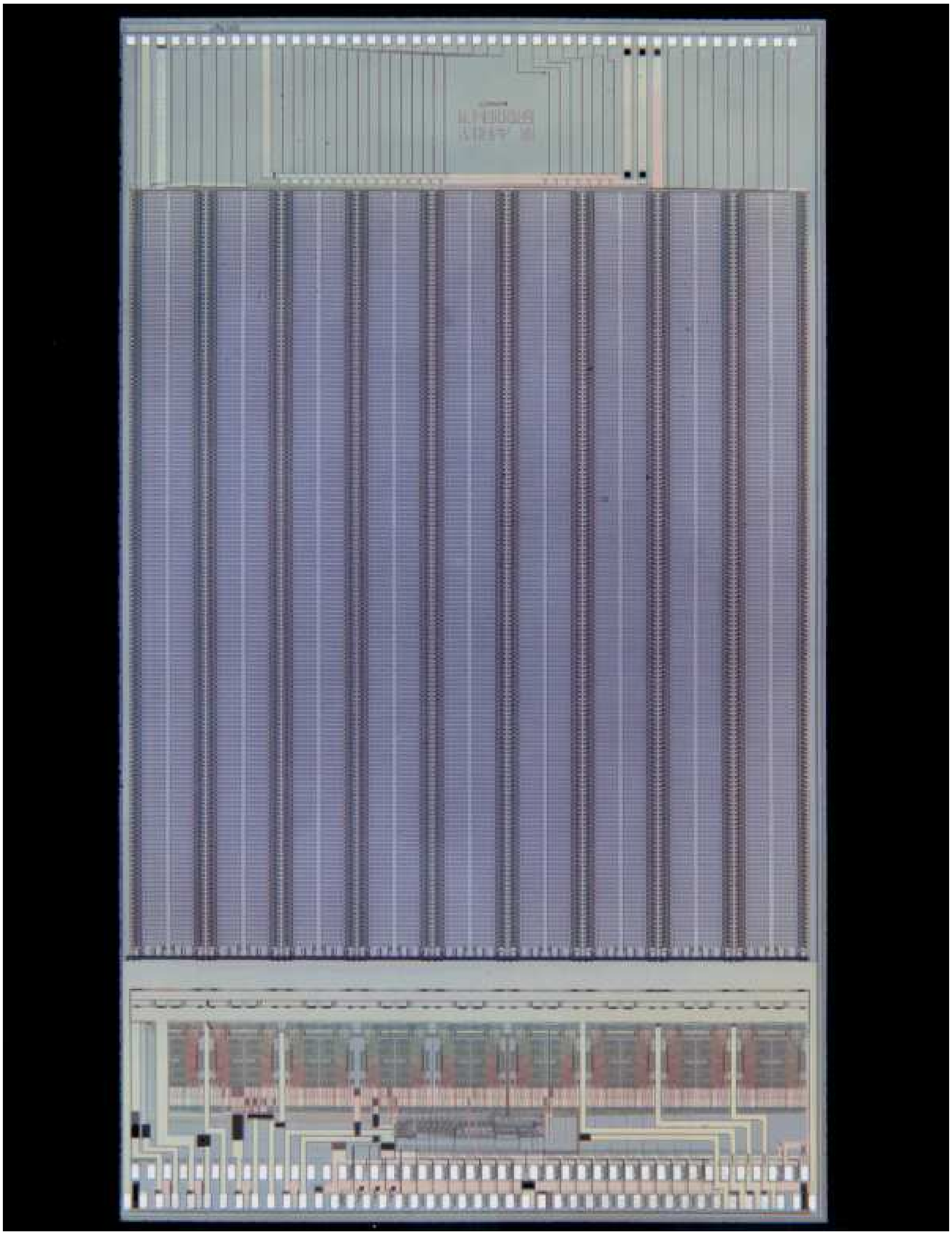

Figure 5.16: Photomicrograph of FPIX1.

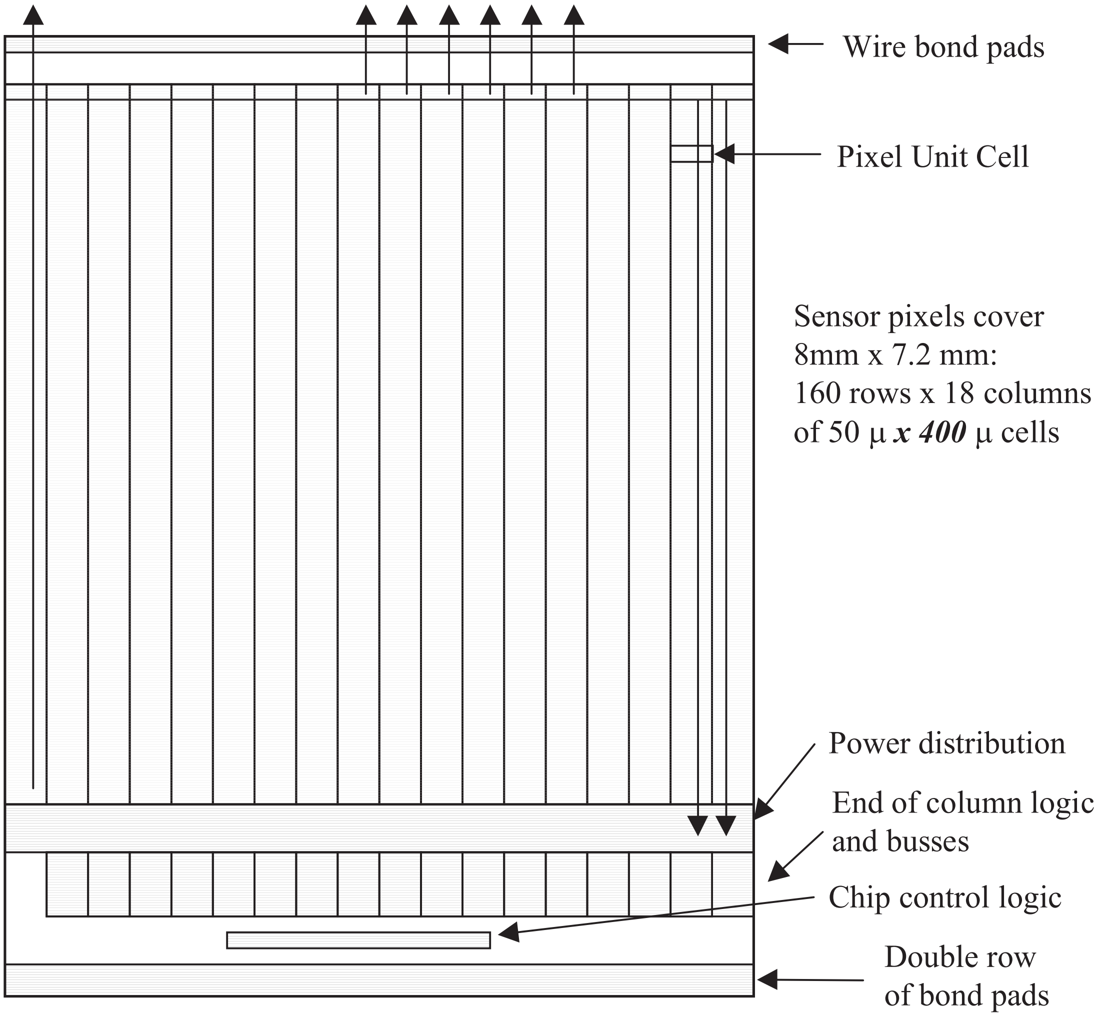

Figure 5.17: FPIX1 Floor Plan.

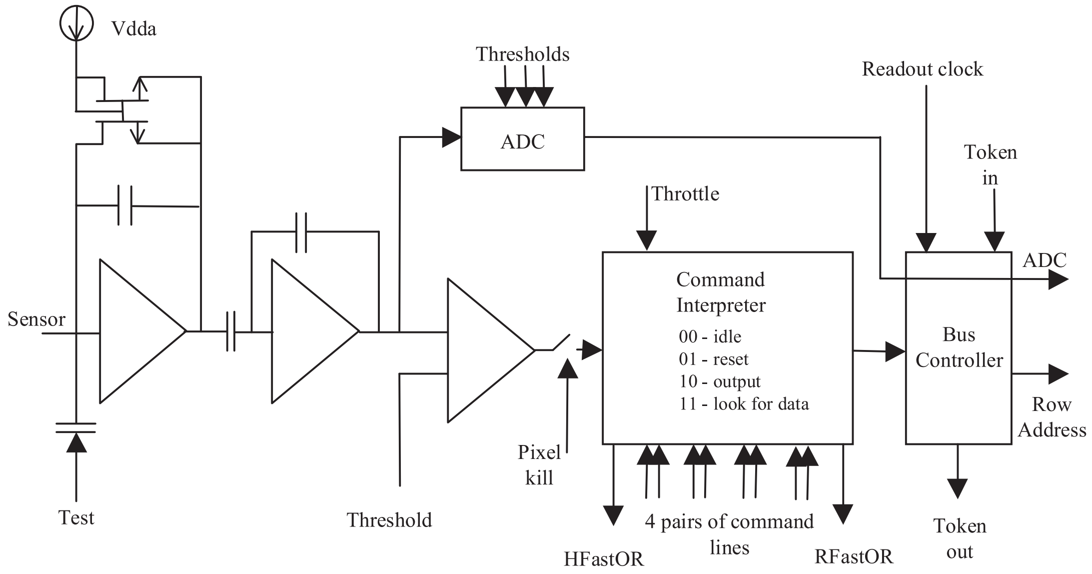

Figure 5.18: The FPIX1 Pixel Unit Cell.

alerts the end-of-column logic to the presence of a hit in the column may mean that only $\sim 125/160$ pixels in each column can be used in the beam test. This error is embarrassing, but completely understood, and trivial to correct in the next FPIX design.

As FPIX1 was designed, simulations were performed using both SPICE and Verilog. SPICE simulations were used in the analog design and also to provide parameters (e.g. time delays) for the Verilog simulations. Layout versus schematic checking was performed both at the cell level and at the full-chip level. The behavior of the entire chip was simulated using Verilog. We are continuing these simulations using pixel hits generated by MCFAST and Verilog models updated with measured FPIX1 parameters. We will rely heavily on Verilog simulations as we decide what features of FPIX1 to modify in the FPIX2 design.

5.3.4 Future plans

FPIX1 was fabricated using the HP 0.5μm CMOS process. This choice was made in order to facilitate the production of a final BTeV pixel readout chip using the radiation hard Honeywell 0.5μm SOI CMOS process. However, recent results from RD-49 at CERN indicate that standard commercial "deep submicron" (0.25μm and below) CMOS processes may be even more radiation hard than military processes such as the Honeywell 0.5μm SOI, provided only that a set of special design rules is followed [29]. An ASIC is currently being designed at Fermilab which contains amplifiers, comparators, and other circuits similar to those required for the front-end of the pixel readout. This chip will be fabricated using a standard commercial 0.25μm CMOS process. Its performance before, during, and after exposure to radiation will be evaluated. Based on this evaluation, we will decide whether to implement the next FPIX chip in HP 0.5μm, or to redirect our efforts towards a deep submicron implementation.

5.4 Bump bonding development

5.4.1 Introduction

The BTeV baseline pixel detector, like all other pixel systems, is based on a design relying on a hybrid approach. With this approach, the readout chip and the sensor array are developed separately, and the detector is constructed by flip-chip mating of the two. This method offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor materials. However, it requires the availability of a highly reliable, reasonably low cost, fine-pitch flip-chip attachment technology.

There are several bonding technologies which may be suitable for this. These include indium bumps, Pb-Sn solder bumps, fluxless solder bumps, and anisotropic conductive films(ACF) or tapes. The technology has to be able to fulfill the following requirements:

- small bump - the typical bump diameter and height for our pixel detector is between $10-12\mu$m.
- fine pitch (50μm)
- high yield - a defect rate of better than 10^{-4} is required.

5.4.2 Prototyping experience

Given the fact that we are mostly dealing with dies (for the readout chip) so far, and that our pitch is extremely fine, we chose to go with indium bumps which possess many attractive features. We have successfully deposited indium bumps on 30 micron pitch for an earlier tests of four hybridized arrays. The low melting point of pure indium, 156°C, allows for cold pressure welding, instead of solder reflow, and low forces (2-3 gram/bump) are used during the bonding process. For small prototype runs, there are only a handful of companies that can provide such services to outside customers. Because of the technical challenges (small die, large aspect ratio, fine pitch), we decided to go to two different vendors. These are Advanced Interconnect Technology (AIT) in Hong Kong, and Boeing North America Inc. in Anaheim. Our preliminary results showed that the failure rate in bump deposition from AIT was better than 2×10^{-4} at 90% C.L. There were a couple of dies with poor bump deposition(bridges or shorts, missing bumps) from the BOEING batch. Ignoring those two bad ones, the failure rate from BOEING was comparable to that of AIT. However, since the beginning of last year, BOEING no longer provides bump-bonding service to outside customers. We did, however, manage to get four pixel detectors using the FPIX0 chip bumped and mated at BOEING before they decided to stop their service. So far, we have fully tested one detector and found out that all the channels have been successfully connected. Fig. 5.19 shows the hit-map of a

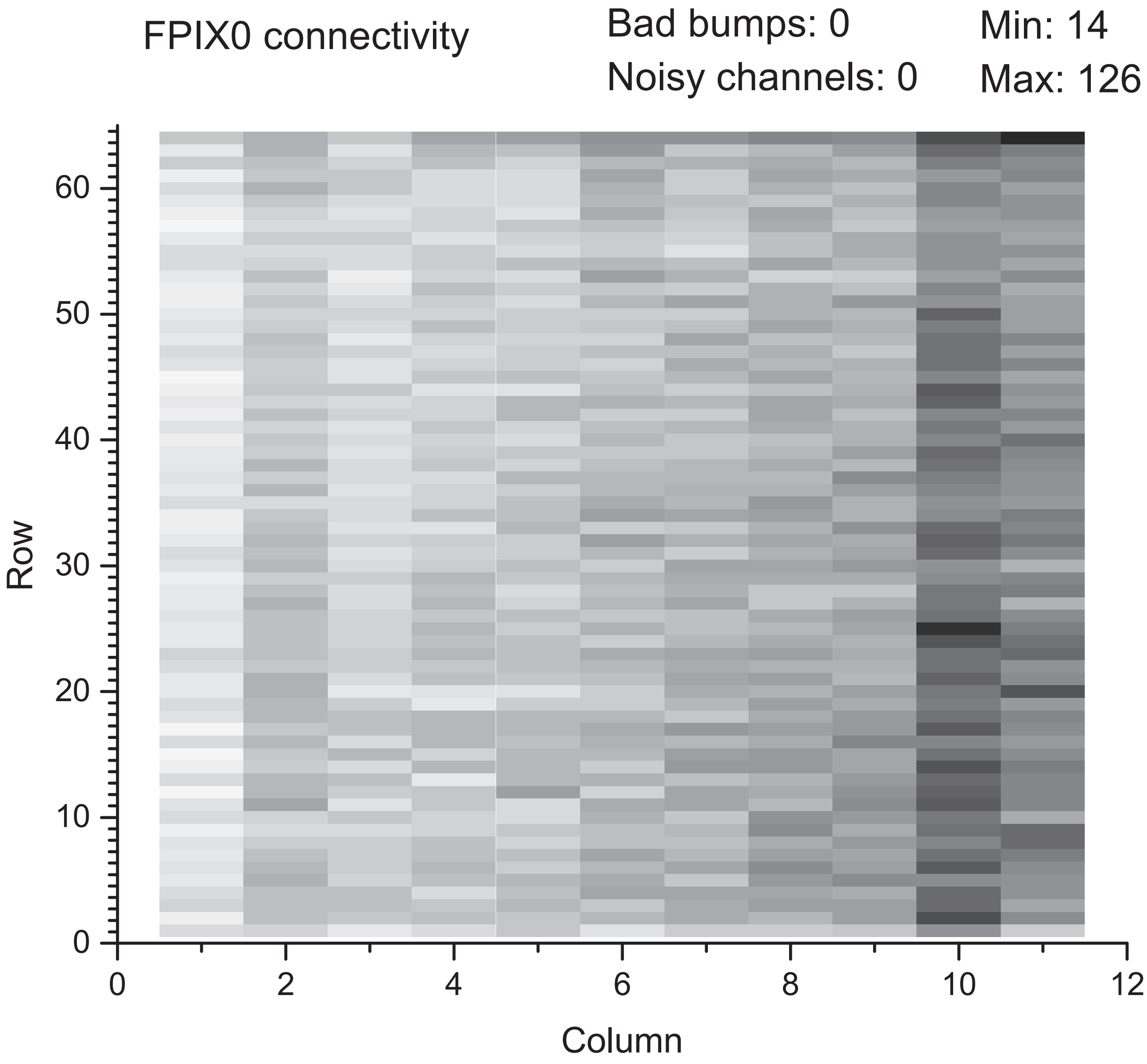

Figure 5.19: Hit map of a bump-bonded FPIX0 pixel detector showing 100% connectivity.

prototype pixel detector using a Sr^{90} source. All the channels were found to work, showing that all the bump bonds were good.

We have also received from AIT four thinned silicon wafers with bumps put on. The wafers were thinned at BNL. Two of the wafers were thinned to 250μm and two to 200μm. They were then sent to AIT where indium bumps were deposited. The pitch in the narrow dimension for the pixels on these wafers was 30μm. Visual inspection under a microscope showed that apart from a few bad or missing bumps on the edge of the wafers, all the bumps were good and fairly uniform. Based on these limited statistics, the failure rate in bump deposition on thin wafers is about the same as for 300μm thick wafers. However, we have not done any tests on flip-chip mating with thinned wafers.

There are lots of companies which can provide flip-chip mating services for large pitch (typically 200μm pitch and 100μm diameter bumps). Our requirements are at the very high end of the technology due to the small bumps, fine pitch, and relative low volume by industrial standards. These rule out high volume companies such as Flip-Chip Technology, Abpac, and Delco.

5.4.3 Large scale study of bump bonding yield

The goals of the large scale bump bonding study are to find a suitable vendor to do reliable and cost-effective bump bonding and to establish a quality control procedure so as to minimize the failure rate. We have established good working relations with industry and institutes working on LHC related projects. We have, and will continue to benefit from, sharing experience and information with LBNL.

Because of our fine pitch and small bumps requirement and that we have been dealing with small readout dies, we have opted to go for indium bumps. However, our recent contacts showed that Pb/Sn solder has been made to work at various places(e.g., IZM in Germany, SII in Japan, and AIT in Hong Kong) for a pitch as fine as 50 μm. Solder bumping is a self-aligning process and is a bit cheaper than indium bumps. However, the process typically involves the use of flux which needs to be removed after flip-chip mating. With small bumps, this may not be easy. Apart from environmental considerations, flux residue will lead to corrosion of the joint. The use of flux-less solder bump is now being pursued by industry. MCNC has a new fluxless, no-clean process called PADS (Plasma Assisted Fluxless Soldering) which has shown considerable success with flip-chip assemblies [34]. This relies on a pretreatment which enables the subsequent solder reflow in inert ambients. The use of this process, however, will pose stringent requirements on the thickness and material of the passivation on the readout and sensor wafers. This needs to be studied. Another concern is that the heavy Pb component in the solder bump may lead to a substantial increase in the electronics single-event upset rate. We plan to study this carefully together with the US-CMS collaboration.

Both pure In and Pb/Sn solder appear to meet our requirements for providing adequate electrical and mechanical bonds at 50 μm pitch. Our task is to start qualifying vendors with facilities to provide such services to outside customers and demonstrate the quality and yield of their bump bonding services by providing bumping and bonding of a large number of dummy pixel detectors. Long term effects on the bump bonding will also be studied. These include mechanical stability, effect of thermal cycles, irradiation, and handling the parts during assembly. The study will be done on different pitches and both technologies (Indium and Pb/Sn) will be tested.

For this purpose, we have designed a dummy assembly module consisting of an upper and a lower array. As much as possible, the two arrays will be close to the size of the real sensor and readout chip that we will have. Each array will have just metallization (Aluminum or gold) which will be covered with passivation with openings for the bump-bond pads and probe pads. The wafers will be made with two pitches, 30μm and 50μm. The upper array mimics the sensor chip and consists of pairs of bump-bond pads connected together. The lower array mimics the readout chip and consists of a large number of bump-bond pads ganged together with traces leading to probing pads on the periphery (Figure 5.20). When the two are mated, one can use an automatic probe station, with the appropriate probe card to test connectivity, and hence determine the presense of bad connections. The probing pads on the periphery are large enough so that they can also be used for wire-bonding. Assembly using these dummy modules can be practiced.

To characterize a vendor, we will send them a number of these dummy wafers. The wafers will be 300μm thick. Depending on the success of these tests, we will send them real sensor wafers and FPIX1 readout wafers so that we can do a real evaluation. We will also do tests on thin wafers. Table 5.3 lists the vendors that we have contacted and have expressed some interests in working with us. Both TRONICS and Rockwell can only handle 4" silicon wafers. This may be a concern for future production runs.

Vendor	*Technology*	*Location*	*Status*
AIT	*Indium* *solder*	*Hong Kong* *Hong Kong/Singapore*	*contract* *pending*
IZM	*Solder*	*Germany*	*SOW sent*
LMCO	*Indium*	*Massachusett*	*SOW sent*
MCNC/Unitef	*solder* *fluxless solder*	*North Carolina* *North Carolina*	*proposal rec'd* *proposal rec'd*
TRONICS	*solder*	*France*	*proposal rec'd*
Rockwell	*Indium*	*California*	*on hold*

Table 5.3: A list of potential vendors that can provide bump bonding services. SOW stands for Statement of Work. Proposal received means that they have already sent in their proposal to our SOW.

Our plan is to select up to four vendors from the list and work together with them. A lot of interaction between us and the companies is needed to understand the possible causes of failures, to rectify them, and to establish a detailed quality control procedure.

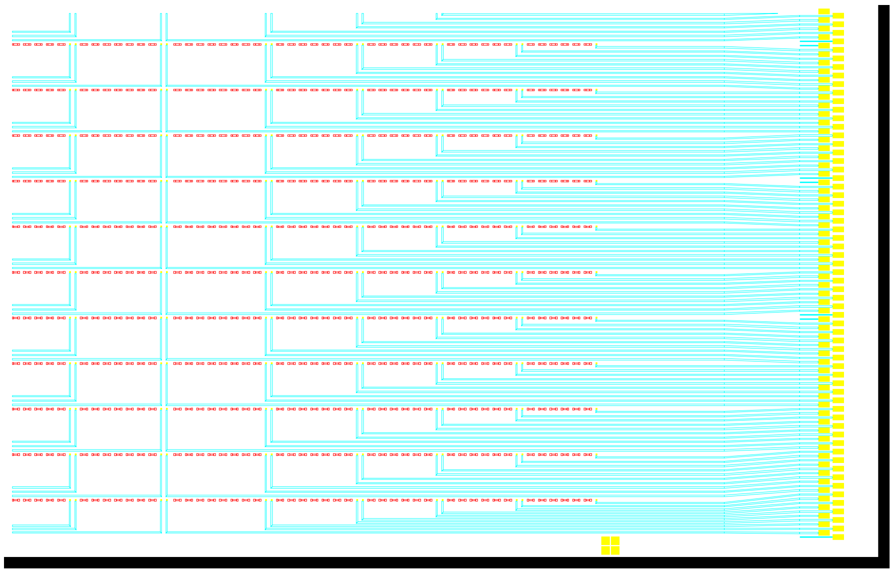

Figure 5.20: Layout of the lower array in the dummy wafer that will be used for large scale bump bonding studies.

5.4.4 Diagnostic tools

To characterize the various vendors and to understand the yield of the process, we need some diagnostic tools. Some of these will also be valuable during the production phase as a means of quality control. Possible tools include:

- optical microscope - Coupled with a precision x-y table, this is a simple and cheap way of detecting defects such as missing bumps, bridges, misplaced bumps, and irregular bump deposition.

- scanning electron microscope - This is useful to measure precisely the bump diameter, height, and placement precision. It also shows the under-bump-metallization.

- wafer profiler system - As a defect inspection tool, the profiler automatically detects bridges, under and oversized bumps, missing and extra bumps, and bump position. Furthermore, the system calculates bump height, diameter, volume, as well as coplanarity.

- acoustic imaging system - Using high frequency ultrasound, high resolution images can be produced to specific levels within a flip-chip mated device.

- X-ray imager - Using a high resolution micro-focus X-ray tube, a highly magnified X-ray image of the flip-chip mated device will show the presence of poorly connected or missing joints between the sensor and the readout chip.

We are working together with local industries and the bump bonding companies to determine which tool will provide the most useful information.

5.5 Data output and control

The input and output links to the pixel planes can be categorized based on the data bandwidth. The highest bandwidth corresponds to the pixel hits generated during the normal operation of the pixel detectors and collected by the pixel detector amplifiers and discriminator chips. However, these chips must be initialized, controlled and monitored by the DAQ system. This latter information will travel to and from the pixel detector planes at a considerably slower speed.

The electronics dedicated to the functions of receiving and transmitting data will be located on the corners of each pixel detector plane. This circuitry must be in charge of adapting electrical protocols, data formats, and data speeds to interface with the pixel detector chips. This electronics, called Data In and Out (DIO) is severely constrained by factors such us physical space, power dissipation, radiation dosage, EMI noise, mass, and outgassing.

The expected occupancy of the pixel detector planes, at the maximum luminosity BTeV intends to run ($2 \times 10^{32} cm^{-2} sec^{-1}$), can generate as much as 16 Gb/s of digitized data. The initialization, control and supervision data will not exceed 160Mb/s for each half-plane of the pixel detector system.

Figure 5.21 shows a block diagram of the proposed scheme. The two links on the upper left corner receive the 53MHz clock and the initialization and control data for the pixel readout chips. The links on the bottom right of the block diagram transmit the pixel hit data to the DAQ and Trigger Processor. These links will also be used to read out the configuration and status information of the pixel readout chip for supervision purposes.

The main building blocks of the DIO electronics are the optical receiver, the data-concentrator and the optical transmitter chips. The optical receiver is an interface chip between the serial optical channels and the pixel readout chips. At the physical level, it must detect the current generated by the pixel detector and generate the CMOS and LVDS signals to interface with the pixel readout chips. Furthermore, it must provide a readout clock with very low jitter (< 150ps). At the logical level, it must decode serial information into initialization and control commands for the pixel readout chips, and decode the BCO clock.

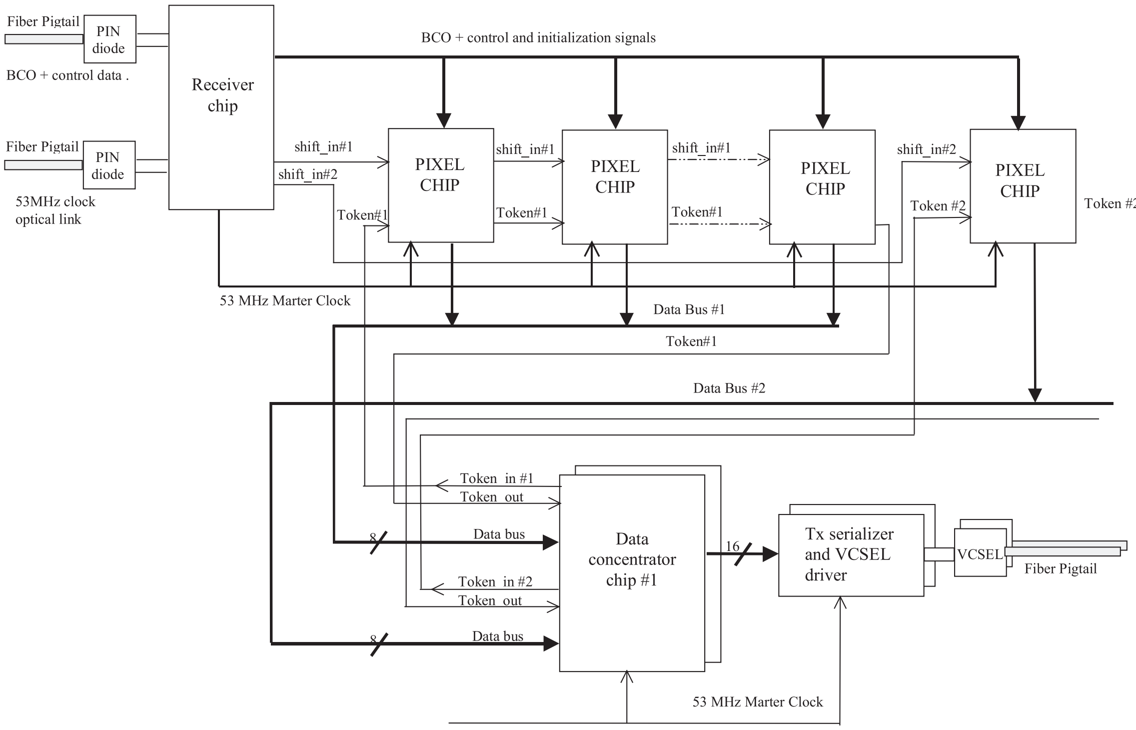

Figure 5.21: Block diagram of the proposed data I/O scheme.

The data-concentrator chip will group the data output of pixel readout chips. Its main function is to control the data flow from a pixel module, manage the token bit passing, equalize the data stream from the pixel chips into a serializer and optical transmitter. The data equalization is needed due to the fact that the hit and data rate is different in every pixel chip according with its proximity to the beam. The pixel chips closest to the beam will generate as much as 400 Mb/s of data and may need a dedicated link to the data-concentrator chip. Other chips, which do not generate as much data, will share a common bus and will be readout following a token passing algorithm. The data-concentrator must keep the token passing algorithm consistency and interface to the serializer and optical transmitter.

The optical receiver and the data-concentrator chips will be designed at Fermilab. The data I/O of the pixel detector planes will be carried through fiber-optic cables. Current studies show that these cables present the best solution to meet the requirements of mass, EMI noise, radiation, power consumption, and physical space. Since other experiments in the HEP community are also designing optical links for pixel detectors and calorimeters, we will benefit by collaborating with other groups working in this area. The following new technologies are currently under study:

- Vertical Cavity Surface Emission Lasers (VCSELs): Allow gigabits of data to be transmitted several hundreds of meters with few mW of optical power. VCSELs have been proven to be very radiation tolerant [30].

- Step Index Pure Silica Fibers: Accept high levels of radiation without increasing attenuation more than a small percentage [31]. Other graded index fibers are also under study. They are not as tolerant as the pure silica core, but they are less costly. Radiation tests will be performed to determine the level of acceptability.

- Custom ceramic and silicon packages: Very small custom designed packages for VCSEL and PIN diodes, and fiber-optic pigtails may allow optimizing for size, along with meeting the requirements of mass budget and radiation tolerance [32].

The fast data output links must deliver up to 16 Gb/s in every half-plane. We are researching the convenience of fast serial links, about 1 Gb/s, versus slower multifiber parallel links. Fast serial links are harder to design, but will reduce the number of fiber channels. No commercial devices exist which can accomplish the task of interfacing to the pixel chips, serializing the data, and transmitting over a fiber optic channel, and meet the pixel detector requirements. Most of the commercial devices are inappropriate for radiation environments. Furthermore, none of the commercial gigabit-speed data serializers meet the power budget. Among the possible alternatives, one of the most attractive is a CHFET-GaAs serializer being designed for the CMS experiment at CERN. We have already started to collaborate with the chip designer to meet BTeV specifications and to support testing at Fermilab. The protocol of this chip will be compatible with the so-called G-Link receiver at a frequency of 1.2 Gb/s, and its power consumption is less than 100 mW [33].

A second possibility is a prototype chip being designed by an R&D section of Honeywell. It codifies four channels of 16 bit words into 3 fiber links. Each link has two fibers for data and a third for clock. The chip is being implemented in a 0.25μm CMOS process. This is not a radiation hard process by design. However, some 0.25μm CMOS processes have proven to be very radiation resistant [29], which may possibly exceed the required levels. Some research groups at the RD47 collaboration at CERN are currently looking into this problem.

The optical components will require a special package. The package must be of low material, non-magnetic, must not outgas and be as small as possible. Furthermore, it must couple the VCSEL or PIN efficiently to the fiber. The fiber must be radiation tolerant as well. Figure 5.22 shows a possible solution where a ceramic substrate is used to host the VCSELs, PINs and fiber pigtails. This kind of substrate has ceramic or silicon alignment blocks, strain reliefs, and wire bond pad to interface to the transmiitter and receiver chips. The fiber pigtails can be ribbonized some distance outside the detector plane and connected to a standard fiber ribbon cable. This connection can be performed either by splicing or through a small-form-factor fiber ribbon connector.

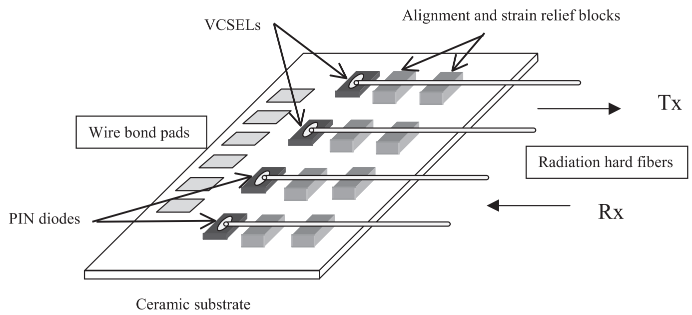

Figure 5.22: Sketch of a possible arrangement of the optical components.

5.6 Pixel Readout and Quadrant Processors

The data read out from the pixel detectors are transmitted through fiber-optic cables to Quadrant Processors. From the Quadrant Processors the data will be delivered to the pixel trigger system and the DAQ system.

There are several factors that impact the number of fiber optic links needed to transmit the data from the pixel detector to the Quadrant Processors: pixel hit and noise rate, forms of data compression of the pixel data, maximum optical-link data rate, and safety margin on the data transmission bandwidth.

The pixel detector will be used for the lowest level trigger, and all the data it generates, whether noise or actual hits, has to be transmitted to the Quadrant Processor. For this reason, it is important to include additional bandwidth.

A simple form of data compression can be achieved directly by the pixel chip, thereby decreasing the data rate. Data alignment by timestamp implemented in FPIX1 already achieves an initial degree of data compression. During readout, the timestamp has to be transmitted just once for all the hits that occurred simultaneously. In the next FPIX generation, we hope to implement what we have named "group" reading. The concept is that instead of reading a column by individually reading each pixel cell, we will read groups of consecutive pixel cells. So, we will not have pixel row address, but actually pixel group address, and the row position of several pixels can be uniquely identified with just one row address. Simulations have shown a data compression by a factor of 2.36 with respect to a pixel by pixel readout if we use a group size composed of four pixels.

To estimate the data that a pixel plane generates, we used the data compression scheme which includes alignment by timestamp and group reading formed by the data of four pixel cells. The readout data is composed of time stamp, group row and column address and two more bytes of pulse heights, each byte with two pulse heights. The pixel size is 50x400 μm^2. Other assumptions used in the simulation were:

1 . There are no noise hits

2 . Charge carriers: electrons

3 . Threshold: 2000 electrons

4 . Magnetic field of 1.6 T

5 . Minimum bias events with two interactions per 132 ns bunch crossing.

With these assumptions, we obtained a data rate for a pixel plane half of 2.5 GBits/s. We will now assume that the data rate for the fiber optic cables is 1.06 GBits/s, and we can now estimate the number of fiber-optic cables required per half plane. Assuming a safety margin of four, we obtain ten fiber-optic data links per half, or five per quadrant.

The Quadrant Processors will have inputs from three groups of five fiber-optic cables coming from the quadrant. These quadrants are the three adjacent quadrants that form a triplet. There will be a total of 124 Quadrant Processors. The main functions of the Quadrant Processors are:

- Sort the data from the pixel detector by time stamp
- Store the data from the pixel detector in its internal buffers until a decision from the Global Trigger
- Find the center of mass of the pixel hits
- Calculate the minivectors from the triplet and send the data to the Track processor
- After a decision from the Global Trigger, if the event was accepted, deliver the data to the DAQ. Otherwise, just discard the event and clear the event buffer.

5.7 Assembly issues

5.7.1 Introduction

The assembly design for the BTeV pixel detector system is dominated by the need to keep the amount of material to a minimum. This requirement is motivated by the adverse effects of multiple coulomb scattering on the achievable spatial and mass resolution. The former parameter is the most critical, since it influences many elements in the final capability of BTeV: separation of decay vertices from interaction vertices, trigger efficiency and enrichment, signal to background levels, proper time resolution, and sensitivity to multiple interactions per crossing. The mass resolution is also important, but mostly influences just the signal to background quality of BTeV data.

Counter to the need to keep materials at a minimum are the need for reproducible, stable position-determining supports, the need to remove significant amounts of heat directly from the active sensor areas, the need to move the detectors back from the interaction region during injection and machine-study periods, and the need to reposition the detectors reliably and accurately for physics data-taking.

In addition to these design criteria, we have to take into account that the pixel readout chips are limited in size, and the final detector assembly must be made as a matrix of communicating, overlapping pieces. The deadspace and/or gaps between materials also need to be minimized to maintain good efficiency for multiparticle charm and, especially, beauty decay modes of interest.

5.7.2 Interconnections

In principle, each half of a pixel plane could be made from a monolithic sensor with a single large readout device bump bonded to it for signal processing. In practice, this concept cannot be used for many reasons. The size of readout chips cannot be arbitrarily large due to the reticle sizes which are repeated to pattern a full wafer. In any event, yields on sensors and readout devices are such that the cost of making pieces so large would be more than prohibitive. Furthermore, the radiation dose varies dramatically from the near-beam region to the edge of each plane (approximately as the distance to the power 1.7 according to experience at CDF). Thus, various regions of sensor need different bias voltages to achieve depletion (as required for sensitivity), and the local breakdown voltages may also vary with radiation dose. Thus, we are necessarily drawn to a matrix of devices and their interconnections.

Current FPIX1 prototypes have sensitive areas of up to 7.4 by 8.0 mm^2. There is additional area on one edge for control and I/O circuitry, and for wire-bond pads. We may be able to increase the readout chip size somewhat, but the basic final element is not going to be much different from what we have now. We do plan to make many of the readout chips double size (back-to-back) and use larger sensors with multiple readout chips in the final detector. This can reduce the complexity of the interconnection scheme to a certain extent.

Nevertheless, each chip will have a full set of pads for interconnection, and the density of control and readout lines remains very high.

In order to gain experience on the technical issues, we are making a five-readout-chip sub-assembly with flexible cable interconnections. This will test industrial capability and allow us to get some design experience in this area.

Fallback options include the more ambitious, and technically challenging solution using traces on the sensor with bump bonds in place of wire bonds for readout-chip-to-control and output-line connection. This technology, referred to as MCM-D technology, is being pursued as an option by the ATLAS collaboration [35].

5.7.2.1 Pixel Plane High Density Circuitry Interconnect

The pixel detector design is severely bounded by several constraints which reflects on the choices of high density cables and pixel plane circuitry interconnect. Some of these constraints are mass, outgassing, distribution of the high voltage for detector bias, radiation exposure, reliability, and cost.

In a pixel detector, the readout chips are interconnected and the output signals are routed to the edges of the pixel planes. There, the output signals are wire bonded to the fiber optics data serializer integrated circuit for data readout.

In this application, the circuit density of the pixel module circuit interconnect is highly associated with the readout speed of the pixel chip. All data generated inside the pixel chip has to be readout for the lowest level trigger decision. In order to accommodate reasonable readout throughput, several readout buses will have to routed from the pixel chips to the data serializers. Based on the space available for routing it is easy to recognize that very high density circuits need to be employed.

We are presently researching the usage of low-mass flex-circuit interconnect. A preliminary analysis and consulting with vendors strongly suggest that this approach should effectively meet the constraints already outlined. For example, Kapton, one of the polyimide dielectrics used for flex-circuit manufacturing supports as much as 118 KV/mm, which is very good for the high voltage distribution of the detector bias. Other advantages include low mass (the radiation length X_o of Kapton is 286 mm), reasonable cost, radiation tolerance, etc.

We have researched a number of flex-circuit manufacturers and decided to work in conjunction with Fujitsu Computer Package Technologies, a division of Fujitsu, on the design, characterization and production of very high density flex-circuits for the pixel-plane interconnect. Fujitsu's nominal design rules include 25μm hole diameter and 20μm line width and spacing in four or more metal layers which represents the state of the art in this technology.

The present proposal for the interconnect is to glue flex-circuits on the top of the pixel-plane substrate, possibly a carbon-fiber plate, which will hold the detector and associated electronics. A similar approach is being pursued by D0 for the silicon detector hybrids and in the implementation of the majority of the pixel plane interconnect for ATLAS [36]. We estimate that the following four layers of flex-circuit would suffice:

- two layers for signal interconnects,
- one more layer for power and other signals and
- one layer for the ground plane.

These layers are quite thin and can be kept within 5μm of copper thickness. However, substantial mass can be saved if we can implement a three layer circuit, two with signals and power and the third, a ground plane made of aluminum. We will investigate the possibility of depositing a thin aluminum layer on the top of the carbon fiber substrate, use this layer as the ground plane, and laminate and interconnect the flex-circuit directly to this substrate. We are also researching vendors that could manufacture aluminum-on-polyimide flex-circuits.

As our first attempt to build a pixel module, we are presently laying out a five-chip pixel module using the FPIX1 readout chip. Figure 5.23 shows the progress on the layout. The wire bonding pads of three FPIX1 chips are already interconnected in this layout. These chips will be bump bonded to a detector and wired bonded to a high density flex-circuit interconnect. Both the chips and the circuit will be glued to a G10 board. The characteristics of this circuit interconnect will be the following:

- Metal layers: 5μm thick Cu, with 20μm line and space design rules. The first metal layer is capped with 2μm of Ni, and 1μm for wire-bondable gold.
- Film: 50μm thick Upilex SGA (which is comparable to Kapton)
- Film via: 25μm via on 108μm capture pad.
- Lamination: 50μm epoxy
- Z-vias: 200μm via on 350μm capture pad. Via filled with $SnSb_5$ solder.
- Size: 27mm x 54mm x 0.2mm

We intend to test this pixel module for several important performance characteristics: noise, threshold dispersion and crosstalk. Specifically for the flex-circuit itself, we intend to measure the electrical and mechanical performance [36, 37] and the effect of radiation, thermal cycle, and outgassing in vaccum.

Future research for the pixel plane interconnect will include technologies like multi-chip-module interconnect type D (MCM-D) and silicon (or possibly diamond) module hybrid to allow greater use of bump bonding and reduce the number of wire bonds. However, important issues such as high voltage distribution need to be carefully considered.

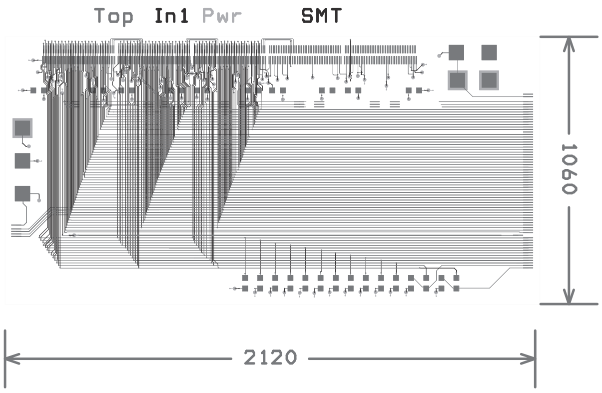

Figure 5.23: Schematic layout of the High Density interconnect prototype. Units are given in mils (0.001 inch).

5.7.3 Mechanical and cooling Issues

The mechanical design is driven by the goal of minimizing the material needed to achieve a satisfactory solution. Carbon-carbon, beryllium and CVD diamond structures appear most suited. We are focusing on plates attached to both sides of cooling pipes. The plates would only be required in the region where they support the pixel devices, with enough periphery to support control chips and pixel-plane-output cables. Rigid support to the outside world can, thus, be limited to a minimum, say the corners of the half-planes.

We will operate with a thermal budget of 40 microwatts per pixel, and doing the engineering as if all the sensors would be placed on the two sides of the above sandwich structure. Furthermore, the sensors will have to be operated at around -10° C and the temperature for each half-plane have to be maintained uniformly to within $\pm 1^\circ$ C. We plan to hire Energy Science Laboratories Inc. (ESLI), San Diego, to perform part of the research work for the development of the mechanics and cooling for a pixel detector plane. This contract will be divided in two phases. The first phase is the theoretical study and simulation of different options for the pixel plane mechanics and cooling, while the second phase is the actual implementation of a prototype of the most promising proposal.

Probably the most important item in this interaction will be the communication between ELSI and Fermilab. Since this is an investigative project and it may have unexpected results, we need to keep evaluating and assessing other promising solutions.

This investigation should answer questions about the ability of different substrates and cooling structures to remove heat from integrated circuits attached to their surface. Also, the mechanical stability of the structure is important for the performance. Two basic approaches are to be considered during this design study:

a) a plate that conducts the heat from the integrated circuits to one or more edges that are attached to a cold sink,

b) a plate that has the cooling channels embedded.

Several different schemes can be envisioned for the second option, such as fluid in pipes between plates, spacers with fluid flow "everywhere" inside, and "fuzzy" carbon spacer with fluid everywhere. Figure 5.24 shows the assembly of pixel plane with pipes between plates.

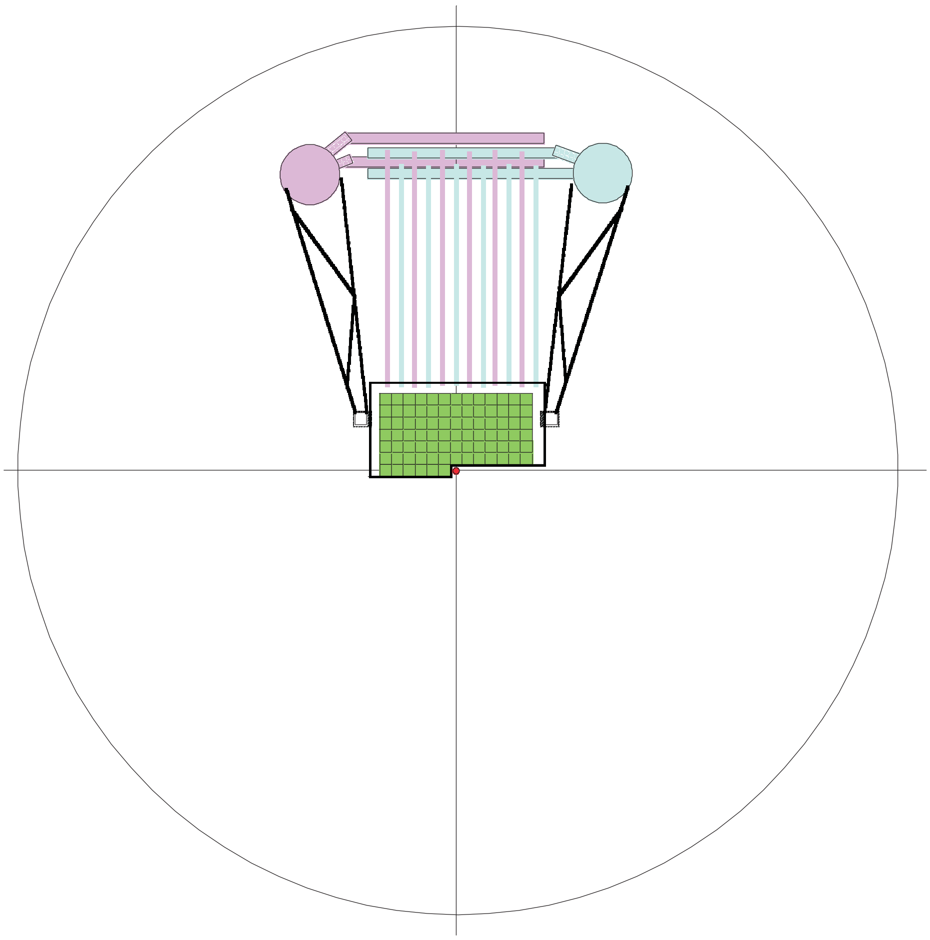

Figure 5.24: Schematic drawing of the pixel plane with cooling channels between the plates

A report from ESLI for the first phase will include the estimated performance of cooling systems and design recommendations, judgements on the feasibility of the economical construction of each option, estimates of the pressure drop of the cooling fluid, heat transfer properties, stiffness, vibration modes, reliability of piping, and temperature profiles. From these, the best solution will be picked.

In the second phase, a prototype of the best solution will be constructed. This model does not need to be a full working unit. However, it will contain enough of the features of the proposed design that it can be tested and compared to simulations.

5.7.4 RF shielding issues

The pixel detector will be installed inside the beam pipe enclosure in the C0 interaction region. The inside of the beam pipe is, in several respects, an aggressive environment for operation of a large, sophisticated detector. We would like to carry out a series of tests both in the laboratory as well as in the Tevatron to study the rf pickup and the shielding that will be required. Our objective with these tests is to investigate the electro- and magnetic (EM) interaction of the Tevatron beam with pixel detectors and associated electronics. When the beam passes close to the pixel detectors and electronics, it generates the equivalent of an electromagnetic pulse which can induce noise and cause other problems in the electronics. Shielding is required to protect the electronics from this pickup. This shielding has traditionally been a metallic skin and adds to the material budget. We are pursuing two kinds of tests, one in a simulator of the Tevatron beam in a laboratory set-up, the other inside the Tevatron itself. We feel that these tests will give us very important insights and will help us to generate guidelines for the design and shielding of the pixel system.

5.7.4.1 Beam simulator

An apparatus has been built to simulate the rf environment of the Tevatron. The basic structure of the test stand is a 5' long cylindrical coaxial pipe made out of stainless steel. It will be used to simulate the electromagnetic field from a bunch of beam particles. The electronics to be tested will be inserted through a slot in the outer conductor. An rf amplifier is used to generate the required current, estimated to be about 8.4Amp. Along with the beam simulator, we have constructed a computer driven test circuit which will feed a controlled bit pattern across a variety of signal paths inside the simulator apparatus. We also anticipate testing various shielding techniques. Our goal is to determine the level of rf pickup in the test circuit and to determine which signal path designs and shielding configurations minimize noise while keeping material use at a minimum. The results of these tests will then be applied to produce a prototype rf shield (if needed) to be tested in the C0 interaction region.

5.7.4.2 Roman Pot Tests for BTeV

We plan to install an existing Roman Pot and castle from E811 into the Tevatron. The pot will make it easy for us to insert various test devices into the region of the beam and make the desired measurements. We will make measurements with pixel detectors and chips placed closed to the beam, and study methods to decrease the EM interference of the beam on the electronics. Our current plans are for a two-year investigation. This will start with simple devices to make EM measurements. Each test will build on the previous tests. The goal is to construct sophisticated electronic test devices with active circuitry similar to whar we could use in the real detector. We hope to learn how to construct a small test pixel detector and take data from it.

The following topics will be investigated:

- layout issues and line terminations;

- rf shielding: its shape, thickness, material, grounding, and support;
- power supplies: their design, location and distribution

Theoretical analysis of the susceptibility of layout traces and transmission lines will be conducted as a first stage of design, to evaluate electromagnetic compatibility rules between the detector and the surrounding media. In such an analysis, it is very difficult to consider all the variables affecting the detector design. Physical prototypes of both general and critical parts of the detector will help to understand the final EM susceptibility of the detector.

We envision two options for the location of the power supplies: outside and inside the enclosure. The first option simplifies the design and procurement of power supplies, but imposes restriction on the distribution cables. The cables can act as EM pick-up elements conducting noise into the detector or generating conductive paths between the different layers of the detector. In these tests we will be able to analyze the performance of this topology, the level of filtering and shielding, and the input-output isolation of the power supplies. Note that the addition of filtering and shielding may require too much mass for the experiment.

The second option imposes more challenges due to the need of locating DC-DC converters near the detector to break conductive paths and decrease the EM pick-up. The pixel detector will be subject to strong magnetic field, which does not allow any magnetic material in the design of such converters. Research will be conducted to evaluate the option of using DC-DC converters based on piezoelectric ceramic transformers [38, 39] and the use of high frequency air core transformers.

5.7.5 Material budget

Table 5.4 summarizes our current understanding of the material budget for one single pixel plane. Each pixel plane will consist of a number of modules. Each module may consist of 4 to 7 readout chips. Figure 5.25 illustrates the way we envisage each plane will be assembled. To account for non-sensitive area in each pixel sensor required for guard rings and scribe edge, the table assumes a 25% overlap of modules on opposite sides of the substrate (this overlap is not shown in the figure). Our baseline design calls for a 5 mm thick Be substrate with integrated cooling channels.

5.7.6 Outlook

Between the time of this PTDR and a full TDR, we anticipate having results from the various prototypes and the engineering studies described above. These will be used to develop engineering calculations and assembly drawings of an actual BTeV pixel detector - optimized for minimum material and stability of positioning. We do anticipate final alignment using charged particles from real physics events for each run (each repositioning of the pixel half-planes), including whatever is needed to make the trigger work effectively.

$Item$	$Thickness(mm)$	$X_0(mm)$	$X/X_0(\%)$
$Sensor$	0.25	93.6	0.30
$Readout\ chip$	0.15	93.6	0.20
$Bumps\ and\ wire\ bond$	0.02	10.0	0.004
HDI	0.224	284	0.08
$Components\ on\ HDI$			0.04
$Glue$			0.02
$Coolant(water/alcohol)$	0.35	40	0.02
$Substrate(Be)$	0.5	353	0.14
$Total$			0.80

Table 5.4: Material budget of a BTeV Pixel plane. This assumes that we can build a pixel plane using only one substrate. Within a plane, we assume that there is a 25% overlap in sensor or readout chip, that the HDI has 100% coverage and that the cooling fluid and cooling channel covers 20% of the substrate. Each HDI has 4 layers with each layer consisting of 50μm kapton and 6μm of Cu.

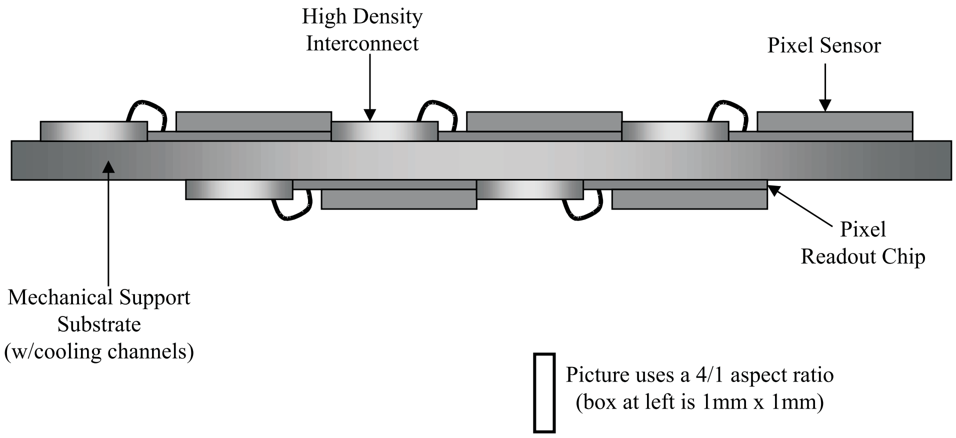

Figure 5.25: Schematic of the assembly of a pixel plane.

5.8 Pixel Beam Test

Beam tests of prototype pixel detectors will take place during the 1999 fixed target run. During this six month period it is planned to test silicon sensors bonded to both FPIX0 and FPIX1 readout chips and a diamond sensor bonded to an FPIX0 chip.

5.8.1 Goals

FPIX0

- To measure the efficiency, charge sharing and resolution as a function angle of incidence, number of ADC bits, and readout threshold. The effect of magnetic field will also be studied.

FPIX1

- To test the fast readout in a high intensity beam.
- To study the resolution as a function angle of incidence, threshold, and different sensor designs.

Diamond Sensor

- To determine whether diamond pixel detectors bonded to FPIX0 chips provide good efficiency, resolution, uniformity, and signal to noise.

5.8.2 Test Stand

The test stand is shown in Fig. 5.26. The central aluminum box at the bottom of the figure has slots for mounting pixel test boards at several different angles. Two triplets of silicon strip detectors form a telescope for tracking the beam particles.

5.8.3 Silicon Telescope

There are six planes of 20 μm pitch silicon strip detectors which are read out with SVX2b chips. A VME based data acquisition system has been adapted from a CDF test stand. It consists of an SGI workstation, a VME CPU, a Silicon Test Acquisition and Readout board (STAR), a Test Fiber Interface board (TFIB), and a Test Port Card (TPC). The STAR has 3 data buffers which can accept data from the SVX2b chips via the TPC. Simulations indicate that we should be able to project track locations at the pixel detector with 4-5 μm precision.

5.8.4 Pixel Readout Board

The pixel readout has been designed to be integrated with the existing SVX2b readout. An RS485 VME interface board is used to send control signals to the pixel readout chip via a pixel readout board. The pixel readout board is physically separated into two boards - an inner board on which is mounted the pixel sensor bonded to the readout chip, an 8-bit flash ADC and power supplies, and an outer board which has all the readout control components. The outer board can accept a trigger either via a NIM or ECL input or through the RS485 cable. After receiving a trigger, the data is read out into one of the STAR buffers. The same outer board can be used for either FPIX0 or an FPIX1 chip. The inner board will be different for each readout chip. For example, the FPIX0 board has a flash ADC whereas the FPIX1 chip itself has a 2-bit ADC in each pixel.

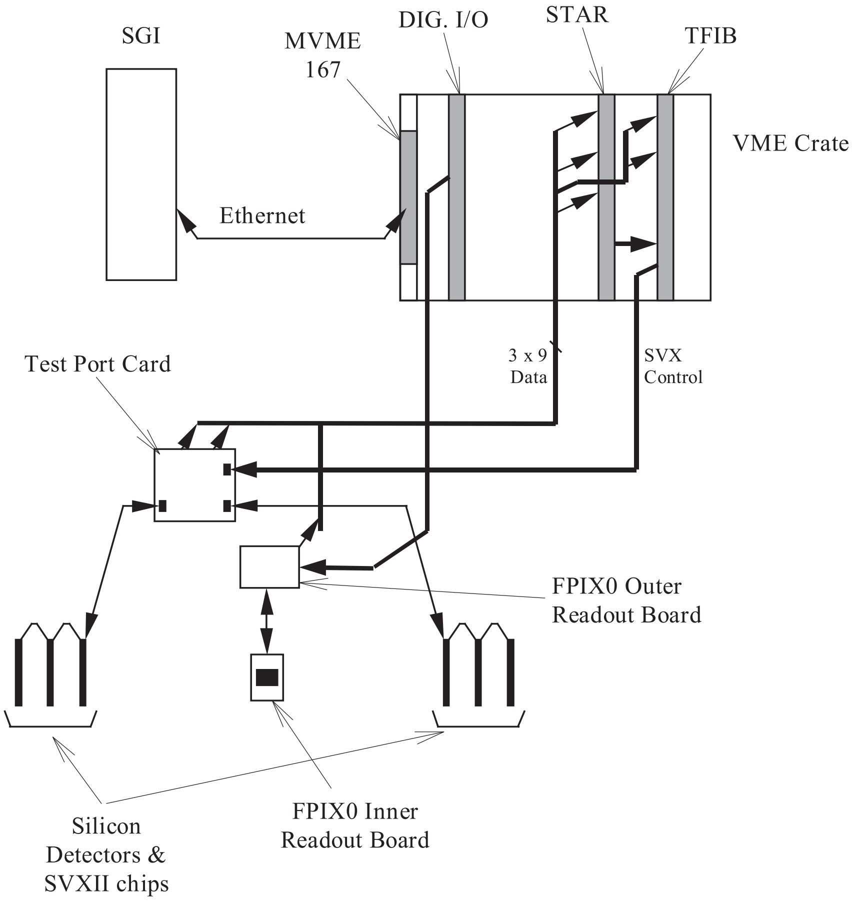

Figure 5.26: Test Stand for Pixel Beam Test.

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