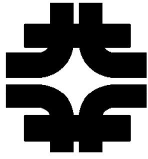

Fermi National Accelerator Laboratory

D-Zero Detector Central Fiber Tracker (CFT) Axial Project Readout Electronics

D0 Central Tracker Trigger (CTT) Mixer System Backplane Description & Power Distribution Specification

Date: July 4, 2000
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1 Introduction

This document describes the mixer system backplane. The mixer system is part of the readout electronics of the D-Zero detector Central Fiber Tracker (CFT) at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page:
http://www.fnal.gov/

More information on the D0 Detector is available on:
http://www-d0.fnal.gov/

The designers welcome suggestions and corrections [Ref. 4], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page:
http://www-ese.fnal.gov/

More information and documentation on the Mixer Project are available on:
http://www-ese.fnal.gov/D0_CTT_MIXER/

2 Overview

The mixer system [Ref 4] consists of a 21 slots subrack with a custom backplane. Slot 1 is occupied by a custom subrack controller, slot 2 to slot 21 host twenty mixer boards. The mixer system is partitioned in five subsystems of four boards each. The mixer system custom backplane was developed as an interconnect and power distribution bus for the mixer board set. It resembles the 6U VME J1/J2 backplane form, but does not necessarily adhere to VME backplane specifications [Ref. 2].

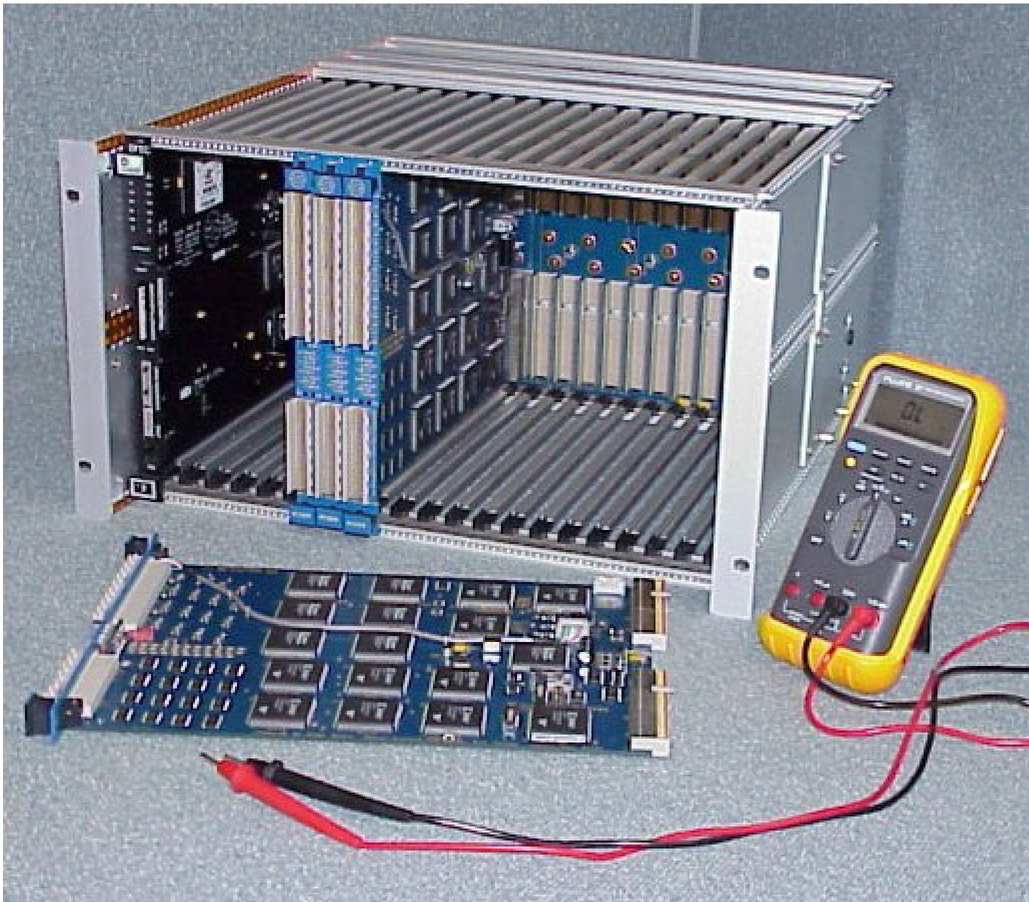

Figure 1, Picture of the mixer subrack.

Figure 2 shows a sketch of the mixer system backplane electrical interconnections. The backplane schematic is available in a separate document [Ref.4].

The backplane support the following interfaces:

Subrack controller general-purpose bus interface.
Used for configuration download and for remote access to the mixer boards. More information about the Subrack Controller is provided in separate documents [Ref.4, 5e].

Subrack controller slow monitoring serial bus interface.
During data acquisition, due to the proximity of the mixer system to detector components, noise considerations suggest to avoid accessing the mixer system over the "general purpose bus interface". The slow monitoring serial bus provides a way to readback status information from the mixer boards.

Subrack controller 1553 interface.
The subrack controller is remotely accessible through a MIL-STD-1553 serial bus. The MIL-STD-1553 is a networking standard used for integration of military platforms [Ref. 6]. The backplane host the two 1553 triaxial connectors needed by the subrack controller to implement the 1553 interface.

Board to board buses.
Mixer boards need to exchange part of the data they receive over the input links with the adjacent boards belonging to the same mixer subsystem (four boards). This is accomplished with two parallel buses 41 bit wide, one to the next backplane slot to the left and one to the next backplane slot to the right.

Timing signals distribution
Out of a mixer subsystem (group of four boards) the leftmost is used as "master" for distribution of global clock and global frame synchronization (SYNC) signals to the other three boards (slaves). The clock is distributed over three (one for each slave board) point-to-point LVDS connections. The SYNC is distributed over three point-to-point LVTTL connections.

Power supply.
A mixer board is powered through a backplane connection to the 3.3Volts subrack power supply. A small brick power supply is used to provide 5 Volts power needed by the subrack controller (slot 1). Two green LEDs, one for each supply voltage are ON when the backplane is powered. Three polyfuses are used as over-current protection. Each mixer board has its own over-current/over-voltage protection.

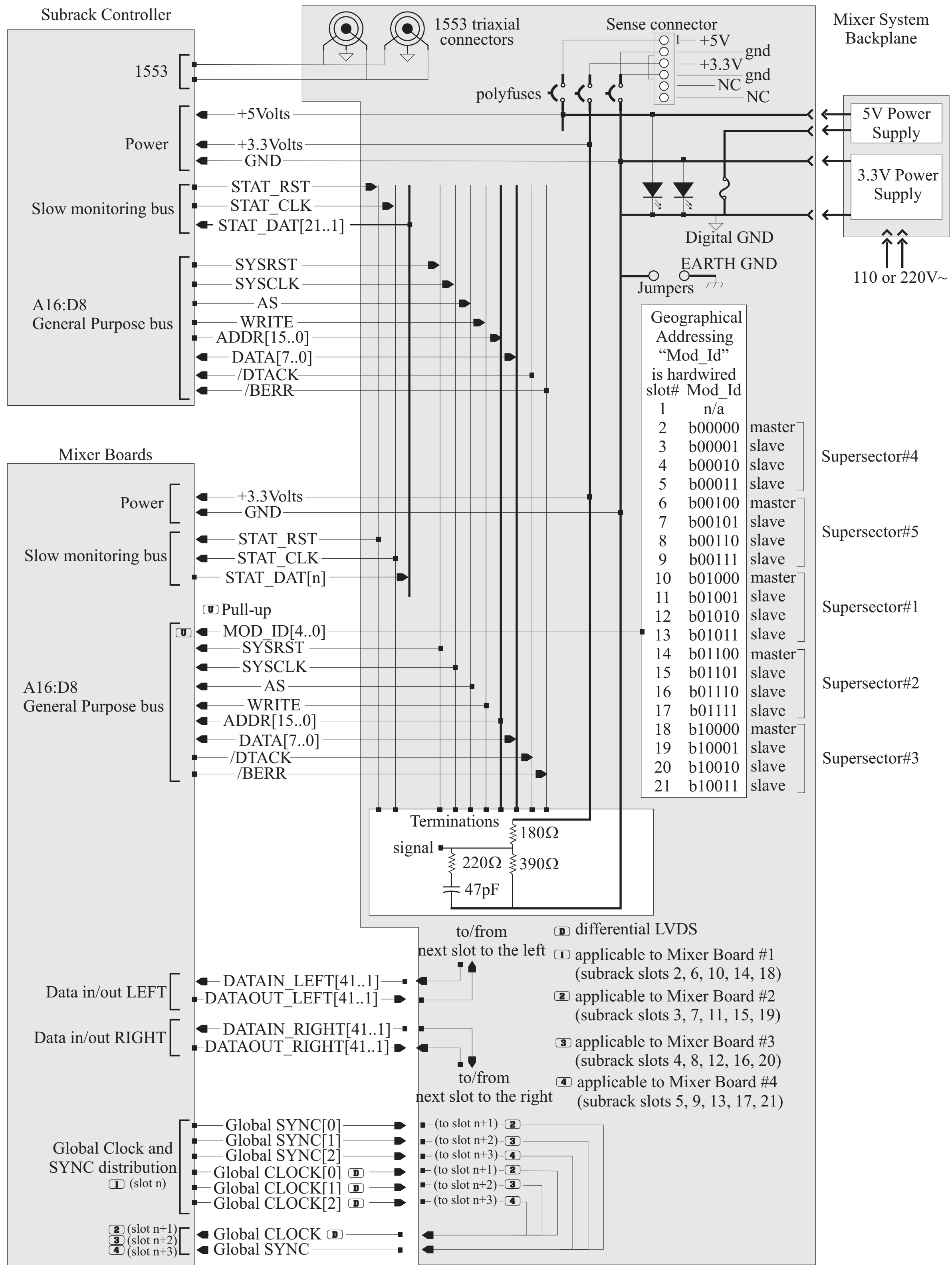

Figure 2, Mixer System backplane

3 Physical Attributes of the Backplane

3.1 Dimensions

The mixer system backplane is 16.910” [429.514mm] wide by 10.310” [261.874mm] high. The thickness is .192” [4.877mm], it was determined using a 8:1 aspect ratio of backplane thickness compared to the smallest thru hole diameter (0.024” [0.6096mm]). The 8:1 aspect ratio is the maximum allowable to assure even plating in thru holes.

3.2 Layer Description

The backplane is fourteen layers thick. Top and bottom layers are 1 oz. copper (thickness: .0014" [.0356mm]) pours attached to digital ground. Plated areas provide the option to connect these copper pours to the earth ground (chassis). There are five inner signal layers, two +3.3V layers, and five GND layers. Layer IN2 and IN4 have 100Ω differential impedance and are used for clock signals with the differential traces stacked in a broadside-coupled stripline fashion. The remainder of the signal layers has 50 Ω impedance and the signal traces are arranged in symmetrical stripline fashion. Figure 3 shows the layers stackup.

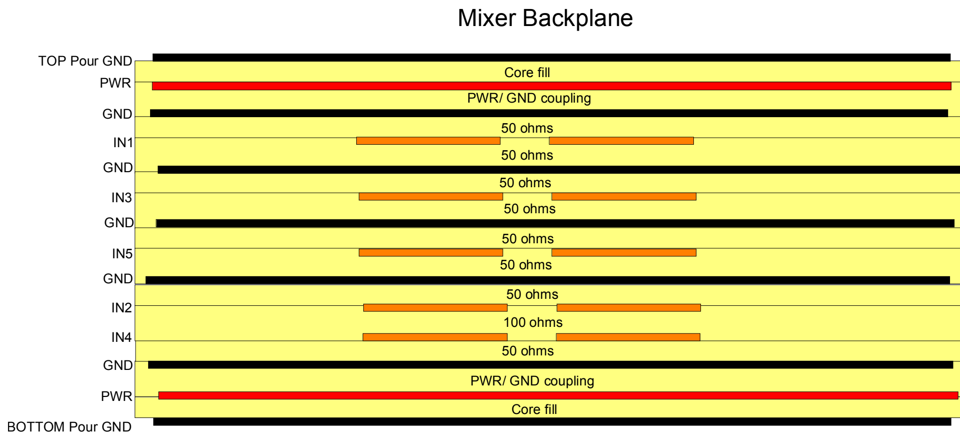

Figure 3, Mixer Backplane Stackup

3.3 Connectors

Backplane connectors used for power distribution to the Mixer Boards and signal lines are a combination of the A and B type 2mm hard metric [Ref. 7]. These are press fit connectors. Each slot is keyed in two places for guiding the mixer boards into the mixer system backplane.

3.4 Backplane to chassis mounting

Standard VME spec backplane mounting is used. Figure 4 shows the front side of the backplane, Figure 5 shows the rear of the backplane.

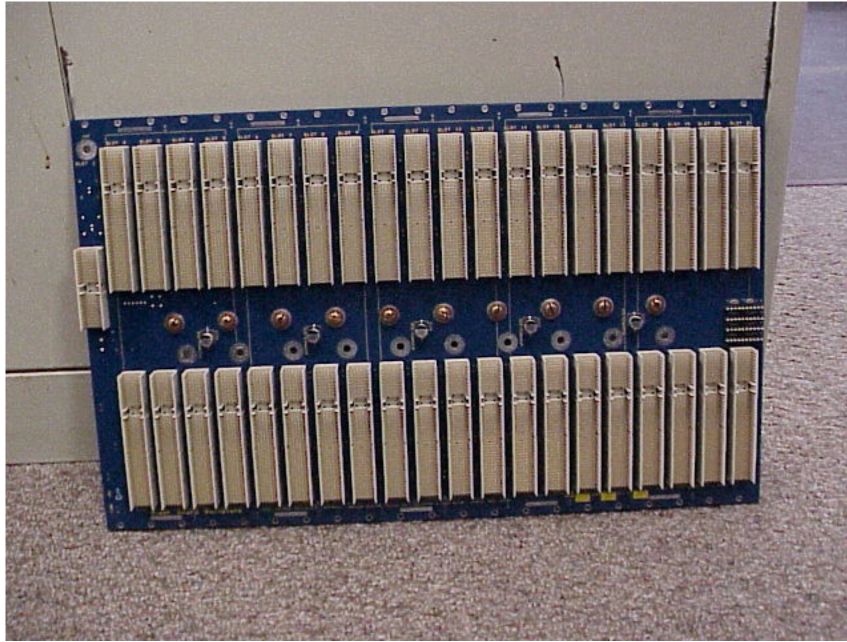

Figure 4. Front View of Mixer System Backplane

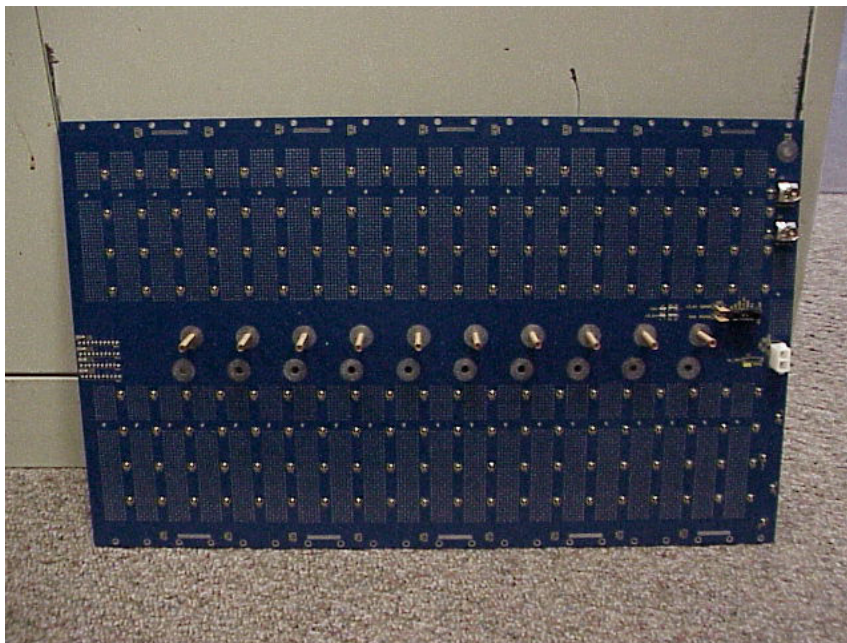

Figure 5. Rear View of Mixer System Backplane

3.5 DC power connections

Power connections meet the “Electrical Design Standards for Electronics to be used in Experiment Apparatus at Fermilab”, rev 4.0, dated October 16 1998 [Ref.3]. The +3.3V supply and the GND return are attached to the backplane via screws attached to the plated copper bus bar assemblies. See Figure 6, Figure 7 and Figure 8.

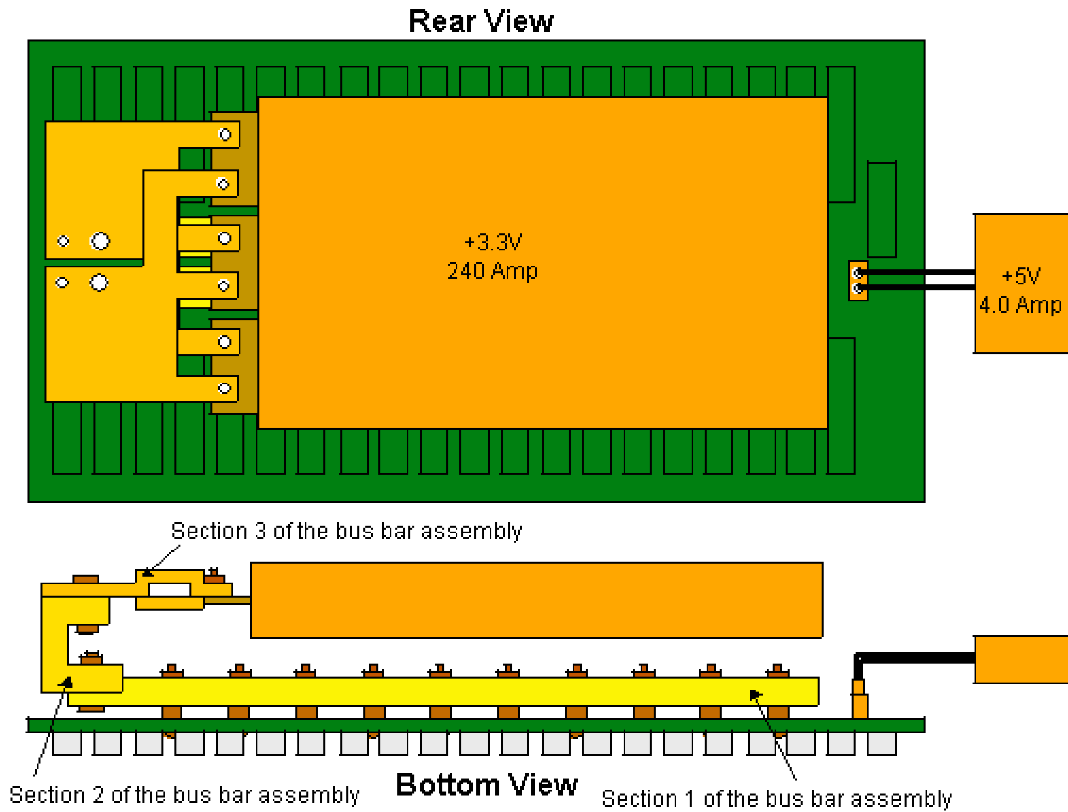

Figure 6. Backplane and Bus Bar Assembly

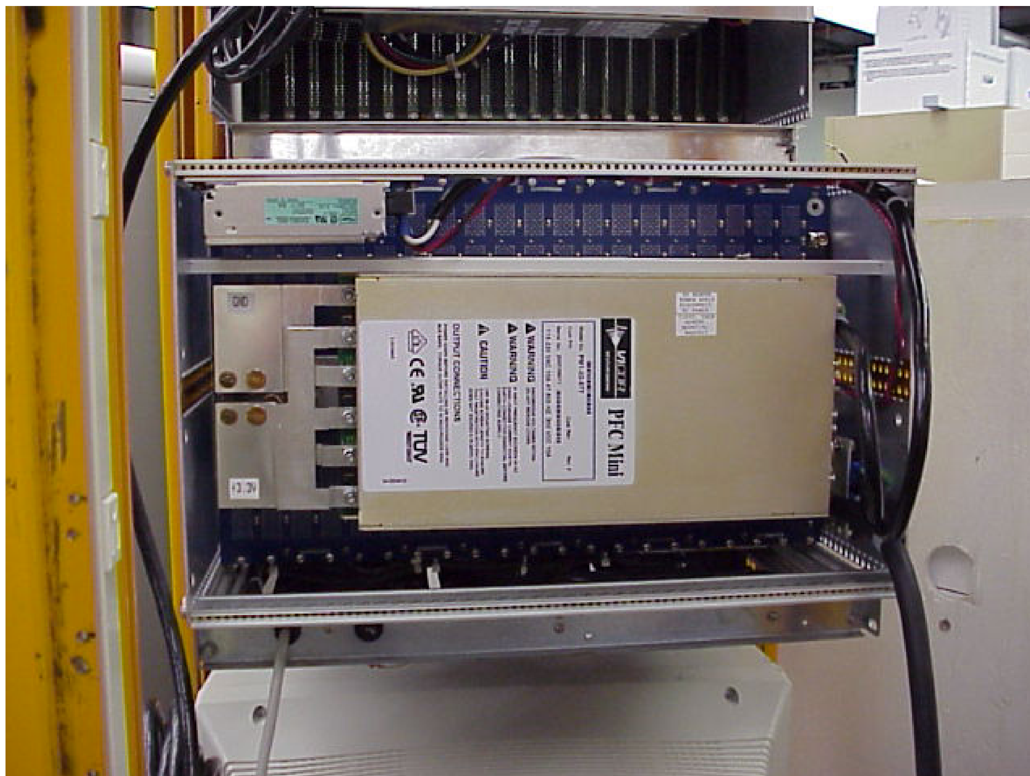

Figure 7. Picture of Mixer Crate with Power Supplies.

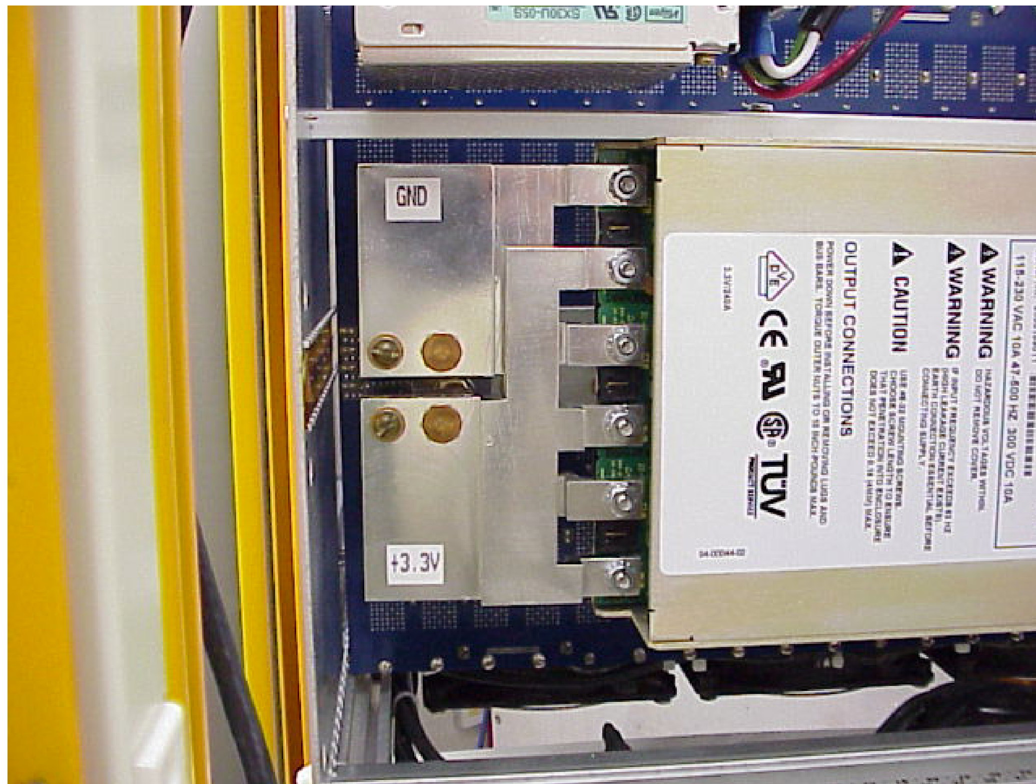

Figure 8. Picture of Bus Bar to Vicor Power Supply Connections.

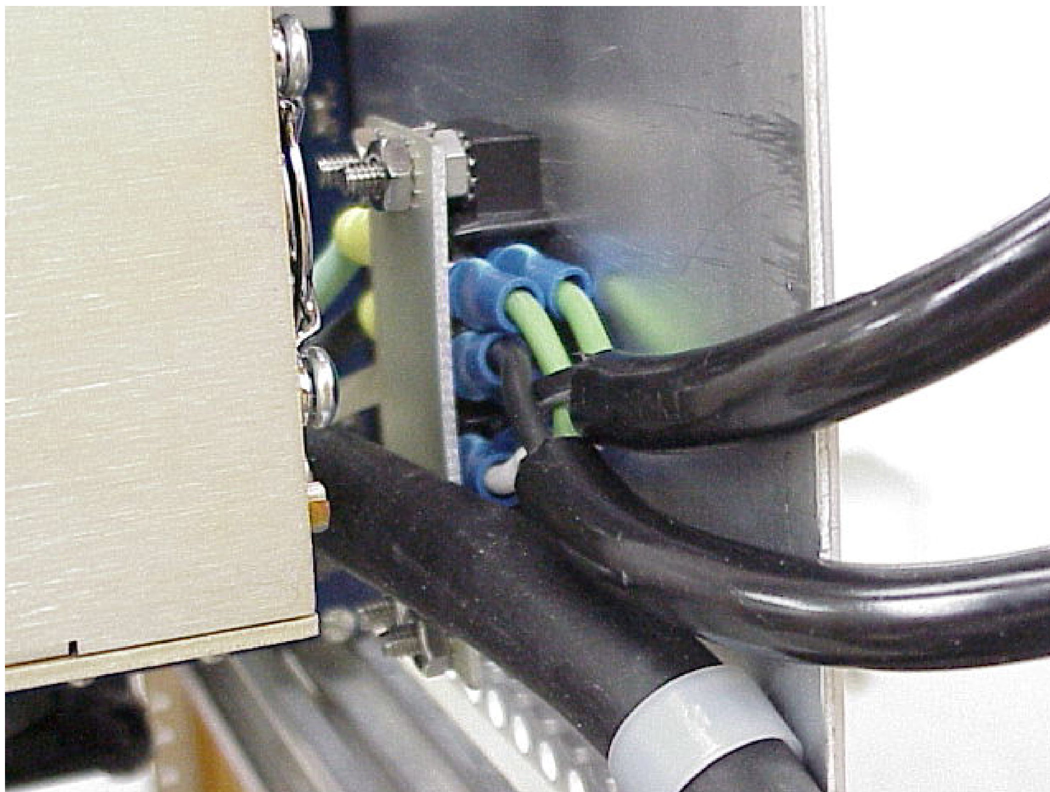

Figure 9. Picture of Mixer Subrack AC Terminal Block Connections

3.6 AC Distribution

BiRa Systems [Ref. 8] built the AC distribution box to D0 specifications. It is a 3U x 19” rack mount unit with circuit breakers on the front panel and AC sockets on the back side. Three phase AC is supplied to the box, and is then distributed as two phase AC to the power supplies. A dual receptacle single phase AC connection is also available. Each AC receptacle is individually controlled/protected with a circuit breaker. Additionally, the distribution box contains a relay to control all of the AC outputs; this relay is connected to the interlock system and requires 3-24 VDC @ 10mA to enable the AC outputs. The three phases are evenly distributed to nine two-phase outlets to allow for load balancing.

The schematic diagram of the AC distribution box is shown below:

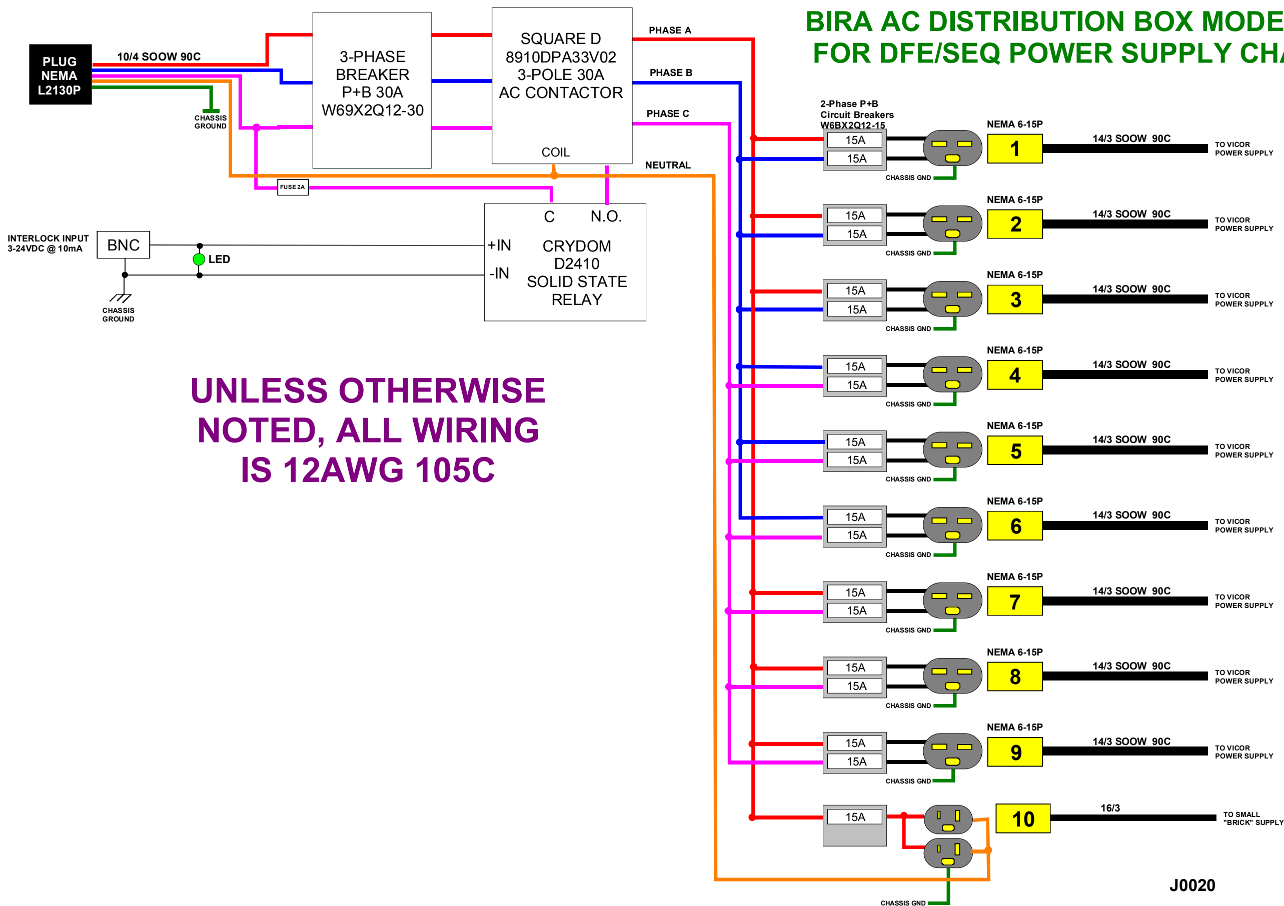

Figure 10, Schematic diagram of AC distribution box.

Figure 11. Picture of Backplane Bus Bar Assembly

Figure 12 shows components of the fastener used to attach the backplane to the bus bar assemblies. The +5V supply is used only for the crate controller (slot# 1) is attached via a molex style connector.

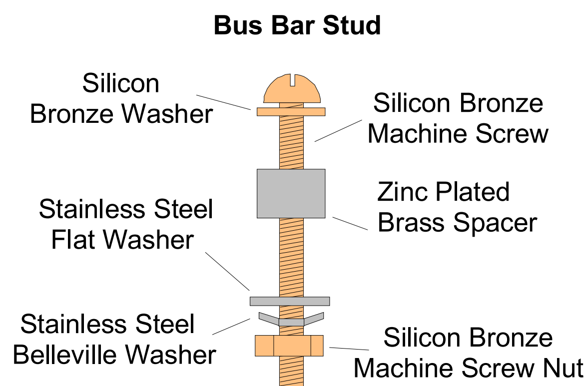

Figure 12. Bus Bar Stud

Figure 13 shows a bottom view of the backplane, fasteners, and section 1 (refer to Figure 6) of the bus bar assembly.

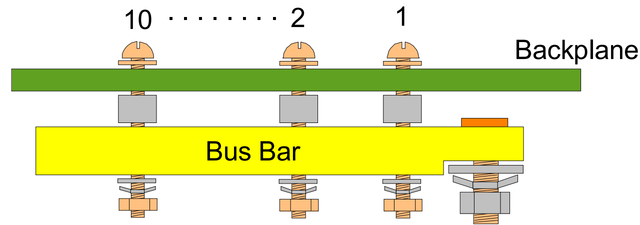

Figure 13. Backplane to Bus Bar Assembly

Figure 14 and Figure 15 show section 1 (refer to Figure 6) of the tin plated copper bus bar assemblies used for the +3.3V and GND.

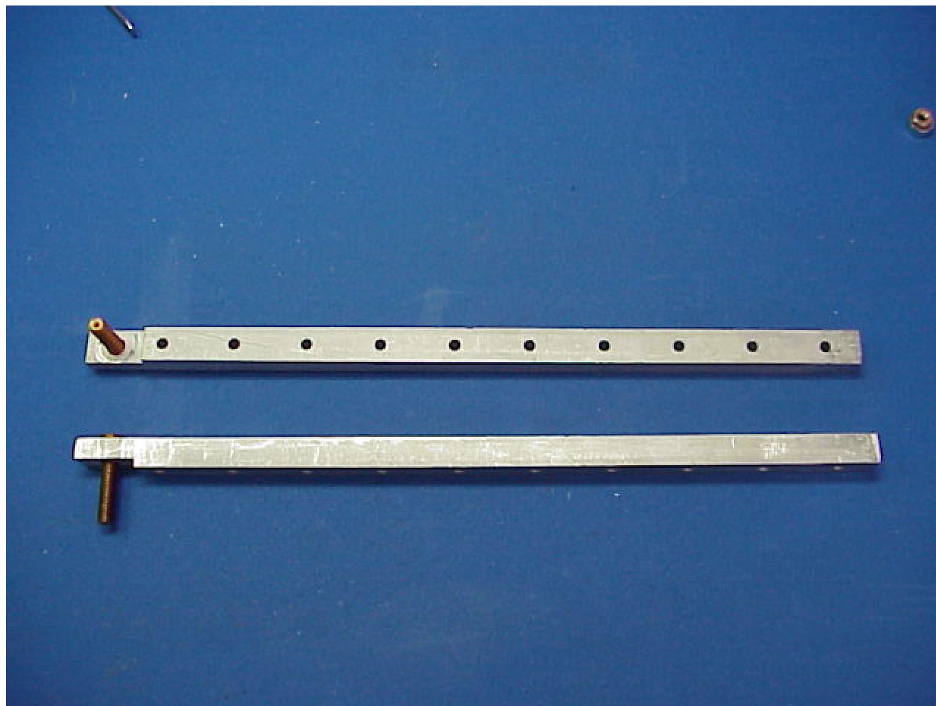

Figure 14. Picture of section 1 of Bus Bar Assembly

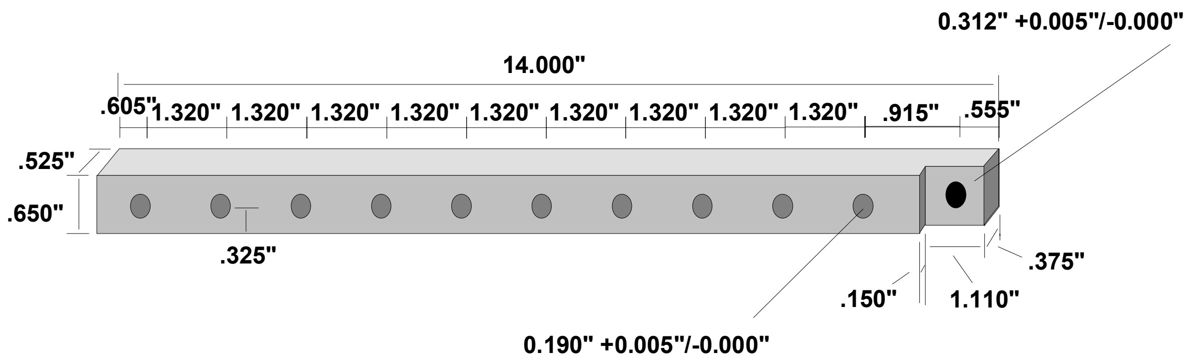

Figure 15. Mechanical Drawing of section 1 of Bus Bar Assembly

Figure 16 shows the hardware for sections 1 and 2 (refer to Figure 6) of the bus bar assemblies used for the +3.3V and GND.

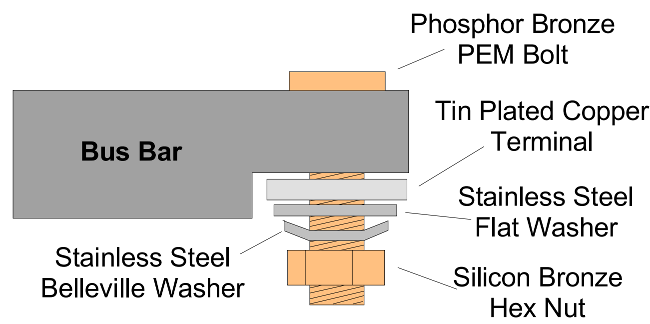

Figure 16. Mounting Hardware for Bus Bar Assembly sections 1 and 2

Figure 17 and Figure 18 show section 2 (refer to Figure 6) of the bus bar assemblies used for the +3.3V and GND.

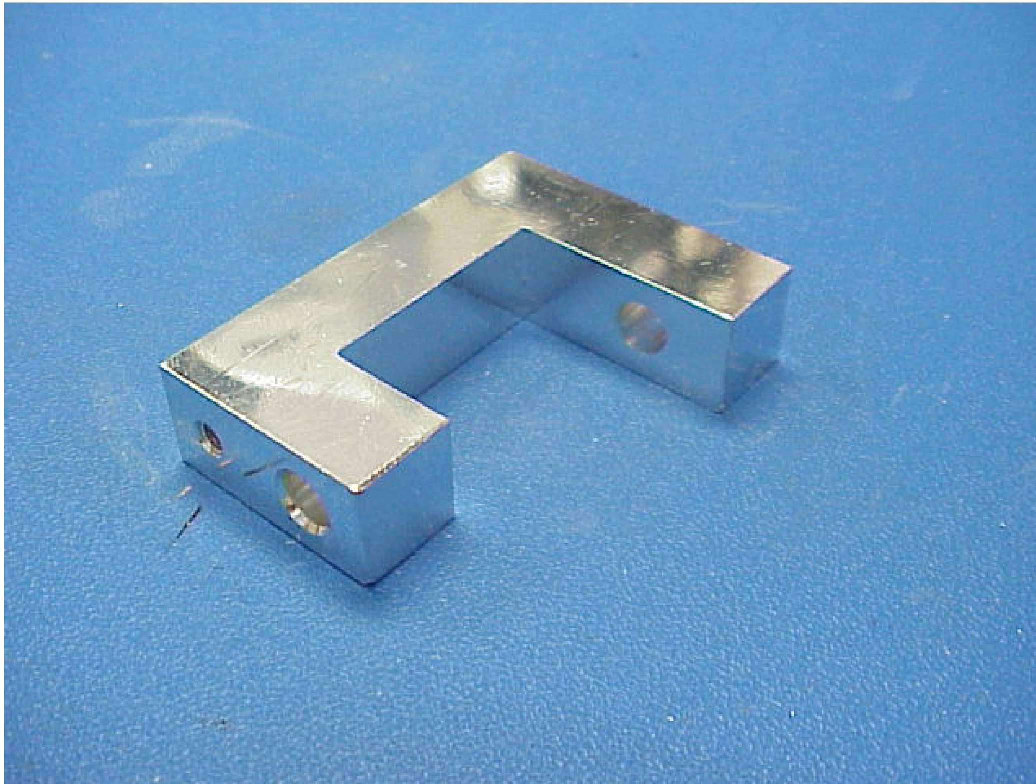

Figure 17. Picture of section 2 of Bus Bar Assembly

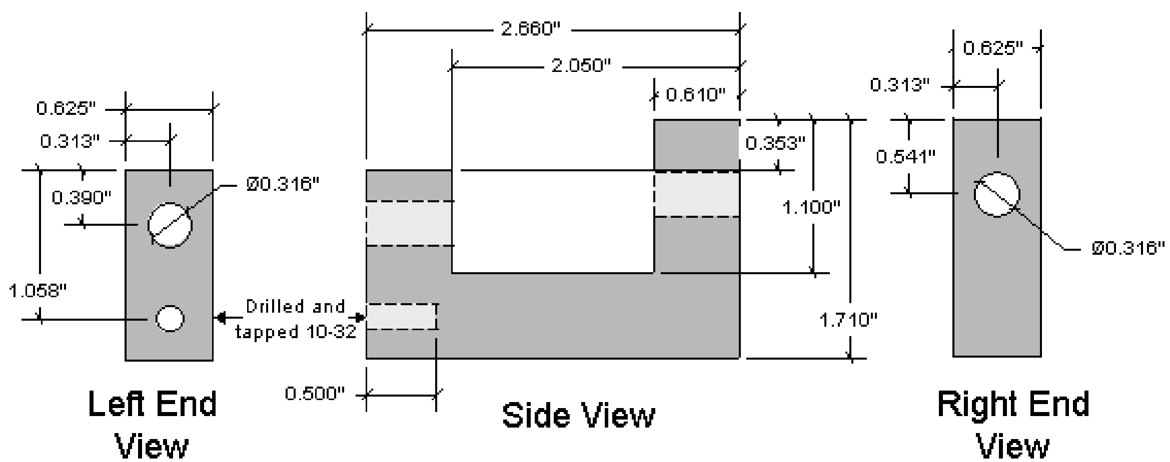

Figure 18. Mechanical Drawing of section 2 of Bus Bar Assembly

Figure 19 and Figure 20 show section 3 (refer to Figure 6) of the bus bar assemblies used for the +3.3V and GND.

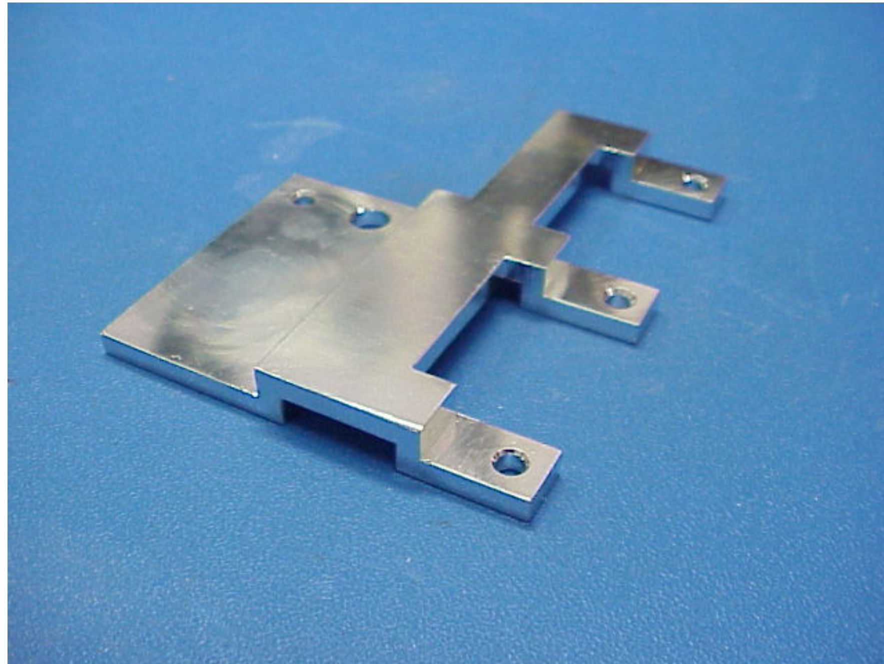

Figure 19. Picture of section 3 of Bus Bar Assembly

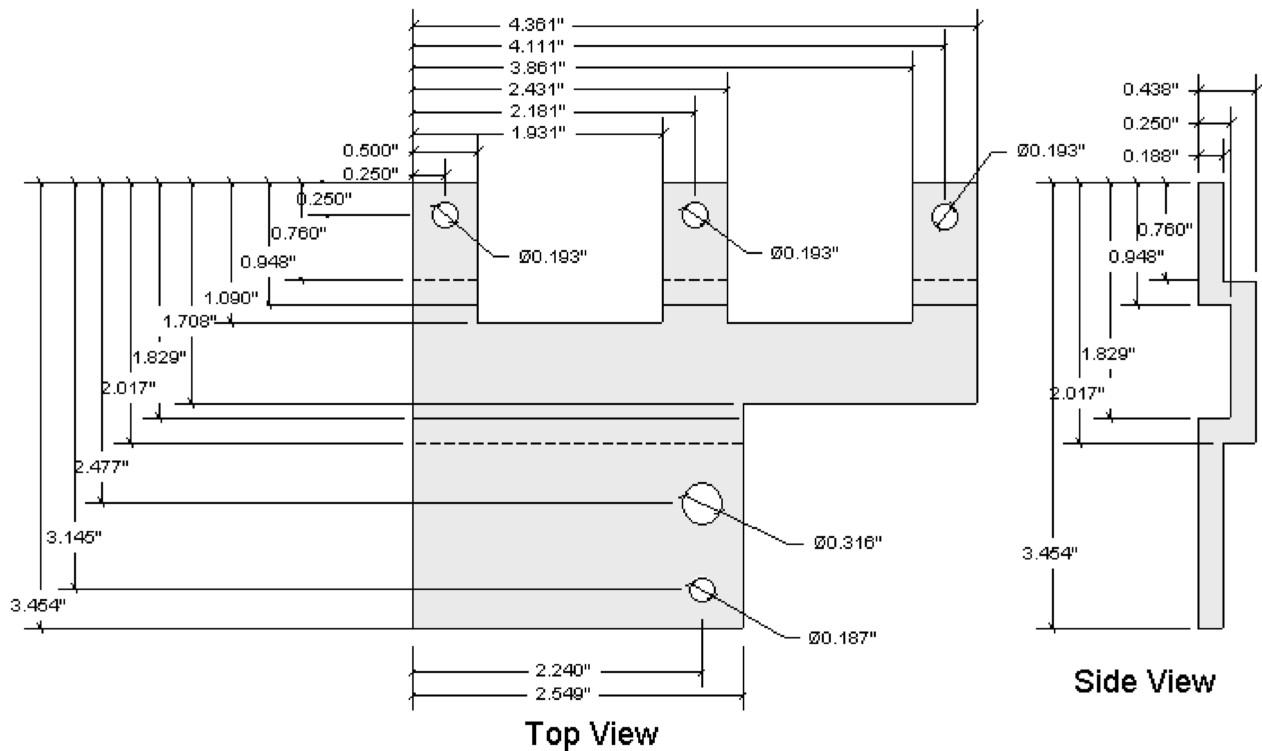

Figure 20. Mechanical Drawing of section 3 of Bus Bar Assembly

Section 3 of the Bus Bar assembly will be attached to the Vicor power supply using 8-32 silicon bronze nuts and lock washers.

3.7 Torque Specs

10-32 Silicon Bronze screws : 24 in.-lb [0.27651 Kg.-m].
5/16"-18 Phosphor Bronze PEM bolts:
125 in.-lb [1.440156 Kg.-m]. (torque spec for silicon bronze)
1/4"-20 Phosphor Bronze PEM bolts:
70 in.-lb. [0.806487 Kg.-m](torque spec for silicon bronze)
8-32 Silicon Bronze screws: 21 in.-lb [0.241946 Kg.-m].
8-32 Silicon Bronze nuts on Vicor Supply: 10 in.-lb (as per Vicor spec)

4 Power source

The +3.3V is supplied by an Vicor Mini PFC power supply [Ref. 20] using three 80 amp modules in parallel for a total of 240 amps @ +3.3V. +5V will be supplied by a small "brick" style supply.

5 Power requirements

As of this writing, estimated power requirements are 240 amps @ +3.3V, 2 amps @ +5V. Gnd is common and requires 240 amps.

6 Analysis of Current Densities

The areas of interest are shown below in Figure 21. Each area should follow the "no more than 1000 amps/sq.in." rule. The charts on the following pages breakdown each of these areas. For each chart, areas that conform to the 1000 amps/sq.in. [155 amps/sq cm] are colored green. Areas that don't are colored yellow. Special formulas are listed where appropriate.

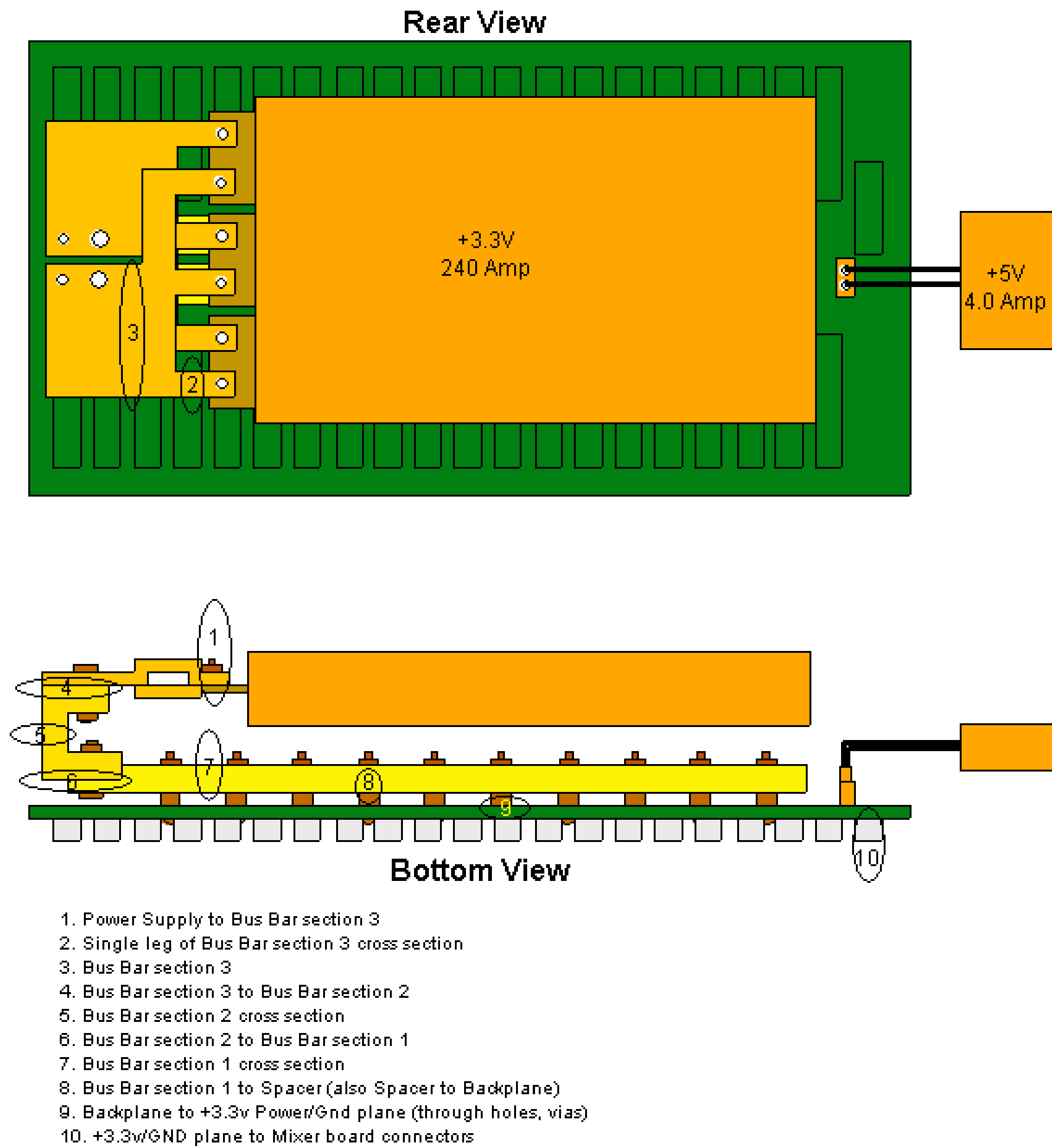

Figure 21. Analysis of Current Densities; Areas of Interest

Supply Name	From	To	Type	Amps	Area (sq. in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Power supply	Power Supply Bus Bar section 3 for +3.3v and GND.	Compression Flat	80	0.1884248 [1.215641]	1	424 [65]	Contact area of nut on power supply (.25 sq.in. [1.61 sq.cm]) – area consumed by power supply stud (.06157522 sq.in. [.3972587 sq.cm])

Table 1. Power Supply to Bus Bar section 3

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Single leg of section 3 Bus Bar Start	Bus Bar section 3	Cross Section	80	0.094 [0.60645]	1	851 [131]	Used cross sectional area of Single Leg of Bus Bar section 3. Cross section area (.188"x.500") [1.213cm x 3.226cm])

Table 2. Single Leg of Bus Bar section 3 Cross Section

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Bus Bar section 3 start	Bus Bar section 3 finish	Cross Section	240	0.419804 [2.7084]	1	571 [88]	Used main area of bus bar section 3 (2.549"x.188") [6.474 cm x .4775 cm] – area consumed by stud (".188x.316") [.4775 cm x .8026 cm]

Table 3. Bus Bar section 3

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Surface of Bus Bar section 3	Surface of Bus Bar section 2	Compression	240	0.740425 [4.7769]	1	324 [50]	Used contact area of Bus Bar section 2 (.625"x1.357") [1.5875cmx3.4468cm] - areas consumed by 2 mounting holes (.0784 sq. in.+.0293 sq. in.) [.5058 sq. cm + .189 sq. cm.]

Table 4. Bus Bar section 3 To Bus Bar section 2

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Bus Bar section 2 cross section start	Bus Bar section 2 cross section finish	Cross Section	240	0.38125 [2.45967]	1	629 [97]	Cross sectional area of bus bar section 2 (.610"x.625") [1.5494 cm x 1.5875 cm]

Table 5. Bus Bar section 2 Cross Section

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Surface of Bus Bar section 2	Surface of Bus Bar section 1	Compression	240	0.64505 [4.1616]	1	372 [57]	Area of contact on Bus Bar section 1 (.650"x1.11") [1.651cm x 2.8194cm] – area of stud hole (.07645 sq. in.) [.4932 sq. cm.]

Table 6. Bus Bar Section 2 to Bus Bar section 1

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Bus Bar Section 1 Start	Bus Bar Section 1 End	Cross Section	240	0.2415 [1.5581]	1	993 [153]	Cross sectional area of bus bar section 1 (.650" x .525") [1.651cm x 1.334cm]) – height of busbar x width of backplane power stud (.525" x .190") [1.334cm x .483cm]).

Table 7. Bus Bar Section 1 Cross Section

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Backplane Bus Bar	Spacer (standoff)	Compression Flat	240	0.16649 [1.074127]	10	144.1 [22.3]	Same spacer as +3.3V. Outside area of spacer (πr^2 where 2r = d =.500" [1.27cm]) – Inside area of spacer (πr^2 where 2r = d=.195" [.495cm])

Table 8. Bus Bar section 1 to Spacer (also spacer to Backplane)

Supply Name	From	To	Type	Amps	Area (sq in.) [sq.cm]	# in parallel	Net Amps/sq in. [Amps/sq.cm]	Measurement Notes for Area
+3.3V, GND	Backplane surface	Internal power plane	PC board vias	240	0.001385 [0.008935]	10	17322.9 [2685.1]	Construction of thru holes as per Figure 22. The "cross sectional area of a via" formula shown below was used. Plating thickness is .001" [.0254mm]. Finished hole size is .190" [4.83mm] for thru hole, and .024" [.61mm] for vias. 10 vias/thru hole

Table 9. Backplane to Power/GND Plane (thru holes, vias)

Cross Sectional Area of a Via

$r_{unplated}$ – radius of unplated thru hole (via)
r_{plated} – radius of plated thru hole (via)

$$Area_{Cross\ Section} = \left(\pi \cdot r_{uplated}{}^{2}\right) - \left(\pi \cdot r_{plated}{}^{2}\right)$$

Note that all of the current densities in thru holes and vias are beyond the 1000 amp/sq.in. [155 amps/sq cm] limit. The actual issue here is how much power is lost in these vias, and will the surrounding area be sufficient to dissipate the heat. Special bus bar mounting screw thru holes were created in the backplane to increase the number of current paths. See Figure 22.

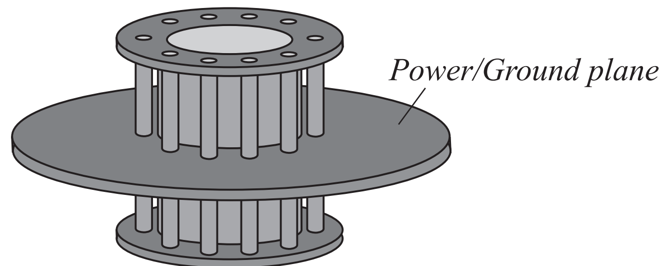

Figure 22. Side View of Through Hole

Power loss through the vias and thru holes is calculated using the formula below to determine the resistance of a single via and a single screw hole. Once these resistances are established, the parallel resistance of all of the vias and screw holes is determined. The formula

$$Power = Resistance \cdot (Current)^2 = R \cdot I^2$$

is then used to determine how much power would be dissipated in the area. We used .100” [2.54mm] for the variable *x* below. The .100” [2.54mm] is worst case. A temp value of 70°C (158°F) was used for these calculations.

Resistance (Ω) of a via or thru hole[1]

See Figure 23 for description of variables

ρ Bulk resistivity of copper $6.787*10^{-7}$ (Ω*in.)
δρ Thermal coefficient of resistance .0039
$r_{unplated}$ – radius of unplated thru hole or via (in.)
r_{plated} – radius of plated thru hole or via (in.)
x – separation between contact points (in.)

[1] Derived from “High Speed Digital Design, A Handbook of Black Magic”. Appendix C, pg. 413 *Resistance of a circuit trace*.

temp – temperature (°C)

$$Resistance = \frac{x \cdot \rho}{\left(\pi \cdot r_{unplated}^{\ 2}\right) - \left(\pi \cdot r_{plated}^{\ 2}\right)} \cdot \left(1 + \left(temp - 20\right) \cdot \delta\rho\right)$$

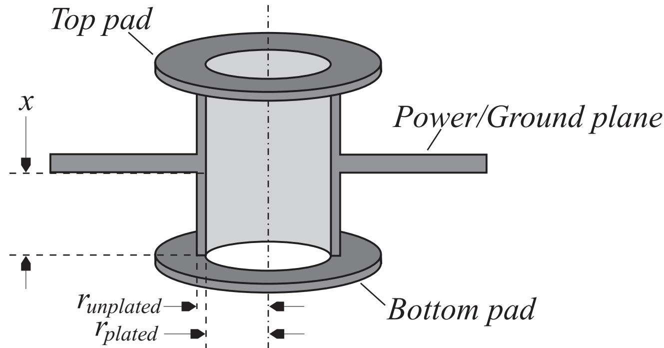

Figure 23. Side View of a Via

Resistance of the .190” [4.826mm] dia. thruhole

$$R_{190D} = \frac{.100 \cdot \rho}{\left(\pi \cdot .096^2\right) - \left(\pi \cdot .095^2\right)} \cdot \left(1 + \left(70 - 20\right) \cdot \delta\rho\right) = 1.35152E - 4\,\Omega$$

Resistance of .024" [0.610mm] dia via

$$R_{024D} = \frac{.100 \cdot \rho}{\left(\pi \cdot .013^2\right) - \left(\pi \cdot .012^2\right)} \cdot \left(1 + \left(70 - 20\right) \cdot \delta\rho\right) = 9.38553E - 5\,\Omega$$

R_{total} of +3.3V and GND thru holes and vias

$$R_{total} = \frac{1}{\sum_i \frac{1}{R_i}} \qquad with\ \ 1 \le i \le 110$$

$$for\ \ 1 \le i \le 100\ \ is\ \ Ri = R_{024D} = 9.38553\text{e - }5\ \Omega$$

$$for\ \ 101 \le i \le 110\ is\ R_i = R_{190D} = 1.35152\text{e - }4\ \ \Omega$$

$$R_{total} = \frac{1}{\frac{100}{R_{024D}} + \frac{10}{R_{190D}}} = \frac{1}{\frac{100}{9.38553\text{e - }5} + \frac{10}{1.35152\text{e - }4}} = 8.77608E - 7\,\Omega$$

Determining power loss in the +3.3V and GND vias and thru holes (Note: in all formulas used, GND and +3.3V calculations are the same.)

$$W_{GND} = I_{GND}^{\ 2} \cdot R_{total} = (200\,Amp)^2 \cdot 8.77608E-7\,\Omega = 5.055022E-2\,Watt \cong 50.6\,mWatt$$

Following the "power density of a circuit card should be limited to a maximum of ½ watt per square inch"[1] rule, the areas of each of the vias and thru holes are calculated, the total area for thru holes and vias is found, and the wattage per square inch determined. For these measurements, the formula for surface area of a cylinder was used. *d* is the diameter of the thru hole or via, and *x* is the distance from the backplane outer layer to the plane layer (.100" [2.54mm] worst case).

$$A_{thru_hole_surface} = \pi \cdot d \cdot x$$

For the .190" [4.826mm] dia. thru hole

$$A_{190surface} = \pi \cdot .190 \cdot .100 = 5.969\text{E - 2 sq.in.} = 38.5096\text{E - 2 sq.cm.}$$

For the .024" [0.610mm] dia. thru hole

$$A_{024surface} = \pi \cdot .024 \cdot .100 = 7.5398\text{E - 3 sq.in.} = 48.644\text{E - 3 sq.cm}$$

As shown before, each thru hole has 10 vias attached to it, and there are 10 thru holes per power supply. So for each supply,

+3.3V and GND total area

$$A_{GNDtotal} = 10 \cdot (10 \cdot (7.5398E-3) + 5.969E-2) = 1.35088\text{ sq.in} = 8.71534\text{ sq.cm}$$

Using the power loss figures we calculated earlier, determine the power loss for unit of area (power density) for the vias and thru holes for each supply.

$$Pd_{supply-thruhole_loss} = W_{supply} / A_{supply_thruhole}$$

+3.3V and GND thru holes and vias

$$Pd_{GNDthruhole_loss} = 5.055\text{E - 2} / 1.35088 = 3.742\text{E - 2} = 37.42\text{ mWatt/sq.in.} = 5.8\text{mWatt/sq.cm}$$

All of these power densities fall well within .500 Watt/sq.in. [.0775Watt/sq.cm] specification.

[1] From "Electrical Design Standards for Electronics to be used in Experiment Apparatus at Fermilab", Rev. 4.0 10/16/98, pg. 9

Table 10. Power/GND Plane to Connector.

Supply Name	From	To	Type	Amps	Area (sq in.)	# in parallel	Net Amps/Sq in.	Measurement Notes for Area
+3.3V	Thru holes and vias	Connector pins	Power/GND plane or copper pour. Sheet current	240	0.045657	2	2628.29358	Total current divided into cross sectional area of copper sheet (.0027" thick), over entire width of backplane (16.91"). Flow is vertical
GND	Thru holes and vias	Connector pins	Power/GND plane or copper pour. Sheet current	240	0.045657	5	1051.317432	Total current divided into cross sectional area of copper sheet (.0027" thick), over entire width of backplane (16.91"). Flow is vertical

Like the vias and thru holes listed in the previous chart, the power and gnd plane layers do not conform to the 1000 amps/sq.in. rule. Instead, the amount of power dissipated in the power and gnd layers will be calculated to determine if the backplane can handle the heat loss. The formula used for power dissipation is $W=I^2R$, where R is the resistance of the plane layers.

The construction of the backplane is such that each bus bar thru hole feeds the equivalent of two slots (10 thru holes per bus bar for 20 slots). For the resistance calculations below, d_0 is one bus bar thru hole and d_i is a connector thru hole. Since each slot has multiple d_i, we define the equivalent diameter value as:

$$\sqrt{\sum_{i=1}^{n}(d_i)^2}$$

Where n is the total number of connector pins in two slots that carry a particular voltage or gnd. This is defined as a section.

The value used for separation between contact points (x) is always the worst case instance.

Once the resistance for a section is calculated, the resistance for the entire plane is calculated by dividing the single section resistance by the total number of bus bar thru holes, in this case ten. This number is again divided by the number of times the plane occurs in the backplane to achieve the total resistance of the planes used for each voltage.

Calculating resistance (Ω) of a power or ground plane with one source and multiple destinations[2]

ρ Bulk resistivity of copper $6.787*10^{-7}$ (in.* *Ω*)
δρ Thermal coefficient of resistance .0039
d_0 – diameter of 0th contact point (in.)

[2] Derived from "High Speed Digital Design, A Handbook of Black Magic". Appendix C, pg. 414 *Resistance of a power or ground plane*

d_i – diameter of i^{nd} contact point (in.)
t – thickness of plane (in.)
x – separation between contact points (in.)
temp – temperature (°C)

$$R_{section} = \frac{\rho}{2 \cdot \pi \cdot t} \cdot \left[\ln\left[\frac{2 \cdot x}{d_0}\right] + \ln\left[\frac{2 \cdot x}{\sqrt{\sum_{i=1}^{n} (d_i)^2}}\right]\right] \cdot \left(1 + (temp - 20) \cdot \delta\rho\right)$$

Resistance calculations for +3.3V plane(s)

$$R_{3.3V_section} = \frac{6.787 \cdot 10^{-7}}{2 \cdot \pi \cdot .0014} \cdot \left[\ln\left[\frac{2 \cdot 3.20}{.190}\right] + \ln\left[\frac{2 \cdot 3.20}{\sqrt{38 \cdot (.024)^2}}\right]\right] \cdot \left(1 + (70 - 20) \cdot .0039\right) = 6.715E - 4\Omega$$

$$R_{3.3V_plane} = 6.715E - 4\Omega / 10\,sections = 6.715E - 5\Omega$$

$$R_{3.3V_planes} = 6.715E - 5\Omega / 2\,planes = 3.358E - 5\Omega$$

Resistance calculations for GND plane(s)

$$R_{GND_section} = \frac{6.787 \cdot 10^{-7}}{2 \cdot \pi \cdot .0014} \cdot \left[\ln\left[\frac{2 \cdot 4.56}{.190}\right] + \ln\left[\frac{2 \cdot 4.56}{\sqrt{680 \cdot (.024)^2}}\right]\right] \cdot \left(1 + (70 - 20) \cdot .0039\right) = 6.040E - 4\Omega$$

$$R_{GND_plane} = 6.040e - 4\Omega / 10\,sections = 6.040e - 5\Omega$$

$$R_{GND_planes} = 6.040e - 5\Omega / 5\,planes = 1.208E - 5\Omega$$

Power loss in +3.3V plane(s)

$$W_{3.3V_planes} = 240^2 \cdot 3.3581E - 5 = 1.934\,\text{Watt}$$

Power loss in GND plane(s)

$$W_{GND_planes} = 240^2 \cdot 1.028e-5 = 6.958E-1Watt \cong 696\,mWatt$$

Following the "power density of a circuit card should be limited to a maximum of ½ watt per square inch"[1] rule, the areas of the planes are calculated, and the wattage per square inch determined.

For the +3.3V plane

$$A_{3.3V_plane} = 3.40'' \cdot 16.70'' = 56.78 sq.in.$$

$$Pd_{3.3V_sq.in.} = \frac{W_{3.3V_planes}}{A_{3.3V_plane}} = (1.934\,Watt)/(56.78\,sq.in.) = 3.406E-2\,Watt/sq.in.$$

For the GND plane

$$A_{GND_plane} = 9.00'' \cdot 16.70'' = 150.3 sq.in.$$

$$Pd_{GND_sq.in.} = \frac{W_{GND_planes}}{A_{GND_plane}} = \frac{6.958\,E-1Watt}{150.30\,sq.in.} = 4.629\,E-3\,Watt\ /sq.in.$$

Worse case of the total power density is the watts/sq.in. sum of the 2 plane layers power densities since the 2 layers are stacked on top of each other.

$$Pd_{total_sq.in.} = \left(Pd_{3.3V_sq.in.} \cdot 2\right) + \left(Pd_{GND_sq.in.} \cdot 5\right)$$

$$Pd_{total_sq.in.} = 68.12E-3 + 23.145E-3 = 91.265E-3\,Watt/sq.in$$

This value of 91.265 mWatt/sq.in. falls well below the 500 mWatt/sq.in. (77.5mWatt/sq.cm) guideline.

[1] From "Electrical Design Standards for Electronics to be used in Experiment Apparatus at Fermilab", Rev. 4.0 10/16/98, pg. 9

7 Appendix A - Mixer System Backplane connectors pinout

Pin #	Row 'z' (bottom shield)	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f' (top shield)
1	GND	INLFT2	GND	INLFT1	GND	OUTRT1	
2		GND	INLFT3	GND	OUTRT2	GND	GND
3	GND	INLFT4	GND	OUTRT3	GND	OUTRT4	
4		GND	INLFT5	GND	OUTRT5	GND	GND
5	GND	INLFT7	GND	INLFT6	GND	OUTRT6	
6		GND	INLFT8	GND	OUTRT7	GND	GND
7	GND	INLFT9	GND	OUTRT8	GND	OUTRT9	
8		GND	INLFT10	GND	OUTRT10	GND	GND
9	GND	INLFT12	GND	INLFT11	GND	OUTRT11	
10		GND	INLFT13	GND	OUTRT12	GND	GND
11	GND	INLFT14	GND	OUTRT13	GND	OUTRT14	
	polarizing and guiding peg						
12	GND	GND	INLFT15	GND	OUTRT15	GND	
13		INLFT17	GND	INLFT16	GND	OUTRT16	GND
14	GND	GND	INLFT18	GND	OUTRT17	GND	
15		INLFT19	GND	OUTRT18	GND	OUTRT19	GND
16	GND	GND	INLFT20	GND	OUTRT20	GND	
17		INLFT22	GND	INLFT21	GND	OUTRT21	GND
18	GND	GND	INLFT23	GND	OUTRT22	GND	
19		INLFT24	GND	OUTRT23	GND	OUTRT24	GND
20	GND	GND	INLFT25	GND	OUTRT25	GND	
21		INLFT27	GND	INLFT26	GND	OUTRT26	GND
22	GND	GND	INLFT28	GND	OUTRT27	GND	
1		INLFT29	GND	OUTRT28	GND	OUTRT29	GND
2	GND	GND	INLFT30	GND	OUTRT30	GND	
3		INLFT32	GND	INLFT31	GND	OUTRT31	GND
4	GND	GND	INLFT33	GND	OUTRT32	GND	
5		INLFT34	GND	OUTRT33	GND	OUTRT34	GND
6	GND	GND	INLFT35	GND	OUTRT35	GND	
7		INLFT37	GND	INLFT36	GND	OUTRT36	GND
8	GND	GND	INLFT38	GND	OUTRT37	GND	
9		INLFT39	GND	OUTRT38	GND	OUTRT39	GND
10	GND	GND	INLFT40	GND	OUTRT40	GND	
11		GND	GND	INLFT41	GND	OUTRT41	GND
12	GND	MOD_ID4	MOD_ID3	MOD_ID2	MOD_ID1	MOD_ID0	
13		+IN_CLK	GND	+OUT_CLK0	+OUT_CLK1	+OUT_CLK2	GND
14	GND	-IN_CLK	GND	-OUT_CLK0	-OUT_CLK1	-OUT_CLK2	
15		GND	GND	GND	GND	GND	GND
16	GND	STAT_CLK	GND	STAT_RST	GND	STAT	
17		Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	GND
18	GND	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	
19		Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	GND

Table 11, Pin/Signal assignments for the backplane top section connector

Pin #	Row 'z' (bottom shield)	Row 'a'	Row 'b'	Row 'c'	Row 'd'	Row 'e'	Row 'f' (top shield)
1	GND	VADDR7	VWRITE	VDAT6	VDAT5	VDAT2	
2		VADDR15	*SYSRST	VDAT7	VDAT0	VDAT3	GND
3	GND	VADDR12	VAS	VSYSCLK	VDAT1	VDAT4	
4		VADDR9	*VDTACK	*VBERR	VADDR13	VADDR5	GND
5	GND	VADDR11	VADDR2	VADDR10	VADDR0	VADDR3	
6		VADDR8	VADDR6	VADDR1	VADDR14	VADDR4	GND
7	GND	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	
8		Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	Power 3.3V	GND
9	GND	OUTLFT2	GND	OUTLFT1	GND	INRT1	
10		GND	OUTLFT3	GND	INRT2	GND	GND
11	GND	OUTLFT4	GND	INRT3	GND	INRT4	
	polarizing and guiding peg						
12	GND	GND	OUTLFT5	GND	INRT5	GND	
13		OUTLFT7	GND	OUTLFT6	GND	INRT6	GND
14	GND	GND	OUTLFT8	GND	INRT7	GND	
15		OUTLFT9	GND	INRT8	GND	INRT9	GND
16	GND	GND	OUTLFT10	GND	INRT10	GND	
17		OUTLFT12	GND	OUTLFT11	GND	INRT11	GND
18	GND	GND	OUTLFT13	GND	INRT12	GND	
19		OUTLFT14	GND	INRT13	GND	INRT14	GND
20	GND	GND	OUTLFT15	GND	INRT15	GND	
21		OUTLFT17	GND	OUTLFT16	GND	INRT16	GND
22	GND	GND	OUTLFT18	GND	INRT17	GND	
1		OUTLFT19	GND	INRT18	GND	INRT19	GND
2	GND	GND	OUTLFT20	GND	INRT20	GND	
3		OUTLFT22	GND	OUTLFT21	GND	INRT21	GND
4	GND	GND	OUTLFT23	GND	INRT22	GND	
5		OUTLFT24	GND	INRT23	GND	INRT24	GND
6	GND	GND	OUTLFT25	GND	INRT25	GND	
7		OUTLFT27	GND	OUTLFT26	GND	INRT26	GND
8	GND	GND	OUTLFT28	GND	INRT27	GND	
9		OUTLFT29	GND	INRT28	GND	INRT29	GND
10	GND	GND	OUTLFT30	GND	INRT30	GND	
11		OUTLFT32	GND	OUTLFT31	GND	INRT31	GND
12	GND	GND	OUTLFT33	GND	INRT32	GND	
13		OUTLFT34	GND	INRT33	GND	INRT34	GND
14	GND	GND	OUTLFT35	GND	INRT35	GND	
15		OUTLFT37	GND	OUTLFT36	GND	INRT36	GND
16	GND	GND	OUTLFT38	GND	INRT37	GND	
17		OUTLFT39	GND	INRT38	GND	INRT39	GND
18	GND	GND	OUTLFT40	GND	INRT40	GND	
19		GND	GND	OUTLFT41	GND	INRT41	GND

Table 12, Pin/Signal assignments for the backplane bottom section connector.

8 References

[1] Howard Johnson, Martin Graham,
"High Speed Digital Design", 1993, Prentice Hall PTR. ISBN 0-13-395724-1.
[2] Wade D.Peterson, VMEbus International Trade Association, "The VMEbus Handbook", Fourth edition 1997. ISBN 1-885731-08-6.
[3] "Electrical Design Standards for Electronics to be used in Experiment Apparatus at Fermilab", Rev. 4.0 10/16/98
[4] D0 CTT Mixer System documentation. Information available on the Internet:
http://www-ese.fnal.gov/D0_CTT_Mixer/
[5] Jamieson T. Olsen,
- **a)** "Digital Front End Mother Board register map", Engineering Note 2000-01-28a.
- **b)** "DFE and Mixer Board Registers ", Engineering Note 2000-01-28a.
- **c)** "DFE backplane address/data bus protocol", Engineering Note 2000-03-28a.
- **d)** "DFE slow monitoring custom serial bus specification", Engineering Note 2000-01-31a.
- **e)** Digital Front End Controller (DFEc) Board:
http://d0server1.fnal.gov/users/jamieson/www/projects/dfec/index.html

Information available on the internet:
http://d0server1.fnal.gov/users/jamieson/www/index.html
[6] MIL-STD-1553 is a military standard that defines the electrical and protocol characteristics for a data bus. Information on the 1553 standard is available on the internet from several sources, one of them is:
http://www.1553-mil-std.com/

[7] Amp. Web site: http://www.amp.com/
[8] BiRa Systems. Web site: http://www.bira.com/
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[17] Penn-Engineering. Web site: http://www.penn-eng.com/
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[19] Trompeter Electronics. Web site: http://www.trompeter.com/
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