FEDERAL TRADE COMMISSION

I N D E X (PUBLIC RECORD)

UNITED STATES OF AMERICA

FEDERAL TRADE COMMISSION

In the Matter of:)

Rambus, Inc.) Docket No. 9302

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Monday, June 23, 2003

9:30 a.m.

TRIAL VOLUME 33

PART 1

PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE

Chief Administrative Law Judge

Federal Trade Commission

600 Pennsylvania Avenue, N.W.

Washington, D.C.

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P R O C E E D I N G S

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JUDGE McGUIRE: Good morning, Counsel.

ALL COUNSEL: Good morning, Your Honor.

JUDGE McGUIRE: This hearing is now in order.

Any items that should come to the Court's attention before we begin today?

MR. STONE: Yes, Your Honor, I do have one issue, if I might.

This arises in connection with the private action involving Hynix in District Court out in California, and they have asked us in connection with that case to produce exhibits which have been admitted in camera and testimony which has come in in camera here in this proceeding.

As to the exhibits, we believe that since all the exhibits that were admitted in camera, we have them pursuant to the terms of the protective order, that so long as we comply with the protective order and give notice to third parties, that we can go ahead and provide them those exhibits and plan to do so unless there's some objection from complaint counsel or if Your Honor has a concern that the in camera order might override that. I don't believe it does.

As to the testimony, however, the only order

JUDGE McGUIRE: Do you have any comment, Mr. Oliver?

MR. OLIVER: Your Honor, we have not had an opportunity to consider this, if we could have perhaps a day to consider this.

JUDGE McGUIRE: Yes, that will be fine.

Yeah, I think in terms of the -- we are talking about the August 2002 protective order?

MR. STONE: Yes, that protective order governs the documents.

JUDGE McGUIRE: Yes, but -- I know, right.

MR. STONE: The in camera testimony I believe is governed by your in camera order and the FTC's regulations.

JUDGE McGUIRE: Yes, which you are saying does not cover this circumstance.

MR. STONE: That's my belief, that it does not.

JUDGE McGUIRE: It would be my suggestion that Hynix offer the Court a proposed supplement to that order, and then the parties and any other third parties could then, you know, be free to comment on that as well, and then I could issue an order either way and then determine how this ought to be handled.

MR. STONE: That's fine with us, Your Honor, and I'll talk to Hynix's counsel and complaint counsel,

and maybe we can all agree to the format.

JUDGE McGUIRE: Maybe you can come up with something that will expedite this and then give some guidance on this issue to Hynix.

MR. STONE: That would be fine.

JUDGE McGUIRE: But I want to comport with whatever outstanding orders I have and whatever is the current FTC rules on this area, and if we can all come to terms on that, then that will be fine. I have no problem with that.

MR. STONE: Thank you, Your Honor.

JUDGE McGUIRE: Yes, sir.

MR. NISSLY: Pardon my interruption, Your Honor. Ken Nissly, I represent Hynix, and we will be happy to talk to Mr. Stone and Mr. Oliver to get this issue resolved.

JUDGE McGUIRE: Okay, good.

At this time, complaint counsel may call its next witness.

MR. OLIVER: Thank you, Your Honor. Complaint counsel calls Mr. Terry Lee.

JUDGE McGUIRE: Mr. Lee, would you please approach the Bench and you'll be sworn in by the court reporter.

Whereupon--

TERRY R. LEE

a witness, called for examination, having been first duly sworn, was examined and testified as follows:

JUDGE McGUIRE: If you will have a seat right there, Mr. Lee.

Go ahead, Mr. Oliver.

DIRECT EXAMINATION

BY MR. OLIVER:

Q. Good morning, Mr. Lee.

A. Good morning.

Q. How are you today?

A. Good, thank you.

Q. Could you please state your full name for the record?

A. My name is Terry Robert Lee.

Q. And are you currently employed?

A. Yes.

Q. Where do you work today?

A. Micron Technology.

Q. What's your current position at Micron?

A. It is executive director of advanced technology and strategic marketing.

Q. Could you please describe your responsibilities in that position?

A. Yes, I'm responsible for four functions, have

four groups. One is called transceiver development group; another is advanced circuit or advanced systems research lab; another is advanced systems technology development; and a final is strategic marketing.

Q. Now, do other Micron employees report to you in your position?

A. That's correct.

Q. Approximately how many people report to you?

A. I believe it's about 93.

Q. Now, you outlined four different functions. I believe you stated first transceiver development. Is that right?

A. That's correct.

Q. Can you explain in a bit more detail what that means?

A. Sure. They perform integrated circuit design for I/O circuits, circuits for communicating off chip, if you will.

Q. And then I believe you also referred to advanced systems research lab. Is that right?

A. Yes.

Q. And what is the function of that group?

A. They do high-speed signal integrity, so they do bus analysis for allowing systems to communicate at high speeds.

Q. And then you also mentioned advanced systems development. Is that right?

A. Advanced systems technology development.

Q. Thank you.

What does that group do?

A. They do logic design and board design, system design. They develop first platforms for new technology.

Q. Now, is that directed towards implementation of current products, or is that directed towards future products?

A. Future products.

Q. And then I believe you also mentioned strategic marketing. Is that right?

A. Correct.

Q. Can you please explain what that involves?

A. Sure. There's actually several functions within that group. There's applications engineering, there's a segment marketing group, there's product definition, and then there's outbound marketing.

Q. I'm sorry, what was the last one?

A. Outbound.

Q. And could you please explain briefly what those groups do?

A. Sure. Applications engineers provide technical

support for customers on existing products, so that involves things like data sheets and customer visits and debugging, problems there might be at the customer using our products.

The second marketing group is a little bit more of a classical marketing role. It is technical marketing, but they're organized by market segments to make sure that we provide the right products for those segments and also to help enable the customer to use our products and move products into those segments.

The product definition role is responsible for defining new products, products that we don't have today. They work a lot with JEDEC and the industry and customers on trying to establish the requirements for new products.

And then outbound marketing is more of a classical marketing role with advertising and trade shows and things like that.

Q. If I could take a step back and ask about your educational background. Could you please explain briefly what your educational background is?

A. Sure. I have a Bachelor's of Science in electrical engineering out of the University of Missouri, Columbia, in 1983. And I have a Master's of Science in electrical engineering out of the University

of Southern California, 1985. And I'm currently working on an MBA out of the University of Washington.

Q. And in your graduate studies in electrical engineering, did you focus on any particular field?

A. Yes, it was in computer engineering and integrated circuits.

Q. Now, after you finished college, when did you enter the work force?

A. I actually started full-time work in 1983 after my Bachelor's.

Q. And where did you work?

A. I worked at Hughes Aircraft Company, Radar Systems Group.

Q. And how long did you work with Hughes?

A. Six years.

Q. And when did you start working for Micron Technology?

A. 1989.

Q. And can you please explain just very briefly the different positions that you've held at Micron since 1989?

A. Sure. I started as a senior design engineer, did integrated design, integrated circuit design for DRAM products, four-meg DRAMs, video RAMs and products like that.

Then I transitioned to applications engineering and also strategic marketing and then product definition. Then I had taken on my current role.

Q. Okay, if we can start with your role as senior design engineer, first of all, what years did you hold that position?

A. I think I held senior design engineer until around 1991 or 1992.

Q. And can you please explain in a bit more detail what your responsibilities were in that position?

A. Sure. It was integrated circuit design. I was involved with some four-meg DRAM products, working on the circuit design, as well as in video RAM products that we did, one-meg video RAMs.

Q. You mentioned four-meg DRAM products. How many people worked on the design of those products?

A. The design team varied. Typically we would have three or four circuit designers like myself, and there would be three or four people doing physical layout, which is basically drawing the geometries for the circuits, somewhat like a draftsman role, with computer-aided design.

Q. So, you're one of three or four people actually doing the circuit design work?

A. That's correct.

Q. And then next I believe you mentioned applications engineer.

A. Yes.

Q. Is that right?

Could you please explain in a little more detail what your responsibilities were as an applications engineer?

A. Sure. I worked quite a bit with customers. We were providing technical support to help them understand how to use our product, to help them understand why perhaps -- if they were using our product in a system, if their system wasn't working, whether they were violating certain timing on the part, worked with them on trying to understand what their future product direction was and what their requirements were for new products.

And we also tried to at times share with them what our product roadmap would be going forward as well as to understand what their product roadmaps were in the future.

Q. I think you next mentioned strategic marketing. Is that right?

A. Yes.

Q. Do you recall when you started performing a strategic marketing function?

A. Not exactly. The transition from applications engineering to strategic marketing and product definition was all in the same group, and so it's a little bit of a fuzzy delineation, if you will, from one to the other, but it might have been on the order of a year or two later, I started doing that.

Q. So, that would have been in the roughly 1993 or 1994 time period?

A. Yeah, maybe around '93.

Q. '93, okay.

And can you explain in a little bit more detail what the strategic marketing responsibilities were?

A. Sure. With the marketing role, I was more trying to identify specific features and functions that were going to be on our next device, tried to basically be an interface between what the customer wanted and what we needed to provide design for -- directions in terms of design.

Q. Now, ever since you started doing strategic marketing work in roughly the 1993 time frame, have you been doing similar types of work ever since?

A. I'm sorry, the question again?

Q. Have you been -- have you had similar responsibilities ever since?

A. Since '93?

Q. Yes.

A. Ah, yes in terms of working with the customers and, you know, identifying roadmaps and trying to identify opportunities in the future, that part of it. My responsibilities have increased, and I now have people doing the roles that I was doing before.

Q. You mentioned that your responsibilities increased. Approximately when did that happen?

A. I believe around 1999, I started the development of the advanced systems research lab, and around 2001, we reorganized, and all of those four functions came underneath my responsibility.

Q. Would it be fair to say, then, that since about 1993, your -- the focus of your work at Micron has been on future products?

A. Yes, that's true.

Q. Now, can you please explain in a little more detail what role customer interaction has had in your work at Micron?

A. It's had a variety of roles. We have a lot of interaction with customers through regular meetings that we'll have either at our company or at theirs, or we would discuss -- depending on the customer, we would discuss what our future plans were for both products and technology going forward and as well as their

future plans.

We would also discuss current issues on today's products, where maybe they're having some challenges or trying to get our part validated in their system. We have a lot of technical exchange. My role tends to be more technical in nature, so we talk quite a bit about some of the system issues and some of the kind of problems they'd like to have solved in the future and some of the constraints and requirements they have for their future products.

Q. Now, Mr. Lee, are you familiar with an organization known as JEDEC?

A. Yes, I am.

Q. How did you become familiar with JEDEC?

A. I believe the first time I attended JEDEC was around 1994, sometime in '94. Terry Walther, who was our JEDEC representative, asked me to attend. And then since that time, I've attended periodically up until about the last year or so I'd say.

Q. Now, you mentioned Terry Walther. Who is he?

A. Terry Walther works for Micron, and he's our JEDEC representative.

Q. Now, what was your understanding of why Mr. Walther asked you to attend certain JEDEC meetings?

A. He asked me to provide some technical supports

for some current issues that were being discussed in the committee.

Q. Now, when you attended JEDEC meetings, did you attend the meetings of any particular committees or subcommittees?

A. The committees I would usually become involved with are labeled by number, 42.3 and 42.5 and JC-16.

Q. And at a certain point in time, did you begin to attend JEDEC meetings on a somewhat more regular basis?

A. Yes, I believe somewhere around 1997, I started attending more frequently, maybe through 2000 I was in pretty frequent attendance.

Q. Now, in the mid-1990s when you first began attending JEDEC meetings, did you have any understanding of JEDEC's patent policy?

A. Yes, I did.

Q. And at that time, what was your understanding of JEDEC's patent policy?

A. Well, as I understood it, the patent policy had a few aspects to it. First of all, there was a requirement to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing.

There was also a policy, as I understand, to -- to try to avoid the use of patents, when possible, in defining a standard. There were other aspects of the patent policy as well. Primarily I relied on Terry Walther, our JEDEC representative, to provide guidance on that.

Q. You may have anticipated my next question. How did you, in fact, learn about JEDEC patent policy?

A. Okay, so I guess there's a few sources. Terry Walther, you know, I relied on pretty heavily, as well as our legal department for guidance in that. Also, aspects of the patent policy were posted usually at the beginning of the meeting or discussed at the beginning of the meeting, the requirement to disclose any known patents or applications and the responsibility to avoid the patents. These were included.

There's also I understand a reasonable and nondiscriminatory policy for licensing of a patent if it was used in the standard, but primarily I got my information through those sources.

Q. Now, do you recall a Mr. Jim Townsend at JEDEC meetings?

A. Yes, I do.

Q. And who was he?

A. He was originally with Toshiba. He was -- I

don't recall if he was a committee chairman, but he was very active in the committee, and he helped run some of the different committees and different meetings.

Q. Now, what, if any, role did Mr. Townsend have in developing your understanding of the JEDEC patent policy?

A. He was pretty vocal at the beginning of meetings to state the policy and to clarify if any question came up. He was pretty active in making sure that the policy was enforced.

Q. Now, I think you mentioned a couple of different aspects of the policy. I'd like to focus on the disclosure aspect in particular, and I'd like to ask, focusing again on the mid-1990s time period, what was your understanding of the purpose of the JEDEC disclosure policy?

MR. PERRY: Your Honor, there's no foundation depending upon what "mid-1990s" means. He went to a couple of meetings before 1996 as a Micron rep in a technical support role.

JUDGE McGUIRE: Okay, Mr. Oliver, could you clarify -- give more context as to the time frame you're referring to?

MR. OLIVER: Yes, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, at what point in time did you, in fact, develop an understanding of the JEDEC disclosure policy?

A. I believe I received some guidance from Terry before I attended my first meeting.

Q. And do you recall when you first heard any presentations or any discussions by Mr. Townsend at a JEDEC meeting?

A. I believe he was at the first meeting, the first meeting or two that I attended.

Q. Now, based on your discussions with Mr. Walther and what you may have heard from Mr. Townsend in the first couple of meetings you attended, did you develop at that point an understanding of the purpose of the JEDEC disclosure policy?

A. Yes.

Q. And what was your understanding at that time of the purpose of the JEDEC disclosure policy?

A. My understanding was that the general goal was to develop a standard that was free from encumbrance from patents, and so the purpose to disclose it was to be able to allow the committee to avoid the use of patents and incorporating them in the standard.

Q. Now, again, based on your understanding, did you understand there to be any consequences if a

company failed to disclose a relevant patent or application at a JEDEC meeting?

A. Yes.

Q. What was your understanding of the potential consequences?

A. My understanding was that if they failed to disclose the patent that may relate to the work of the committee and if it was adopted into the standard, that they would forego their right to enforce the patent against the standard.

Q. Now, do you remember any examples of instances in which Micron disclosed relevant patents or applications?

A. Yes, Micron has disclosed -- made patent disclosures over time.

Q. Are you aware of any relevant patents or patent applications that Micron did not disclose at JEDEC meetings?

A. Yes.

Q. And can you please explain that understanding?

A. Sure. I recall an instance, it was around 2000, and we had no intent on enforcing the patent against the standard, and so we were involved with some work of the committee, and we did not disclose that.

Q. Now, with respect to the relevant work of the

committee, do you have an understanding as to whether that work was ever incorporated in a JEDEC standard?

A. On the case where -- the patent we're talking about, is that the question?

Q. Yes.

A. Okay. No, that was not adopted.

Q. Mr. Lee, I'd like to shift now to your understanding of the Rambus architecture in the mid to late 1990s, and let me ask first, are you familiar with Rambus' DRAM architecture?

A. I guess could I get clarification on what you mean by "architecture"?

Q. I guess I would refer to it as the system incorporating the Rambus bus, DRAMs and interface.

A. Okay, yes, so -- and I believe the question was was I familiar?

Q. Yes.

A. Yes.

Q. Now, when did you first become familiar with Rambus' DRAM architecture?

A. I believe I first heard of Rambus and the product, what we call base RDRAM, around the '93 time frame, although I only had peripheral exposure to it at that time, and around 1995, I became more -- more aware of what Rambus was.

Q. Okay. Focusing first on the first awareness you had in 1993 or so, how was it that you first became aware of the Rambus architecture?

A. I'm not sure of the exact -- where the exact exposure started, if you will. I work closely with a gentleman Kevin Ryan, who was doing a similar position as mine, and he was focusing in the graphics segment, and so he was looking at Rambus for use in graphics applications. So, it was through my interaction with him that I became involved with it.

Q. Now, I believe that you also mentioned that in about 1995 or so you came to have a better understanding of Rambus' DRAM architecture. Is that right?

A. That's correct.

Q. And how was it that you came to have a better understanding in the 1995 time period?

A. I believe it was late '95, Rambus was going to come out to Micron, and they wanted to discuss their product with us and their architecture, and I believe the purpose was to see if Micron would license the product and start to develop and build that product. So, in preparation for that meeting, I did a little bit of research, tried to understand -- got on their website and tried to understand a little bit more about

that product.

Q. And did you, in fact, attend the meeting in 1995 with Rambus representatives?

A. Yes.

Q. Now, focusing on the 1995 time period, based on what you learned in the 1993 time period, what you learned in the research that you did for this meeting and what you had learned in this meeting, can you please explain your understanding at that time of the Rambus architecture?

A. Yes. At that point in time, this is what we called base RDRAM, and it was a narrow bus device. We called it narrow meaning there were not very many pins. The command, address and data were all multiplexed onto the same signals. It was a relatively high-speed architecture at that time.

I'm not sure what other kind of details you'd like.

Q. Okay. First of all, you mentioned a narrow bus. Can you please explain what you mean by the term "narrow bus"?

A. Sure. Today typically a computer is 64 bits wide in terms of the data channel. That's the width. And in the case of Rambus, back at that time it was actually a nine -- I believe a nine-bit device. So, it

was rather narrow. It wasn't as wide. And so the idea was to use less pins, run at a higher rate, and multiplex all the information on the same pins, versus what we call a wide bus architecture that uses more data pins.

Q. Okay. And then I believe that you mentioned that command, address and data were all multiplexed. Can you please explain in a little more detail what you mean by that?

A. Sure. All these functions or signals, if you will, shared the same signal line, and the -- whether it was command, address or data depended on the slot in time that you were looking at it on the bus. So, it was time division multiplexed on the same lines.

Q. So, in other words, any individual line may carry command, address or data information at different points in time?

A. That's correct.

Q. Now, focusing again on the late 1995 time period, did you have any understanding about the Rambus clocking scheme?

A. Yes.

Q. Could you please explain your understanding of the Rambus clocking scheme?

A. Sure. They had a clocking scheme that was an

architecture that we sometimes call loop back clock. They had a clock that would run first in one direction, then turn around and then attach to all the DRAMs. I believe at that point in time they were actually connecting to that signal in two places, and they had a -- and they would average the two signals or the arrival of each of those signals in time, and they would use that to drive the internal clock.

Q. Now, you referred to two signals. Were there two clock wires or just a single clock wire?

A. There was one clock wire, and they tapped off of it in two places, if you will. So, they had two separate pins attaching to the same wire at different points of the segment.

Q. And then I believe you said that they then took an average of those two signals. Is that right?

A. That was my understanding.

Q. And did you have an understanding as to why the Rambus -- why the Rambus architecture was taking an average of those two signals?

A. My understanding was that they were -- they were trying to essentially find a midpoint in time between those two signals, and they were trying to get a clock that was traveling in the direction that the data was going.

Q. Now, focusing again on the late 1995 time period, did you have any familiarity with Rambus patents at that time?

A. I did by the time we had the meeting.

Q. Okay. And can you please explain how that came about?

A. Sure. In preparation for the meeting, Jeff Mailloux had asked that we look at what kind of patents that Rambus would have. It was our understanding that Rambus was trying to get us to -- or they wanted us to purchase a license to use that. So, we -- at that time, Kevin Ryan and I took the abstracts, the patent abstracts that they had granted at that time, and we split them up, and we each looked at the abstracts.

Q. Okay, I'll follow up on that in just a minute. Before I do, let me ask you to clarify one point, though.

I believe you said that Rambus was talking to Micron in the context of possibly taking a license.

A. That's correct, for the RDRAM product.

Q. Okay. That, in fact, was my question. Can you explain in a little bit more detail what you understood the potential scope of the license to be?

A. It was my understanding the scope of the license that they were going to come in and offer was

to be able to build and produce and sell that particular device.

Q. That is, the RDRAM device?

A. Correct.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes, go ahead.

MR. OLIVER: I'm sorry, Your Honor, we're having a problem with the computer here.

JUDGE McGUIRE: Go ahead.

(Pause in the proceedings.)

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes, go ahead.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked as RX-629. We've now been able to pull that up on the computer screen as well.

Let me ask you first, Mr. Lee, do you recognize RX-629?

A. Yes.

Q. What is this document?

A. This is a copy of a memo from Jeff Mailloux to myself and others basically asking -- it's the request that I talked about earlier to look at the Rambus abstracts.

Q. Now, who is -- at this time, who was Jeff

Mailloux?

A. I reported to Jeff Mailloux at that time.

Q. And I believe that you testified a moment ago that Mr. Mailloux asked you to look at some patent abstracts. Is that right?

A. That's correct.

Q. Now, I see that RX-629 was actually distributed to eight different individuals here.

Do you see that?

A. Yes.

Q. Was he asking all of these individuals to look at the abstracts or was his request more focused?

MR. PERRY: Calls for speculation about Mr. Mailloux's state of mind.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. At the time that you received this memorandum, what was your understanding of your assignment?

A. It was my understanding that between Kevin Ryan and I, we were to basically respond to the request.

Q. Okay. And I direct your attention to the first sentence that says, "Attached are the abstracts for the patents that have been granted to Rambus, Inc. so far."

Do you see that?

A. Yes.

Q. And then if I can direct your attention to the first sentence of the second paragraph, "Please consider both the quality (is there prior art?) and the breadth (apply to more than just Rambus?) of the patents."

Do you see that?

A. Yes.

Q. Let me ask first, what did you do to follow -- if anything -- to follow up on this memorandum?

A. Kevin and I -- Kevin Ryan and I took the abstracts, and we divided them between ourselves, and then we looked over them, and in one or two cases, I think I had to pull the full patents because I couldn't understand enough by reading the abstract alone.

Q. Do you recall any particular patents that you looked at?

A. We split those up roughly in half, and I think there was, like I said, a couple abstracts that -- that we couldn't tell enough just by reading the abstract what was meant and pulled full patents on those. The one that I remember for sure that I looked at was the clock patent.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-1460. This is a document bearing the caption United States Patent, on the right-hand corner, patent number 5,243,703, and then down at the bottom of the first page, there's a diagram showing, among other elements, clock 1 and clock 2.

Do you recall whether you've seen CX-1460 before?

A. Yes.

Q. Can you please explain when you have seen CX-1460 before?

A. This is one of the patents that I had them pull the full patent on. This is what I'm referring to as the clock patent or the loop back clock, if you will.

Q. And this is one of the patents that you considered in doing the follow-up to Jeff Mailloux's request in 1995?

A. That's correct.

Q. And based on your review of the '703 patent at that time, can you please explain your understanding of the '703 patent at that time?

A. Yeah, my understanding -- you know, to summarize, is they had a -- they were patenting this clocking scheme, which -- what I call this loop back clock. As you can see from the figure, kind of the

figure speaks for itself. And they were using this -- this loop back clock in connection with this multiplexed command/address/data bus for this narrow bus system that was the RDRAM product as I knew it.

Q. Now, looking at the first sentence of this second paragraph of Mr. Mailloux's memorandum, RX-629, in which there's a reference to "is there prior art," did you do any type of an investigation to determine whether there was prior art?

A. Not an investigation as much -- I think he just wanted us to rely on what we already knew based on our experience, whether there was -- whether this was unique or there was other things out there.

Q. Did you consult any other sources other than the abstracts and the patents that you've already discussed?

A. No.

Q. Now, based on your review in 1995, what conclusions did you reach with respect to the breadth of the Rambus patents?

A. The patents -- at least the abstracts that I had reviewed seemed to apply kind of specifically to this bus architecture, to this RDRAM product. There was a couple patents I think relating to tests which didn't seem that interesting to me as well. So, they

seemed to be consistent with what it was that Rambus had put together as this base RDRAM product.

Q. Just to be clear, I think you said that you understood the Rambus patents to be related to "this bus." Can you please explain in a bit more detail what you mean by "this bus"?

A. Yes, once again, it's the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme.

Q. Now, what, if anything, did you do with the conclusions that you reached following this analysis?

A. I traded notes basically with Kevin. I looked at his. He came to similar conclusions. And then reported that information to Jeff Mailloux.

Q. Now, was it after that time that you participated in the meeting with Rambus representatives at Micron?

A. Yes.

Q. And do you recall who participated in that meeting?

A. I recall some of the people. Myself and Kevin was there and Gene Cloud was there. I don't recall if Jeff Mailloux was there for sure or not.

On the Rambus side, I believe Dave Mooring was there and a couple other people.

Q. Now, based on your recollection, what was discussed at that meeting?

A. Rambus went through a presentation I believe and showed us more about what their -- as you referred to -- architecture was, what the Rambus product looked like in a system, what kind of benefits they thought it would be. They shared some implementation -- or some information of existing licensees. So, they basically showed us background information to give us a little more understanding of the product.

Q. Now, did they discuss Rambus patents at that meeting?

A. No. I don't recall.

Q. Was the subject of licensing discussed at that meeting?

A. The subject of licensing was discussed.

Q. Can you please explain your recollection of the discussion of licensing at that meeting?

A. Sure. I'd like to back up a little, if I could and clarify that question on the patents. They may have discussed that their licensing included a license to their patents for this technology. I don't remember any specific discussion on patents in the meeting.

Q. Okay. Well, if I can follow up on that answer, you say that they said that the license would include a

license to their patents. Did they explain for what use -- for what use the license would cover?

MR. PERRY: Your Honor, objection, leading, and it misstates the testimony. He said he can't remember and it may have come up.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, what do you recall with respect to the discussion of licensing at that late 1995 meeting?

A. After we first listened to the technical presentation, and then I believe Gene Cloud asked them what was the nature of the license, you know, and then he asked what kind of fees were involved with the license, and they stated there was some up-front fee and then there was a royalty-based fee.

Q. Now, in the context of those discussions, do you recall any discussion with respect to the potential scope of the license that was being offered?

A. No, I don't.

Q. Now, as a result of this meeting, did Micron sign a license with Rambus?

A. No.

Q. Now, were you involved in any way in the discussions at Micron with respect to whether Micron should take a license from Rambus?

A. Yes.

Q. What is your understanding, if any, about why Micron did not choose to sign the license agreement with Rambus in 1995?

A. There were a few reasons. One, Kevin had done quite a bit of analysis on the graphics system performance and found that the architecture and protocol was a disadvantage, if you will, for system performance relative to some other products we were doing.

Also, we had some information at that time as to the relative increase in die size that a Rambus architecture die would have. I think we got that from Rambus themselves based on some of their earlier licensees.

And then finally, the -- that combined with the royalty for doing the product was unacceptable.

Q. Now, do you know whether Micron signed a license agreement with Rambus at some point after 1995?

A. In '97, we signed a license for the direct RDRAM product.

Q. Do you have any understanding as to why Micron decided to sign a license in 1997?

A. Yes, we were --

MR. PERRY: Your Honor, that's a yes or no, so

that then we can --

JUDGE McGUIRE: Yes, it is.

MR. PERRY: -- object to the next one.

THE WITNESS: I'm sorry?

JUDGE McGUIRE: Sir, just try to answer his question first, and then at that point I'm sure he will follow up.

THE WITNESS: Okay, sure.

BY MR. OLIVER:

Q. Now, what is your understanding, if any, about why Micron signed the license agreement with Rambus in 1997?

A. From a business standpoint, we were pretty much forced to do so. Intel was stating at that time that they were going to use Rambus across most all of their product lines, and so as a DRAM company, we had to provide memory products that would support Intel's platforms, and RDRAM was -- a license was required for direct RDRAM to do that.

Q. Now, what technology did Micron license from Rambus in 1997?

A. Direct RDRAM.

Q. Now, were you involved in any way in the negotiations leading up to the agreement in 1997 between Micron and Rambus?

A. I was involved with providing technical feedback. I wasn't involved in the actual business negotiations.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

THE WITNESS: (Document review.)

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked as RX-829 for identification. Have you had a chance to look through this document?

A. Yes.

Q. Okay. Do you recognize this document?

A. Yes.

Q. What is this document?

A. This is an email from Jeff Mailloux to myself, amongst others. He was -- he was sending to Steve Appleton some negotiating points, if you will, for the license agreement.

Q. Now, if I can direct your attention to the second full paragraph, it's the paragraph that begins, "As a bigger negotiating point," and specifically within that paragraph there's a reference in the third line, "I would imagine that it would also help their IPO."

Do you see that?

A. Yes.

Q. And then if you look -- I believe it's in the eighth line, there is also a reference there to, "If they are planning an IPO."

Do you see that?

A. Yes.

Q. Now, at the time that you received this email in December of 1996, did you have an understanding of those references to an IPO?

A. Yes.

Q. What was your understanding at that time?

A. It was my understanding that Rambus was getting ready to take their company public.

Q. If I could direct your attention to the second page of this document, there's a paragraph, it would be the second full paragraph, "Steve, I anticipate that they will tell you that if we don't go with their 'put all our wood behind one arrow' approach that the NRE price goes back up."

Do you see that?

A. Yes.

Q. Now, this was a statement that was written by Jeff Mailloux. Is that right?

A. Yes.

Q. Let me ask first in that sentence, at the time

that you received this email, did you have an understanding of the term "NRE price"?

A. Yes.

Q. What was your understanding of that term at the time?

A. That's what I called the up-front fee.

Q. In other words, the fee that would be paid by Micron to Rambus for the license?

A. Yes. As I understand, the license had two aspects of fee. There was a fixed up-front fee and then there was a variable fee based on volume.

Q. Now, at the time that you received this email, did you have an understanding of the phrase used by Mr. Mailloux, "put all our wood behind one arrow"?

A. Yes.

Q. What was your understanding of that phrase?

A. He was repeating a phrase that Geoff Tate had used in an email to Steve Appleton, and by that phrase, Geoff Tate was referring to having Micron drop all of our other competing products and support only Rambus.

Q. And at the time you received this email, did you have an understanding of the relationship, if any, between the "put all our wood behind one arrow approach" and the NRE price?

A. Yes.

Q. What was your understanding at that time?

A. From that earlier email from Geoff Tate, they were offering us a discount if we would basically discontinue our other products, other high-speed products, and I think the discount was on the order of $7 million or something like that.

Q. Now, also on the second page immediately underneath that, there's a caption that reads, "Reasons for lower royalty."

Do you see that?

A. Yes.

Q. Before we go any further, let me ask based on your understanding at the time that you received this email in December of 1996, what was your understanding at that time about what royalty rate Rambus was offering to Micron?

A. It was 2 percent.

Q. Again, based on your understanding at that time, what was your understanding of what that 2 percent royalty would apply to?

A. It would apply to the direct RDRAM product.

Q. In the late 1996 and early 1997 time frame, did you ever hear anything about Rambus asking for royalty on SDRAMs?

A. No.

Q. Now, if I could direct your attention within the first paragraph underneath the caption that I read to you, it's the first paragraph underneath the caption "Reasons for lower royalty."

In fact, actually, let me take a step back here. Let me just ask you generally about the three paragraphs appearing underneath that caption. Do you see they're numbered 1, 2 and 3?

A. Yes.

Q. And let me ask generally, at the time that you received this email, did you have an understanding of the contents of those three paragraphs?

A. Yes.

Q. In general terms, what was your understanding of the contents of those three paragraphs?

A. Jeff was trying to come up with some negotiating points for positioning for Steve to try to negotiate a lower royalty from Rambus.

Q. If I could then direct your attention to paragraph number 1, and within paragraph number 1, starting I believe in the sixth line, the sentence, "From our research, we think many Rambus patents read on prior art or other patents."

Do you see that?

A. Yes.

Q. Now, at the time that you received this email, focusing again on your understanding, did you believe that Rambus patents read on prior art?

A. I wouldn't characterize it that way.

Q. Can you please explain your understanding?

A. Yeah, my understanding is I believe Jeff took strictly from the feedback Kevin and I had given him from the patent abstracts and the couple patents we had looked at, that some of the abstracts looked familiar, didn't seem that novel. I think he extrapolated on that statement.

Q. Between the time in late 1995 when you looked at the Rambus patent applications and the date of this email in December 1996, had you conducted any other research into prior art in connection with Rambus patents?

A. No.

Q. Were you personally aware of any other research done within Micron with respect to any research into prior art relating to Rambus patents?

A. No.

Q. I'd like turn next, if we could, to the topic of SyncLink. Now, Mr. Lee, are you familiar with the term "SyncLink"?

A. Yes.

Q. And how did you first become familiar with SyncLink?

A. My first familiarity came from Terry Walther, who had attended some early meetings.

Q. And I'd like to have you explain, if you could, briefly your understanding of the SyncLink architecture.

A. Okay, so can I assume that the architecture is the same terminology used earlier?

Q. Yes, thank you, it would refer to the bus structure, the devices and the interface.

A. Okay. SyncLink architecture was kind of a combination between the narrow bus and wide bus. It was in between the width of a DDR bus and that of a Rambus, and it was a source-synchronous design that used strobes. It used what we call verniers for a thing we call leveling the bus by moving around timing of the data onto the bus.

Is that the kind of information you want?

Q. Yes, thank you.

Now, do you have an understanding of when Micron began work with respect to SyncLink?

A. Yes, I -- yes.

Q. Okay. And what is your understanding?

A. I believe Terry started attending meetings I

think it was in late '95, and then we started getting more involved in '96, Kevin Ryan and myself.

Q. And that was, in fact, the next question. At some point did you personally become more involved with SyncLink?

A. Yes.

Q. And when did that occur?

A. It was sometime in the first half of '96.

Q. Now, you've discussed in general terms the -- what I referred to as the SyncLink architecture. Based on your understanding in the 1996 time frame, were there any differences between the Rambus architecture, as you understood it, and the SyncLink architecture?

A. Yes, there were many.

Q. Could you please explain your understanding of those differences?

A. Sure. In the case of Rambus, they used this loop back clock scheme and forwarded the clock with the signal. SyncLink used, instead of a loop back clock, they used a source-synchronous design, which used data strobes, and the data strobes traveled in either direction on the same signal, unlike the Rambus, which always -- the clock moved in one direction.

SyncLink used a -- what we call an SL I/O, which is -- I'm getting into some technical terms here,

but it's a push/pull driver scheme. Rambus used this open drain driver. They're quite a bit different.

SyncLink used these verniers for aligning when data would be put onto the bus. Rambus didn't do anything like that. They relied on the loop back clock for providing the timing of when to put the data on the bus.

There were many differences in the protocol and the bank organization and things like that as well.

Q. Now, I believe you also referred to SyncLink as somewhere between Rambus and -- and SDRAMs in terms of its bus structure.

A. Yes.

Q. Was the SyncLink bus structure multiplexed?

A. No, the SyncLink bus structure just had command/address multiplexed. Data was a separate bus.

Q. So, in other words, it was multiplexed with respect to the command and address buses but not with respect to the data bus. Is that right?

A. The command and address were in the same grouping. I don't recall what the time slot placement of the SLDRAM protocol was at this time, but the data was on a completely separate bus.

Q. Now, was SyncLink a packetized system?

A. The -- I would call the command/address

packetized.

Q. Now, are you familiar with the various features in the JEDEC SDRAM standard?

A. Yes.

Q. And are you familiar with features in the JEDEC DDR SDRAM standard?

A. Yes.

Q. And I'd like to focus first, if we could, on programmable CAS latency and programmable burst length. Are you familiar with those features?

A. Yes.

Q. Now, based on your understanding, does the JEDEC SDRAM standard require programmable CAS latency and programmable burst length?

A. Yes.

Q. And does the JEDEC DDR standard require programmable CAS latency and programmable burst length?

A. Yes.

Q. Mr. Lee, are you familiar with the term "SDRAM-Lite"?

A. Yes, I am.

Q. Can you -- actually, let me ask first, when did you first become familiar with SDRAM-Lite?

A. I believe the time frame was roughly late '95.

Q. Can you please explain your understanding of

what SDRAM-Lite was?

A. Sure. SDRAM-Lite was an attempt to create a simpler SDRAM that would be cheaper to manufacture, and so it had a reduced set of features.

Q. When you say a reduced set of features, do you recall any particular features that were reduced in SDRAM-Lite?

A. Yes. They were proposing to go to a single fixed burst length and a single fixed CAS latency.

Q. Now, based on your understanding in the late 1995 and early 1996 time frame, what, if any, were the advantages of an SDRAM-Lite?

A. The advantages would be it would be faster to design and it would be cheaper to produce and test.

Q. Can you please explain your understanding at that time of why SDRAM-Lite would be faster to design?

A. It was simpler for us. We didn't have to design in different modes and consider all the combinations of burst lengths and CAS latencies for the timing data path.

Q. And can you please explain your understanding at that time of why SDRAM-Lite would be cheaper to produce?

A. Yes, our test times would be reduced for similar reasons. We would not have to test against

different burst lengths and CAS latencies and repeat the entire test for them.

Q. Based on your understanding at that time, what, if any, were the disadvantages of SDRAM-Lite?

A. I don't think there were any fundamental disadvantages other than at that time there was still some discussion as to which was the best burst length and which was the best CAS latency.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked JX-29. I'll give you just a moment to look at it.

A. (Document review.)

Q. Mr. Lee, I've handed you JX-29, which is a set of minutes from the interim meeting of JC-42.3 in January of 1996.

Do you recognize this document?

A. Yes.

Q. Were you at this meeting?

A. Yes.

Q. Could you please turn to page 13 of JX-29. This is a page that reads in the upper right-hand corner, "Attachment E," and underneath that, "Results of SDRAM 'Lite' survey ballot."

Do you see that?

A. Yes.

Q. Now, were you present at the JEDEC meeting when this item was discussed?

A. Yes.

Q. At the time, did you have an understanding of this item?

A. Yes.

Q. Can you please explain in general terms what was being discussed in connection with this Attachment E?

A. Sure. We were trying to decide which features an SDRAM-Lite should have, and there was also consensus on particular features, and we were trying to decide -- there were some that were still undecided, and they were trying to resolve that.

Q. If I could direct your attention to the -- to the table appearing in about the middle of this page, it's the upper of the two tables. The first line item within that table is "single write."

Do you see that table?

A. Yes.

Q. Can you please explain what was being summarized in that table?

A. In that table, we were looking at a variety of

features, burst length, CAS latency, as listed here, all bank precharge, and those were items that we had already had some agreement on and were agreed that that would be part of the SDRAM-Lite device; or in some cases, they were already items that we rejected, and it was agreed that we rejected them.

Q. Okay. If I could direct your attention to the caption for that table, it reads "Item," then "Yes, no" and "Don't Care."

When the caption reads "yes," what does that mean?

A. That means that you agree to include the feature in SDRAM-Lite.

Q. And if I could direct your attention to the fourth line from the bottom, "CAS latency equals 3," do you see that?

A. Yes.

Q. And what was your understanding at the time as to what, if any, consensus had been reached with respect to a CAS latency of three?

A. It was our understanding that there was a consensus to use CAS latency three for SDRAM-Lite.

Q. And then if I could direct your attention to the last two lines, "burst length equals 8" and "burst length equals full page," for one, on the "No" column,

it's unanimous, and the "No" column for full page is 14.

Can you please explain your understanding at this time, if any, as to what consensus, if any, had been reached with respect to the use of those two items?

A. The consensus was to exclude those features from the device.

Q. And above that, there's a reference to "burst length equals 4." What was your understanding at the time as to whether there was any consensus with respect to a burst length of four?

A. Yeah, the consensus was to include burst length four in SDRAM-Lite.

Q. Now, if I could direct your attention to the table appearing at the bottom of page 13, what was your understanding at the time of what was reflected in this table?

A. These were the items that were still under discussion, and the discussion was taking place as to whether these should be included in the SDRAM-Lite device.

Q. Then the first line there reads, "CAS latency equals 2."

Do you see that?

A. Yes.

Q. What was your understanding at the time as to whether there was any consensus with respect to a CAS latency of two?

A. There wasn't a consensus at this time. There was some -- there was general discussion that we didn't want to include other CAS latencies or burst lengths either into this device since it was a "lite" device.

Q. Based on your understanding at the time, what were the implications of a "no" vote for CAS latency of two?

A. That means that you did not want to include it on the device.

Q. And in that circumstance, based on your understanding at the time, how would CAS latency have been determined?

A. At that time, CAS latency would have been determined the way -- I'm sorry, let me ask a question to clarify.

You mean if CAS latency two had been included?

Q. No, my question was if CAS latency two had not been included.

A. Okay, in that case, then the CAS latency was fixed, so it was set. There was no need to control it.

Q. And based on your understanding at the time,

what, if any, were the implications of a vote in favor of CAS latency of two?

A. If that became consensus, then we would have to have more than one CAS latency.

Q. And if I could direct your attention to two references to burst length underneath that, "burst length equals 1" and "burst length equals 2," again, what was your understanding at the time as to whether there was any consensus with respect to use of those burst lengths?

A. It was similar in that we hadn't received consensus at that time, and it was similar in that there was general discussions to try to avoid adding other burst lengths or CAS latencies on a "lite" device.

Q. Now, would this be similar in that the implications of a "no" vote would be that burst length might be fixed?

A. If -- if you had voted "no" to the burst length proposals, yes, then the result would be a fixed burst length.

Q. Now, what, if any, was your understanding of Micron's position at the time with respect to SDRAM-Lite?

A. We were in support of SDRAM-Lite. We preferred

it.

Q. And did you do any evaluation of SDRAM-Lite at that time?

A. Yes, I worked with Kevin Ryan, and we did some evaluation work with the design teams to establish our position.

Q. Can you please explain why you were in favor of SDRAM-Lite?

A. Sure. It was simpler for us. It was -- it would be faster for design. We felt it would be cheaper to produce and cheaper to test. Our feedback from the test group and design was they much preferred the "lite" device over a full-feature device.

Q. Now, based on your assessment at that time, was use of a fixed CAS latency acceptable from a technical point of view?

A. Yes.

Q. Again, based on your assessment at that time, was use of fixed CAS latency acceptable from a cost perspective?

A. Yes.

Q. Based on your assessment at that time, was use of fixed burst length acceptable from a technical point of view?

A. Yes.

Q. And based on your assessment at the time, was use of fixed burst length acceptable from a cost perspective?

A. Yes.

Q. Now, what, if anything, eventually happened with respect to the SDRAM-Lite proposal?

A. The proposal eventually lost support, and it was abandoned.

Q. Can you please explain your understanding of why?

A. Sure. There were a couple issues going on. First of all, it had taken quite some time, the SDRAM specification process, and there was becoming some frustration that the process was taking too long.

And second, some of our concerns had to do with the cost of implementing the full-feature device, as we called it, and over time, as we did more engineering work, more data was brought in that indicated, although there was some cost adder, it was lower than we thought, and that combined with the fact that the committee was getting frustrated that we didn't have a standard yet, essentially we capitulated and agreed to drop it and go with the full-feature device.

Q. Now, were you involved in any discussions within Micron with respect to whether Micron should

stop supporting SDRAM-Lite?

A. Yes.

Q. Can you please explain in a little more detail what role, if any, the concern about the delay in the standard had within those discussions within Micron?

A. Sure. Our business is -- tends to be seasonal, and so there is particular increased demand towards back-to-school and Christmas, and we had certain customers that wanted to be able to use the designed SDRAM, and so if we could not get standardized in time, it would delay their product, and therefore, we wouldn't be offering new memory technology in a suitable time frame. So, we agreed in the interests of schedule to just go ahead and accept the full-feature proposal.

Q. And in connection with the internal discussions within Micron, did you recommend that Micron go ahead and accept the full-feature device?

A. I think it was a consensus decision that involved myself, Terry Walther, Kevin Ryan, and I think we agreed that based on the momentum of the committee at this point and the data that we had seen so far, that it was probably better if we just pursued the full-feature device.

Q. Now, if Rambus had disclosed while it was a

member of JEDEC that it would pursue patent rights over use of programmable CAS latency and burst length, what effect, if any, would that have had on your recommendation within Micron?

A. We would have opposed the full-feature device, and we would have increased our support on the SDRAM-Lite device.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-260. It bears the caption underneath the JEDEC heading Committee Survey Ballot and a date in the upper right-hand corner, October 30, 1995.

Mr. Lee, do you recognize CX-260?

A. Yes.

Q. What is this document?

A. This is a JEDEC survey ballot for future synchronous DRAM features, which later became known as DDR.

Q. Now, approximately when did you first see this document?

A. It was late '95. I believe it was -- information was brought back from a meeting and then discussed internally at Micron.

Q. I believe you said the information was discussed internally within Micron. What, if any, role did you have within those discussions?

A. I was involved in the discussions and provided some technical input and recommendations.

Q. If I could ask you to turn, please, to page 9 of CX-260, can you please explain in general terms what was being set forth on page 9 of CX-260?

A. Yes. They were taking votes on what other CAS latencies should be supported on the future SDRAM device.

Q. Now, did the discussion of the questions on page 9 explain how CAS latency would be determined in the future SDRAM standard?

MR. PERRY: Your Honor, that's vague as to whether he's talking about the Micron internal discussions or just asking him to interpret the document.

MR. OLIVER: I'll withdraw the question, Your Honor.

JUDGE McGUIRE: Go ahead.

BY MR. OLIVER:

Q. Based on your understanding at the time that you were reviewing and discussing this document in late 1995, did you understand that page 9 of CX-260

explicitly explained how CAS latency would be determined in a future SDRAM standard?

A. Yes.

Q. And what was your understanding of how page 9 proposed to determine the CAS latency of the future SDRAM standard?

A. The last sentence of the paragraph discusses the mode register, so it would be programmable through the mode register just like the SDRAM device, and specifically called out that there were fields available for that.

Q. Now, following the survey ballot that we just looked at, were you familiar with JEDEC work towards the future SDRAM standard or what became the DDR SDRAM standard?

MR. PERRY: Objection, it's leading and compound.

MR. OLIVER: Your Honor, I'm simply trying to find -- establish a basis in order to --

JUDGE McGUIRE: Overruled. I'll hear the question.

MR. PERRY: Your Honor, just to be specific, the question assumes that this survey ballot became the later DDR standard, and that's leading.

MR. OLIVER: Your Honor, I'll withdraw and

rephrase the question.

JUDGE McGUIRE: Okay, restate it.

BY MR. OLIVER:

Q. After late 1995, were you involved in any of the work at JEDEC directed towards a future SDRAM standard or DDR SDRAM standard?

A. Yes.

Q. Based on your understanding and your experience at JEDEC, what was your understanding of when JEDEC began work on what became the DDR SDRAM standard?

A. I'm sorry, I'm not --

MR. PERRY: Lacks foundation, Your Honor. There's no foundation for when he was actually at JEDEC. He went to a couple of meetings before this point in time.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, if I could then simply ask, based on your involvement in JEDEC, did you have any understanding as to whether JEDEC began work on what became the future SDRAM or DDR SDRAM standard before you began attending on a more regular basis in 1996?

A. Yes.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked JX-40. It's a set of minutes from the September 1997 42.3 subcommittee meeting in Taipei, Taiwan.

Mr. Lee, do you recognize JX-40?

A. Yes.

Q. Did you attend this JEDEC meeting?

A. No.

Q. Did you see this set of minutes at some time around or shortly after September of 1997?

A. Yes.

Q. Can you please explain the context in which you saw the minutes in late 1997?

A. Yes. Nobody from Micron attended this meeting, so we received the minutes and had to go through the minutes to understand what had transpired in our absence.

Q. And did you personally go through these minutes?

A. Yes.

Q. If I could ask you, please, to turn to page 7 of JX-40, and I'd like to direct your attention to the paragraph appearing underneath heading 8.1 towards the bottom of page 7. It's the paragraph that carries over to the top of page 8. The caption reads,

"JC-42.3-97-62B, DDR Mode Register Modification Item 815.02C."

Do you see that paragraph?

A. Yes.

Q. Is this one of the paragraphs that you reviewed in late 1997 when you reviewed these minutes?

A. Yes.

Q. At the time you reviewed them, did you have an understanding of this paragraph?

A. Yes.

Q. Could you please explain your understanding as of late 1997 of what was reflected in this paragraph?

A. Sure. They voted to approve the DDR mode register settings, and this aspect of the mode register settings was centered around CAS latency.

Q. And based on this proposal, how was CAS latency to be determined in the DDR SDRAM standard?

A. It was to be determined through mode register setting, it was programmable through the mode register, and the specific values in the mode register were agreed upon at this time.

Q. Did this represent adoption of programmable CAS latency in the DDR SDRAM standard?

A. Yes.

MR. OLIVER: Your Honor, I'm about to switch to

a new topic. I can either continue or we can take a break, as you wish.

JUDGE McGUIRE: Let's take a ten-minute break here, and then we'll return.

MR. OLIVER: Thank you, Your Honor.

JUDGE McGUIRE: Off the record.

(A brief recess was taken.)

JUDGE McGUIRE: Let's go back on the record.

Mr. Oliver, you may proceed.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, during the break we've set up a tablet of paper just in case at any point in time you do wish to use that, please let me know, and please feel free to do so.

Mr. Lee, are you familiar with on-chip DLL as used in the JEDEC DDR SDRAM standard?

A. Yes.

Q. How have you become familiar with the on-chip DLL technology?

A. In late '95, we were trying to determine whether we needed to include that feature for -- as part of that survey ballot that we discussed earlier.

Q. Now, does JEDEC's DDR SDRAM standard require an inclusion of an on-chip DLL?

MR. PERRY: Objection, Your Honor, calls for expert opinion testimony. It's not limited to his understanding.

JUDGE McGUIRE: Sustained.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, based on -- actually, let me withdraw that.

Mr. Lee, were you involved in JEDEC work leading up to the adoption of the DDR SDRAM standard?

A. Yes.

Q. And do you have an understanding of the contents of the JEDEC DDR SDRAM standard?

A. Yes.

Q. Based on your understanding, does the JEDEC DDR SDRAM standard require the inclusion of on-chip DLL?

A. Yes.

Q. Now, focusing on the 1996 and 1997 time period in particular, were you involved in evaluating whether Micron should support using on-chip DLL in the JEDEC DDR SDRAM standard?

A. Yes, I was.

Q. Can you please explain what your involvement was within Micron?

A. Sure. Kevin and I worked together to try to

establish what would be necessary in terms of a clocking and data capture scheme, and DLL was involved in that consideration. So, we had to decide whether we felt it was necessary or whether we preferred it or not.

Q. You've mentioned a Mr. Kevin Ryan. Actually, I probably should have asked this earlier, because you have mentioned him a couple times now. Who is Mr. Kevin Ryan?

A. Kevin Ryan works for Micron. During this time period, we worked side by side on the same kind of projects, although we took on different aspects of the projects, so we were essentially a team. So, we worked together on most things.

Q. And is he now part of the group that reports to you within Micron?

A. Correct.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked JX-41. These are the minutes of the JC-42.3 subcommittee meeting in December of 1997 in Tempe, Arizona.

Do you recognize this document?

A. Yes.

Q. Were you present at this 42.3 committee meeting?

A. No.

Q. If I could ask you to turn within JX-41, please, to page 107. That's a document that in the left-hand corner reads, "From 921, Attachment T," and across the top it reads, "16M DDR SGRAM," and in the bottom right-hand corner, reads "Micron."

Mr. Lee, are you familiar with this document?

A. Yes.

Q. Let me ask you, if you could, to flip through a few pages and just identify the pages that belong to this Micron presentation.

A. Okay.

Q. Can you please identify which pages belong together as part of this presentation?

A. I'm sorry, the question was again?

Q. Is it page 107 through page 115, are those the pages that belong together as part of this presentation?

A. Yes.

Q. Now, focusing then on pages 107 through 115, how did you become familiar with this document?

A. I believe I reviewed it with Kevin before he

prepared it for the meeting.

Q. In other words, you reviewed it with him in the late 1997 time frame?

A. Yes, I believe that's correct.

Q. And did you provide any feedback to Mr. Ryan at that time?

A. I don't recall if there was specific feedback. It was our normal habit to show each other our -- what we planned for a presentation prior to a meeting to make edits, and I don't remember if I made edits on this particular presentation or not.

Q. Did you understand this presentation at the time you reviewed it?

A. Yes.

Q. Did you agree with the contents of the presentation at the time you reviewed it?

A. Yes.

Q. If I could ask you to turn, please, to page 114. Could you please explain just in general terms what is being set forth on this page?

A. Yes. Kevin was trying to explain the relative merits and disadvantages of including a DLL on chip.

Q. If I could direct your attention to the first bullet point, Disadvantages of DLL, and then underneath that, it reads, "Start-up time after power-up, after

exiting self-refresh, and after changing operating frequency."

Do you see that?

A. Yes.

Q. Can you please explain your understanding at the time that you reviewed this of that bullet point?

A. Sure. DLL, the way it works, it takes a certain amount of time to lock, what we call lock. You can consider it like a warm-up time for a car or something. And after certain operations or upon power-up, it took a certain amount of time before DLL was guaranteed to be accurate.

Q. And if I could direct your attention to the next bullet point, "Power-consumption," could you please explain your understanding at the time you reviewed this document of the disadvantage of DLL with respect to power consumption?

A. Yes, the DLL circuitry used current and therefore consumed power.

Q. The next bullet point reads, "Jitter."

Could you please explain your understanding at the time you reviewed this of why that was a disadvantage with respect to DLL?

A. Yes, I think the simple way to look at jitter is it's the relative accuracy of the DLL, that it --

rather than putting out something at a specific period of time, it may meander about that time.

Q. The next bullet point reads, "Design time/uncertainty."

Can you please explain your understanding at that time of why that was a disadvantage of the DLL?

A. Yes, at that time there was concerns about the amount of time it would take to get a DLL designed right in the DRAM process, which was not really optimized for this type of circuit, and some uncertainty on the amount of time it would also take to debug it and get it to where it's ready for production.

Q. And the then final bullet point under Disadvantages of DLL reads, "Cost."

Could you please explain your understanding at the time of that bullet point?

A. Yes, at that time our understanding is that, of course, the DLL circuitry increased the die size and had some increased die cost, but also there was concern about how to test a part with a DLL at that time.

Q. Can you please explain what the concerns were with respect to how to test a part with a DLL at that time?

A. Yeah, one of our concerns was whether our testers, our DRAM testers, would do a good job on that.

Another concern was that we felt we would have to test it with the DLL off and the DLL on, both, thus increasing the test time.

Q. If I could direct your attention to the next major bullet point, Advantages of DLL, and underneath that it reads, "Reduces bus turnaround time when different devices will be driving."

Could you please explain your understanding at the time of that advantage of a DLL?

A. Sure. The DLL used in -- as proposed for this device would reduce the uncertainty in the amount of time when data would be present on the bus from the device. So, by incorporating the DLL, you could reduce that uncertainty in time.

Q. The next sub-bullet point under Advantages reads, "Eases DQS preamble timing."

Could you please explain your understanding at the time of what that bullet point referred to?

A. Sure. This is somewhat related to the bullet above it, but it had to do with the strobe signal and when you were getting ready to transfer operations from one device to a different device, there was a strobe signal that you had to release from the bus and have the new device drive the strobe signal, and the fact that it was more certain in time in which data would be

present on the bus helped ease this timing hand-off problem.

Q. Then if I could direct your attention to the final bullet point, it reads, "The DLL does not simplify data valid/capture timing."

What was your understanding at the time of what was meant by that bullet point?

A. In this case they were using a strobe signal, and they -- and there was some confusion I think within the committee on the -- some of the technical aspects of the DLL, and in the pages prior, I think Kevin goes through and explains data-to-data strobe skew and how it affects data capture timing, and he I think proves that the DLL itself doesn't necessarily improve the data capture timing, because they're using the strobe to capture the data.

Q. Now, based on your understanding at the time, did you recommend that Micron support including on-chip DLL in the JEDEC DDR SDRAM standard?

A. No.

Q. Why not?

A. We preferred not to use the DLL. We thought we could accomplish the timing and the data capture through other techniques, and we thought including it would have all these disadvantages that we mentioned

here. So, we preferred the simpler, lower-cost solution.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked as CX-2713. This is an email from T. Walther dated November 14, 1997 to a number of people. Do you see that you are included on the list of recipients?

A. Yes.

Q. Mr. Lee, do you recognize this document?

A. Yes.

Q. I'm sorry, did you want a moment to look at it?

A. Yeah, if I could.

Q. Sure.

A. (Document review.) Okay.

Q. Do you recall receiving this document in around November of 1997?

A. I recall reviewing this, yes.

Q. Now, do you see the top from/sent/to/subject box says it's from T. Walther to a number of individuals, including yourself, and then underneath that it reads, "Original Message," and it's from Ken McGhee to T. Walther?

Do you see that?

A. Yes.

Q. What was your understanding at the time you received the email of what that represented?

A. This represented some comments of some items that were in discussion at JEDEC at that time. It represented Micron's feedback on those issues. I believe Terry Walther had sent it to Ken McGhee, who sent it out to the JEDEC members, who then forwarded it back to us.

Q. If I could ask you to turn, please, to the second page, the second paragraph reads, "Comments on JC-42.3-97-128A."

Do you see that?

A. Yes.

Q. Now, did that refer to a JEDEC ballot?

A. Yes.

Q. Then underneath that, paragraph number 1 reads, "The role of the DLL has been diminished to the point where the DLL now has more disadvantages than advantages."

Do you see that?

A. Yes.

Q. And then underneath that, there's a list of disadvantages of DLL?

A. Yes.

Q. Based on your understanding at the time that you received this, are those disadvantages essentially the same ones that we looked at a moment ago in the presentation prepared by Mr. Kevin Ryan?

A. Yes, they are.

Q. Then underneath that, there's a reference to advantage of DLL.

Do you see that?

A. Yes.

Q. Now, is that similar to the advantages identified in the presentation prepared by Mr. Kevin Ryan?

A. It's similar, but I believe he's added some I guess -- some new information about how it specifically affects data capture in the controller side.

Q. Can you please explain your understanding at the time of what additional information was added at the time?

A. Yes, he specifically identifies that it may be possible that if a DLL is used, you might be able to eliminate a FIFO of circuitry from the controller for doing data capture versus the scenario if you didn't have a DLL, he felt that was necessary to be included.

Q. What is FIFO circuitry?

A. It stands for first-in/first-out. It's kind of

a buffer, and it's temporary memory where data comes in on a first-come basis and out on a first-serve basis.

Q. Based on your understanding, did the inclusion of any of this additional information change Micron's position with respect to whether on-chip PLL or DLL should be included in the DDR SDRAM standard?

A. No.

Q. And what position -- based on your understanding, what position was Micron advocating within JEDEC at this time?

A. Well, we still preferred to try to eliminate the DLL.

Q. Now, in the 1996 and 1997 time frame, based on your understanding, did Micron ever propose an alternative within JEDEC to the use of on-chip PLL/DLL?

A. Yes.

Q. And based on your understanding, who gave that presentation?

A. Kevin Ryan.

Q. Mr. Lee, if I could ask you to find JX-29 which I handed to you earlier this morning. These are minutes of the interim meeting of the JC-42.3 committee of January of '96.

Do you have JX-29?

A. Yes.

Q. By the way, were you at the January 1996 interim meeting of the 42.3 committee?

A. I believe I was.

Q. I'd ask you to turn to the second page, under the list of others present, about five names down.

A. Yes.

Q. Does that refresh your recollection as to whether you were present at this meeting?

A. Yes.

Q. If I could ask you to turn, please, to page 17 of JX-29, and if I could ask you to flip quickly through pages 17 through 22, this is a document that -- handwritten it appears to be Attachment F, and the top reads, "Future SDRAM - Clock Issues," and it has a Micron logo in the lower right-hand corner.

Mr. Lee, do you recognize the document appearing at pages 17 through 22 of JX-29?

A. Yes.

Q. What is this document?

A. This is a presentation by Kevin Ryan addressing alternatives to DLL for DDR, in which case he was proposing using echo clocks is what we were calling them.

Q. Now, did you review this document before Mr. Ryan made the presentation?

A. Yes.

Q. Did you provide any feedback on the document?

A. Yeah, I believe I did.

Q. If I could ask you to turn, please, to page 18, this is a page under the subcaption PLL/DLL Circuits, has certain bullet points, including added cost and complexity, should avoid replicating these circuits in every DRAM in the system, and under that certain recommendations.

Can you please explain just in general terms your understanding at the time of what was being reflected on this page?

A. He was expressing some disadvantages of having DLL on chip and that it would increase costs and that you would have to have this increased cost among many parts in the system, every DRAM. So, he was providing an alternate recommendation.

Q. If I could ask you to turn, please, to page 20, and there under the caption of Echo Clocks, I believe you referred to a moment ago, is the first bullet point, "There are several sources of variation of data valid windows."

Do you see that?

A. Yes.

Q. And then under that, there's five sub-bullet

points.

I'm wondering if you could explain in general terms -- and please feel free to use the pad of paper here if it helps to do so -- but could you please explain in general terms what the problem is, if you will, that Mr. Ryan was attempting to describe here?

A. Okay, I'll start just generally. When we're trying to get a capture on a controller, there's loop timing from when we send information out to when data eventually comes back, and we need to have some certain period of time in which we can accurately capture that data, and the challenge with that is that there's several components of delay in the system that occur.

Some of those delay components are what we call static in that they're fixed for a given system, and other ones are dynamic in that they move with voltage or temperature. So, the problem is, as we get to higher clock rates, this percentage of timing variation due to either static or dynamic timing variations becomes a larger percentage of the clock period, makes it more difficult to capture data.

So, what we do is we have a few tools -- there's actually several ways to improve this problem. A few of the tools we like to use, probably the most are to use verniers or variable delay elements to

compensate for these changes in time, or we can use a DLL to compensate for the component of timing variation that's due just by the chip itself, and also we do things like run source-synchronous -- run strobes so that we've converted the timing from an absolute timing problem to that of a relative timing problem, the timing difference between two signals as opposed to the absolute timing variation.

And then Kevin identified -- he kind of broke down all the different possible timing variations into several categories and described -- I think describes how you can address those different categories of timing variation. So, beyond that, I'd probably have to use the board to show you what those different categories are.

Q. Okay. Well, why don't we take them one at a time, and let me ask you first what your understanding was at the time of what Mr. Ryan depicted here by clock skew to DRAMs, and if it helps you to use the pad of paper here to help explain that, please feel free to do so.

A. Okay, the -- I assume you are going to have me go through all of them?

Q. Yes. Is it easier to --

A. Then I'll use the pad.

Q. Okay.

A. I don't know how that works for them to see or --

MR. PERRY: It's fine.

MR. OLIVER: Mr. Perry can stand next to me if he wishes to do so.

THE WITNESS: So, the clock scheme in the system will have a controller, and there will be -- I'll draw it first as a module, and there will be several DRAMs on the module, and there might be -- because of the number of DRAMs, there might be multiple clocks, different clocks used for different DRAMs. So, if these DRAMs receive this clock and some other DRAMs receive a different clock, there may be a difference in arrival time of this clock to this clock. So, that's what we're calling clock skew to the DRAMs. I'm just going to -- I'll put a 1 next to the first one.

Then there's -- then the DRAMs, after receiving a clock, they will eventually drive data out of the DRAM device back to the controller for data capture, and there's multiple data lines. There may be eight data lines, for example, from each chip, and so there's on-chip skew of the DRAM, which means that each one of these output pins ideally would fire at the identical point in time, but there's some differences and delays

inside the chip, so they actually fire at slightly different times. So, there's skew. Whenever we talk about skew, we're talking about variation, time variation. So, there's skew across these pins on the chip itself. So, I'll write 2 here.

Then, there's also what we call chip-to-chip skew. Whatever the skew is for this chip, there's also -- there may be a difference in what the skew is from this chip. So, when we're capturing the data bus, all these DRAMs are driving. So, I have got to capture this entire word. So, this -- the output delay of this chip might be slightly different from this chip. So, we'll call that -- and that's just due to the variations of one chip to the other. We'll call that 3.

Can I write on this?

BY MR. OLIVER:

Q. Yes.

A. And then he refers to a component called data path skew after the DRAMs, and that has to do with variations in delay of flight time versus this data path to this data path or this DQ to this DQ. Some of that is just physical length differences in the board routing. Some of this has to do with characteristics of the way -- of the board itself due to other things

going on on the board, such as power supply, noise and cross-talk. So, that's what we'll call 4.

And then the last component he's talking about has to do with variations due to differences in system loading. There might be -- they might be trying to capture something from one module versus a different module, and they might have longer lines in this case, so there's longer distances, or there might be different clock loading because of the number of devices on a module. So, I'll just put that as 5. So, that has to do with changes in timing that occur due to having different loading -- different amounts of DRAMs populating the system.

Is that -- is that an adequate explanation?

Q. I believe so.

Your Honor, do you have any follow-up questions?

JUDGE McGUIRE: No, go ahead.

MR. OLIVER: Okay, I would like to mark this as a demonstrative. I don't know where we stand in the numbers at this point.

JUDGE McGUIRE: Does anyone keep track of that? I know it's about 110 or something.

MR. PERRY: We think it's 117.

JUDGE McGUIRE: All right, let's mark it as

that, and if it changes, we will note that for the record. Let's mark it as DX-117.

MR. OLIVER: May I approach it, Your Honor?

JUDGE McGUIRE: Yes.

(DX Exhibit Number 117 was marked for identification.)

BY MR. OLIVER:

Q. Okay, thank you, Mr. Lee.

Now, Mr. Lee, based on your understanding in the 1996 to 1997 time period with reference to the work that JEDEC was doing directed towards what became the DDR SDRAM standard, was it -- in your understanding, was it necessary to fully correct for the data capture problem that you've illustrated in DX-117?

A. I'm not sure I understand what you mean by "fully correct."

Q. Was it -- was it necessary to ensure that the data was perfectly aligned with the system clock?

A. No.

Q. Can you please explain why not?

A. The -- for a given data rate of a system, there will be a window on which all the data from all the buses or all the DQs that you're looking at would be valid and accurate.

In other words, if you capture the data at that

time, they would all be correct. And that window has a certain size depending on the amounts of these timing uncertainties, and the greater uncertainty there is, the smaller that window gets.

So, what we just had to do is make sure that that window was large enough relative to the clock or whatever we're going to use to capture the data such that the set-up and hold time of the DRAM was met.

In other words, the DRAM or the controller in this case could tolerate a certain size window, and as long as it's at least as big as that window, we could accurately capture data.

Q. Now, if I could ask you to turn back to the five components of the -- of variation of data valid windows that Mr. Ryan outlined on page 20 of JX-29, and focusing again on your understanding in the 1996 time frame, what was your understanding of which, if any, of these five components would be corrected for or improved by an on-chip DLL?

A. The on-chip DLL would primarily improve component number 3, which he's called chip-to-chip skew. It would just improve the certainty of time in which the data was output onto the bus from the DRAM relative to the clock coming in.

Q. Now, again, based on your understanding in the

1996-1997 time frame, what, if any, effect would an on-chip DLL have with respect to the -- to bullet points 1, 2, 4 and 5 of Mr. Ryan's presentation?

A. It really wouldn't impact those.

Q. Now, in Mr. Ryan's presentation, what technology, if any, was Micron proposing to help solve the variation of the data valid window problem?

A. I think at this time he was primarily proposing the use of echo clocks, which was a technique described earlier where we're converting the problem of absolute timing variance to relative timing variance.

Q. Can you please explain first what an echo clock is?

A. Yeah, in this case he's creating -- he's using a clock input, a separate clock input to clock the data out of the device, and I believe in this case the clock -- the echo clock was to travel in the direction -- same direction of data so that it could also be used to capture the data.

Q. Again, based on your understanding at the time, with reference to DX-117, where would the echo clock originate?

A. He's -- I believe he suggested that there would be a PLL, so they would have some circuit that would regenerate some clock source to create the correct

phased relationship for the read clock, and the output of the PLL on the board or wherever it was located, on the controller, would generate these read clocks.

Q. And again with reference to DX-117, the read clock would travel from where to where?

A. Okay, in this proposal, it would travel from a PLL to the DRAM, and optionally, it could also travel to the controller, although he wasn't specific in mentioning that.

Q. Now, based on your understanding in the 1996 and 1997 time frame, when compared to use of an on-chip PLL or an on-chip DLL, what, if any, were the advantages of using an echo clock?

A. The echo clock, one of the advantages, I think it addressed more components of possible skew than what the DLL did. So, we believed that it could provide larger improvement in timing certainty than the DLL.

Also, because it didn't require the circuitry on chip, we were able to decrease cost, decrease power, eliminate this lock time I talked about earlier.

Q. Based on your understanding at the time, what, if any, were the disadvantages of using an echo clock compared to either on-chip DLL or on-chip PLL?

A. Well, it would compare what your baseline would be. Sometimes when you take one of these things out,

you make other trade-offs, but with that in mind, potentially it could add another clock pin to the DRAM, depending on what your other trade-offs were, and if the controller had a PLL on it already, it would -- it would require no other parts, but if it did not, we might have to put a PLL on the board, a centrally located PLL, for example.

Q. Now, based on your understanding at the time, did you understand the use of an echo clock to be a viable alternative to either on-chip PLL or on-chip DLL from a technical point of view?

A. Yes.

Q. Again, based on your understanding at the time, did you understand use of an echo clock to be a viable alternative to use of an on-chip PLL or on-chip DLL from a cost perspective?

A. Yes.

Q. By the way, did JEDEC ever adopt use of an echo clock in its DDR SDRAM standard?

A. No.

Q. Based on your understanding in the 1997 time frame, what, if any, was the relationship of an echo clock to a data strobe?

A. It was slightly different in that in this proposal he's suggesting it's an input clock, which is

used to clock data out of the device; whereas the data strobe is a strobe that's sourced from the device that's driving the data. And so, then there's different choices of whether that's a uni-directional or bi-directional strobe.

Q. Again focusing on your understanding in the 1996 and 1997 time frame, did you ever consider whether Micron should recommend any other alternatives to use of an on-chip DLL or on-chip PLL to JEDEC?

A. I'm not sure I understood your question. Sorry.

Q. Let me phrase it another way.

In the 1996 or 1997 time period, were you familiar with the concept known as vernier?

A. Yes.

Q. Again, focusing on your understanding at that time, can you please explain what your understanding of the vernier method was?

A. Sure. The vernier is -- you can consider it an adjustable delay element, so the way we would use it, it was one of the tools we liked to use to solve this timing uncertainty problem, is if the timing varied, you could use the vernier adjustable delay to compensate for that. So, if the timing increased, you could use less delay, and if the timing decreased, you

could use more delay, so the loop delay was constant.

And so providing that constant loop delay created a less timing uncertainty and a larger data valid line back at the controller, and this was a technique we were looking at in SyncLink at the time.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked as JX-36. These are the minutes of the JC-42.3 subcommittee meeting from March of 1997 in Fort Lauderdale.

Do you recognize JX-36?

A. Yes.

Q. Were you present at this meeting? If it helps, I direct your attention to page 2, about three-quarters of the way down the page.

A. Yeah, I was at the meeting.

Q. Okay. If I could ask you to turn in JX-36 to page 58, and I'd like to -- I'll give you just a moment.

A. Yes, sir, my copy is cut off a little bit. I can't read the page number.

Q. Excuse me?

A. My copy is cut off a little, so the page

numbers at the end are hard to read.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes, go ahead, if you have another copy.

MR. OLIVER: Yeah, that's right.

THE WITNESS: Okay.

BY MR. OLIVER:

Q. Mr. Lee, I've directed you to a page that bears the caption DDR SDRAM Clocking, Desi Rhoden, and I would like to ask you to flip through the following six pages after that as well, if you could, please.

A. So, I should point out that there's a page in here that it's out of sequence in that it doesn't belong in this presentation. It was part of a different presentation.

Q. Thank you, I think you anticipated my first question. I believe that would be page 59, a page that has an NEC logo?

A. Correct.

Q. Okay, that I believe does not belong to the presentation by Mr. Rhoden, that document.

A. That's correct, that wasn't part of Desi's presentation.

Q. Now, do you recognize the remainder of the pages to which I directed your attention as part of Mr.

Rhoden's presentation?

A. Yes.

Q. For the record, that would be pages 58 through 64, with the exception of page 59, which belongs to a separate presentation.

Now, Mr. Lee, were you present at the time of Mr. Rhoden's presentation at this meeting?

A. Yes.

Q. And did you understand Mr. Rhoden's presentation at the time it was made?

A. Yes.

Q. If I could ask you to turn, please, to page 60, this would be the second page as you've identified it of Mr. Rhoden's presentation, and it bears a caption at the top that reads, "Mini System Block Diagram."

A. Okay.

Q. Could you please explain just in general terms your understanding at the time of what Mr. Rhoden was discussing here?

A. Yes, the presentation generally was what we call an informational presentation. It was just to provide in this case some background information for the committee, and he was through this presentation trying to discuss some of the timing issues that occurred as we moved from a -- from a synchronous

system towards this DDR-type system, and he's talking a little bit about this loop timing issue that I had brought up here.

Q. And if I could ask you to turn two pages further in, this is page 62, has a caption that reads "Simple DDR System Block Diagram," and it contains a diagram that looks anything but simple to me.

Do you see that page?

A. Yes.

Q. Can you again explain, please, your understanding at the time of what Mr. Rhoden was explaining on this page?

A. Yes, I can. I think it might be helpful for me to walk through the first two pages really quick to lead to that.

Q. Certainly, please do so.

A. It's a large jump in complexity, so...

Q. Okay.

A. So, now referring to page 60, what he's just saying, he's looking at the loop timing and he's looking at an SDRAM module, in this case single data rate, and he says that from when you send clock out, there's some flight time of the clock, there's some delay between the device and module, and there is some flight time coming back, and that the read data comes

back to the system controller with some sort of different phase relationship than the clock had sent out. At the SDRAM data rates, we could tolerate this. We were able to handle this. That's kind of the point.

Then on page 61, he shows that -- and he just shows -- it's a mini DDR system, as he calls it, but he's saying as we go to this higher data rate, we still have this loop timing, and part of how we solve that is by transmitting a data strobe out of the DDR SDRAM that what I call flies with the data, so that the phase relationship of the data and the data strobe at the controller are well known, and we use that to capture data. So, we've solved some of the problem and converted it to relative time, like I talked about.

We no longer care about the round-trip time it took, but we start to care about the difference in time of the data strobe versus the data.

Q. Mr. Lee, if I could -- before you continue, if I could ask you to define what you mean by "loop timing" in your previous answer.

A. Okay, so the loop timing is the summation of the time from when the clock is sent out, as data comes out of the DRAM and it travels back towards the controller. So, it's the time from clock out to data back into the controller.

Q. And how, if at all, is that time represented on page 61?

A. He tried to represent it by a phase. These arrows, if you kind of view them as a clock, like a -- to tell time, and it's rotating around, and these phases are rotating around. So, as it advances through the system, you see that the arrow is turning clockwise.

Q. All right. With that background, are you now able to explain what Mr. Rhoden was describing at page 62?

A. I can explain it. I hope we can understand it, but --

Q. Okay.

A. -- I'll try.

MR. PERRY: Can I just make sure that we're still talking about his recollection of his understanding at the time of six years ago?

MR. OLIVER: Yes, Your Honor, that is my question.

JUDGE McGUIRE: Noted.

THE WITNESS: Okay. So, on page 62, he shows an example of -- it's expanded from page 61. Page 61 shows the instance of a single DRAM in a system and how the data strobe is used to resolve the timing

uncertainty, but then he points out that as we look in a bigger system and there's multiple DRAMs out there and multiple DRAM modules, that although the timing from each DRAM is well aligned from its data to its data strobe, the actual arrival of all those different DRAMs occur at different points in time to the controller.

So, if you follow his arrows around, you'll see that although there would be a data strobe that would be perfectly out of phase with the data, when it arrives at the controller, each one of those would arrive at the controller at different points in time, if that makes sense.

BY MR. OLIVER:

Q. Now, again, based on your understanding at the time, how, if at all, did the problem that Mr. Rhoden was describing in pages 58 through 64 of JX-36 relate to the problems that Mr. Ryan had identified in his presentation as you've explained them in DX-117?

A. The relationship would be that what Kevin Ryan was proposing with the echo clocks was similar in terms of what it was trying to solve as the data strobes in that there became a different time reference for when data came out of the memory device, and in Kevin's case, that time reference was this read clock, and that

became a reference for relative time.

In Desi's case, it was using a DDR example, and the time reference is to data strobe, and so the relative time difference is the data strobe relative to the data.

Q. Perhaps I need to break my question down in two parts. Let me focus first just on the definition of the problem, if you will, before moving to any particular clocks or strobes that were being proposed.

Focusing just on the description of the problem, if you will, how, if at all, was the problem being described by Mr. Rhoden in his presentation related to the problem described by Mr. Ryan in his January 1996 presentation as you've explained it in DX-117?

A. Okay, he -- in this case, Desi's trying to address the problem of some of these other delays, if you will. He's addressing the data path skew delay and the clock distribution delay and the on-chip -- I think he called it the chip-to-chip delay.

Q. Would it be fair to say, then, that Mr. Rhoden was describing some but not all of the delays that Mr. Ryan had described in his presentation?

A. Yes.

Q. Now, Mr. Lee, focusing on the 1996 and 1997

time period, did you give any consideration during that time period as to whether a vernier method could be used to improve capture of data at the memory controller?

A. Yes.

Q. And based on your understanding at that time, could a vernier circuit have been used in place of an on-chip DLL to facilitate capture of data at the memory controller?

A. Yes.

Q. Could you please explain your understanding at that time of how a vernier method could have been used to do that?

A. Sure. There's really a couple places we could have put a vernier to solve the timing uncertainty of data coming out of the DRAM, which is what the DLL was trying to address. One is we could have put it in the DRAM itself, and as the delay started to increase, we could reduce the delay -- the number of delay elements in the vernier inside the DRAM to offset that so that there was a more constant output data time.

The other thing we could do is we could put it in the controller itself, and as the delay coming -- of the data coming back from the DRAM started to increase, we could reduce the number of delay elements in the

controller to offset that, so that once again the loop time remains nearly constant.

Q. Focusing again on the 1996 and 1997 time period, during that time period, did you ever consider the advantages of using vernier circuits rather than on-chip PLL or DLL to facilitate capture of data at the memory controller?

A. Yes.

Q. And based on your understanding at that time, what were the advantages of using a vernier circuit rather than on-chip PLL or DLL?

A. They had some of the same advantages of the DLL, that might be easy for me to contrast it. While they both had the disadvantages of some power and die size utilization, with the vernier, we didn't have this lock time problem. We didn't have to wait for it to lock.

And also, we felt that with the vernier, we could put it on the controller so it didn't have to be replicated on every DRAM, and by doing that we could reduce the cost and complexity.

Q. Now, compared with using on-chip PLL or on-chip DLL, based on your understanding at that time, did you understand there to be any disadvantages with using vernier rather than on-chip PLL or DLL?

A. I would say the disadvantages were similar, as I mentioned, to the DLL with power and die size if it was included on the DRAM. I think there was probably more familiarity in the DRAM business with DLL than vernier, but other than that, there's no disadvantage.

Q. Now, based on your understanding at that time, did you regard use of the vernier method to be an adequate substitute for use of an on-chip PLL or on-chip DLL from a technical point of view?

A. Yes.

Q. And again, based on your understanding at the time, did you regard use of the vernier method to be an acceptable alternative to on-chip PLL or DLL from a cost perspective?

A. Yes.

Q. Mr. Lee, if I could ask you to locate JX-41 in front of you, it's a document that I had handed to you earlier today. These are the meeting minutes from the December 1997 42.3 subcommittee meeting in Tempe, Arizona.

Do you have that document?

A. Yes.

Q. If I could ask you to turn, please, to page 18 of JX-41, on that page, I'd like to direct your attention to the caption about a quarter of the way

down the page, capital letter C, JC-42.3-97-128A, AC Spec Parametrics for DDR SDRAM DLL Enabled Item 849.20.

Do you see that?

A. Yes.

Q. If I could ask you to read to yourself the three paragraphs underneath that heading, please.

A. (Document review.) Okay.

Q. At the time that you reviewed the minutes from this meeting in late 1997, do you recall whether you reviewed this portion of the minutes?

A. I believe I did.

Q. And based on your understanding at that time, can you please explain your understanding of what was reflected in this portion of the minutes?

A. Sure. They were discussing what the specification should be, what we called the AC timing specs, for a part that had the DLL turned on. We had agreed on having the ability to turn DLL on or off as a feature of the part, and so at this time they were -- they had taken a vote on it and were discussing the results of that vote about the specific timings for a device with DLL on.

Q. And what was your understanding of the result of that vote?

A. The result was that it passed, the specific

parameters did; however, they agreed to reballot it. They made some changes and then agreed to reballot it as 128B, which is the last sentence of the third paragraph.

Q. Now, what understanding, if any, did you have at this time as to whether there was a consensus within JEDEC as of December 1997 to use on-chip DLL in the DDR SDRAM standard?

MR. PERRY: Objection, Your Honor, he wasn't at the meeting. Lack of foundation.

MR. OLIVER: Your Honor, my question is based on his review of the minutes in late 1997.

JUDGE McGUIRE: In that context, he can answer the question.

THE WITNESS: Okay, my understanding is that there already was consensus for the DLL, and based on the fact that we -- we had already agreed not only on the DLL but on the fact that it could be turned on and off, and at this point we were discussing the timing parameters, very specific of what the timing numbers should be in the case of when it's on.

And I believe also at this time, we were discussing what the timing parameters should be in the case when the DLL is off. So, at this point, we were just resolving the issues and the details of the

specific timing parameters.

BY MR. OLIVER:

Q. Now, based on your understanding in the 1997 time frame, did JEDEC also approve use of a data strobe?

A. Yes.

MR. PERRY: Your Honor, I think I'm going to start objecting to the leading questions. I think we have had enough.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Based on your understanding in the 1997 time frame, what -- what, if any, position did JEDEC take with respect to use of a data strobe?

A. In the 1997 time frame, a data strobe was assumed. We were working out specific issues, and if I recall, around that time frame, there was still some discussion on whether it should be center-aligned strobe or edge-aligned strobe. It was just working out the details of how the strobe would be actually used in the system.

Q. Now, based on your understanding in the 1997 time frame, could you please explain your understanding of how data strobe would be used in connection with the DDR SDRAM standard?

A. I'm not sure I understand what you mean by how it would be used.

Q. Can you please explain the purpose, as you understood it, for consensus to include a data strobe in the DDR SDRAM standard?

A. Yeah, the data strobe was to be used for data capture, for source-synchronous timing, so it assumed a source-synchronous system.

Q. Now, based on your understanding in the 1997 time frame, did you believe it was necessary to include both a data strobe and on-chip DLL in the standard?

A. It was the consensus of the committee; however, I think we still felt -- that Micron in general still felt that there were alternatives that we could have done.

Q. Can you please explain your understanding of the consensus to include both a data strobe and an on-chip DLL in the standard?

A. Sure. There were -- the majority of the people I believe felt that if you used a data strobe as a source-synchronous system, that you wouldn't need a DLL, because you could use the data strobe with relative timing advantage to capture the data. There were a few companies who felt that they were going to try to use DDR in what we call synchronous application,

where they wouldn't use the data strobe and they'd try to capture data with the clock itself, with the internal clock itself, and this is typically for a small system.

And so, the people who wanted to use the DRAM that way wanted DLL to improve the ability to capture this in a synchronous system, and the companies that wanted to use the data strobe didn't feel like it was necessary. So, those were the kind of two differing viewpoints at the time.

And finally, a compromise was made -- I would say we capitulated -- and the reasonable compromise was to do both but provide the ability to turn off the DLL.

Q. Now, at the time, were you involved in any discussions within Micron concerning what position Micron should take and whether it should agree to use of on-chip DLL in the standard?

A. Our preference was still not to have one, but our action was to -- to go along with the committee in general with this compromise, because there was -- because of these differences of opinion, it was causing some delay in the standardization process. So, we agreed to go along, if you will, although we still preferred not having a strobe.

Q. Can you please explain why the potential delay

that you just mentioned was a factor in your understanding at the time?

A. It's similar to the delay problem we discussed before. If the standard takes too long to develop, then we would miss a market opportunity. Customers needed a certain amount of time to start designing these things in. They rely on the standard to start making their designs. So, we were holding up progress of new technology development.

Q. Now, focusing again on your recommendations within Micron, if Rambus had disclosed within JEDEC in 1995 or early 1996 that it believed it had patent rights that would cover the use of on-chip DLL, how, if at all, would that have affected your recommendation?

MR. PERRY: Objection, vague, compound and calls for speculation.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, focusing again on your recommendation within Micron in the relevant time period, if Rambus had disclosed within JEDEC in the 1995 or 1996 time frame that it believed it had patent rights covering the use of on-chip DLL, would that have had any effect on your recommendation within Micron?

MR. PERRY: Objection, the question is

identical to the one that was just --

JUDGE McGUIRE: Mr. Oliver, how is that not calling for speculation?

MR. OLIVER: Your Honor, with respect to the speculation issue, that again goes to the issue that they have raised in their pretrial brief, expecting us to prove but for causation.

Now, as we've said, we don't think we have that burden, but nevertheless, just in case you or the Commission were to find that, we do need to establish that.

JUDGE McGUIRE: All right, I'll entertain the question.

MR. OLIVER: Thank you, Your Honor.

THE WITNESS: Okay, so --

MR. PERRY: Your Honor, if I could, my -- I had additional objections. The phrase "patent rights" is vague and imprecise, and it's not clear at all what he means.

JUDGE McGUIRE: Okay, Mr. Oliver, then on that basis, could you restate the question? Otherwise, I will hear it.

MR. OLIVER: Yes, thank you, Your Honor.

MR. PERRY: And Your Honor, my other objections I don't have to make again to this new question?

JUDGE McGUIRE: No, you do not.

MR. PERRY: Thank you.

BY MR. OLIVER:

Q. Mr. Lee, if Rambus had disclosed in JEDEC in -- at any time in 1994, 1995 or 1996 that it had a pending patent application that it believed contained claims that would cover use of on-chip PLL or on-chip DLL, how, if at all, would that have affected your recommendation within Micron?

A. We would have avoided the use of it and developed an alternative. It was part of the JEDEC policy to avoid the use of patents when possible.

MR. OLIVER: Your Honor, I'm about to move to a new topic. I can either continue or we could break for lunch, as you prefer.

JUDGE McGUIRE: How much more time would it take to at least get to a point in your new topic where you are able to break?

MR. OLIVER: Your Honor, I'm guessing my next topic will go for an hour or so.

JUDGE McGUIRE: Then I guess we ought to break. It's a quarter after 12:00. Why don't we convene back here at 1:45, about an hour and a half.

MR. OLIVER: Thank you, Your Honor.

JUDGE McGUIRE: Hearing adjourned.

(Whereupon, at 12:15 p.m., a lunch recess was taken.)

AFTERNOON SESSION

(1:45 p.m.)

JUDGE McGUIRE: This hearing is now in order.

At this time, complaint counsel may proceed with its inquiry of the witness.

MR. OLIVER: Thank you, Your Honor.

JUDGE McGUIRE: Mr. Lee, you may have a seat back on the stand, if you would.

BY MR. OLIVER:

Q. Good afternoon, Mr. Lee.

A. Good afternoon.

Q. Mr. Lee, focusing now on the late 1995 to 1997 time period, at that time, did you have an understanding of the concept of dual edge clocking?

A. Yes.

Q. Can you please explain briefly your understanding at that time of dual edge clocking?

A. By dual edge clocking, it's referring to capturing data off of both edges of a clock.

Q. If I could ask you to locate in front of you, please, CX-260. This is a copy of the survey ballot from October of 1995.

Do you have a copy of that?

A. Yes.

Q. If I could ask you to turn, please, to page 12,

and I'd like to direct your attention in particular to question 3.9-4 on page 12, which reads, "Does your company believe that future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?"

Do you see that?

A. Yes.

Q. Now, based on your understanding when you reviewed this survey ballot in late 1995, what, if any, was the relationship between dual edge clocking and the clocking scheme being asked about in question 3.9-4?

A. In this case, they're asking if we felt that the SDRAM would benefit -- the future SDRAMs would benefit from using both edges of the clock for sampling inputs. In other words, using a dual edge clock.

Q. So, in other words, using both edges of the clock was similar to using or the same as using dual edge clock?

A. Yes.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked JX-31. These are the minutes from the JC-42.3 subcommittee meeting from March of 1996 in San Diego,

California.

Mr. Lee, do you recognize JX-31?

A. Yes.

Q. Were you at this JC-42.3 subcommittee meeting in San Diego?

A. I believe I showed up for just a day or so.

Q. Okay. Do you recall whether you saw the minutes in or shortly after March of 1996?

A. Yes.

Q. If I could direct your attention --

JUDGE McGUIRE: Wait a minute, wait a minute, the answer is do you recall if you saw the minutes, and the answer is yes, that you saw the minutes? Is that --

THE WITNESS: Yes.

JUDGE McGUIRE: All right, I'm unclear as to what you're answering to.

THE WITNESS: Yes, I was --

JUDGE McGUIRE: Go ahead.

THE WITNESS: -- I was just trying to refresh myself on the contents.

JUDGE McGUIRE: That's fine. I just wanted to make sure I'm clear on what the answer was in terms of the question.

Go ahead.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. If I could ask you to turn, please, to page 68 of JX-31, I would like you to look at pages 68 through 72.

A. (Document review.) Okay.

Q. Have you had a chance to look at those pages?

A. Yes.

Q. Do you recall whether you reviewed those pages in or shortly after March of 1996?

A. Yes, these were some of the pages that I reviewed.

Q. If I could ask you to turn, please, to page 71. Could you please explain briefly your understanding of the proposed clocking scheme that Samsung was proposing as you understood it at the time that you reviewed this document?

A. Yes. Samsung was offering an alternative and suggesting we move the DLL off the memory device and instead use a controller -- use a PLL in the controller to generate a phase-shifted read clock, and they were proposing to sample data on both edges of the clock for data in the memory and using both edges of the strobe to sample it on a read into the controller.

Q. Now, Mr. Lee, focusing on the time period from

late 1995 through 1997, and again, focusing on your knowledge and understanding at that time, do you recall whether issues of Rambus patents with respect to a proposed clocking scheme ever arose at JEDEC?

A. I'm sorry, that was in the 1995-'97 time frame, your question is?

Q. Yes.

A. Yes, I do.

Q. Can you explain briefly your recollection of in what context the issue of Rambus patents relating to a clocking scheme arose within JEDEC?

A. Yes. There was a meeting in '97, and a clocking scheme was proposed that looked similar to one of the Rambus patents, and the committee basically objected.

Q. If I could ask you to locate JX-36 among the documents in front of you, these were the minutes from the March 1997 meeting in Fort Lauderdale.

If I could ask you to turn in particular to page 7 in this document, and item 6.6 towards the bottom of the page is encaptioned NEC DDR SDRAM for High End Systems Item 844.

Do you see that?

A. Yes.

Q. And then the paragraph under that reads, "A

first showing was made by NEC (See Attachment F). It included a read clock and a write clock. A discussion of the clock issue took place. Some on the Committee felt that Rambus had a patent on that type of clock design."

Do you see that?

A. Yes.

Q. Is that the proposal and the discussion that you had in mind in your answer a moment ago?

A. Yes.

Q. By the way, were you present at the time that NEC made this proposal?

A. I'm sorry, what was the question?

Q. Were you present in the meeting at the time that NEC made this proposal?

A. Yes.

Q. And did you observe that presentation?

A. Yes.

Q. And did you understand it at the time?

A. Yes.

Q. If I could ask you to turn, please, to page 56 of JX-36, and if I could ask you to look at pages 56, 57 and 59, and you may recall that you actually looked at page 59 earlier this morning and it was out of order.

A. Okay.
Q. Do you recognize pages 56, 57 and 59?
A. Yes.
Q. And is that the presentation being referred to in item 6.6 we looked at a minute ago?
A. Yes.
Q. Can you please explain your understanding at the time this presentation was made of what this presentation involved?
A. Yeah, this was a proposal by NEC for a different clocking scheme for DDR.
Q. What clocking scheme was NEC proposing?
A. They were proposing a scheme that had a separate read clock that was free running and the -- the topology of the read clock was that it went down to the end of bus and then looped back.
Q. Do you recall any discussion of any technical elements of this proposal that are not reflected in pages 56, 57 and 59?
A. Technical issues?
Q. Yes.
A. Yes.
Q. Can you please explain what technical issues you recall that are not reflected in those pages?
A. Sure. When Asa Kura of NEC presented this, it

wasn't very clear what kind of scheme he meant by this. We couldn't tell from the timing diagram what really topology or what he had in mind, and so it was difficult to understand exactly what the scheme was. So, he was asked to kind of draw it up. I can't remember if it was on a foil or on an easel, but he had a drawing with what the bus topology would look like.

Q. And based on that drawing, what did you understand his proposal of the bus topology to involve?

A. Well, it looked similar to the loop-back clock, similar to that '703 patent we talked about earlier, the Rambus patent.

Q. What, if any, was your reaction when you -- when you saw this proposal?

A. I was opposed. I believe I was the one that asked him to draw it when he showed it. It looked like the '703 patent from what limited information we had of his -- you know, his drawing, his hand drawing, excuse me, and I objected that I thought that this was -- looked similar to the Rambus patent.

Many other people in the room also objected. There was a variety of comments from quite a few people from the committee who were -- strongly objected to the consideration of this proposal for the standard.

Q. What, if anything, happened with respect to

this proposal at this March 1997 meeting?

A. I did not see it presented again after this time, so there was -- it was -- there was no support for it at the meeting, and as far as I know, they never brought it back in.

Q. To the best of your understanding, was this NEC proposal ever incorporated in any manner in the JEDEC DDR SDRAM standard?

A. No.

Q. Now, at some point after this March 1997 meeting, did you make a proposal to JEDEC with respect to a proposed clocking scheme?

A. Yes, for DDR2.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

THE WITNESS: (Document review.)

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-368, has a title Proposal for DDR Data Strobe, and in the lower left-hand corner a date of April 3, 1997, and the lower right-hand corner, the Micron logo.

Do you recognize this document?

A. Yes.

Q. And what is CX-368?

A. This is a JEDEC proposal for how to do the data

strobe, a proposal for using a data strobe.

Q. And who made -- actually, what -- do you know whether this was actually presented at JEDEC?

A. Yes.

Q. And who made that presentation at JEDEC?

A. I did.

Q. Just to be certain that the record is clear, the proposal, CX-368, was this made in connection with the DDR SDRAM standard or the DDR2 standard?

A. This one's DDR. The one I referred to earlier was a different presentation.

Q. Okay. Can you please explain in general terms what you were proposing in CX-368?

A. Yes, we were proposing the use of -- we call it bi-directional data strobe that is edge-aligned with the data, which means the edge of the clock is roughly aligned with the edge of the data.

Q. If I could ask you to turn, please, to page 2, you'll see the first and the second bullet points contain references to a loop-back strobe.

Do you see that?

A. Yes.

Q. And then the third bullet point contains a reference to bi-directional strobe.

Do you see that?

A. Yes.

Q. Could you please explain what you had in mind when you made this presentation with respect to a loop-back strobe?

A. Yes, it's more correctly the loop-back clock. It was basically responding to the earlier NEC proposal the month prior. This was an interim meeting which followed the regular meeting. And we were pointing out some problems with the loop-back clock and making a proposal to do a bi-directional strobe.

Q. I just want to be certain we establish for the record what you meant in technical terms by a "loop-back clock."

A. The loop-back clock was a -- was referring to the NEC proposal, in their case a free-running clock that went to the end of bus and came back and was tapped off by the DRAMs for use of a read clock.

Q. And then in the last bullet point, you refer to a bi-directional strobe. Can you please explain what you had in mind at the time you gave this presentation with respect to a bi-directional strobe?

A. Yes, the bi-directional strobe is a data strobe that data -- or the information would be communicated in either direction, so in the case of a read, it's driven by the DRAM, and in the case of a write, it's

driven by the controller.

Q. Now, looking at the second bullet point on this page, "Loop-back strobe could have intellectual property problems."

Do you see that?

A. Yes.

Q. Now, at the time you gave this presentation, what did you have in mind with that bullet point?

A. We were concerned that NEC's proposal was related to the Rambus '703 patent, so we were -- we were stating that we should avoid this, that there might be IP problems in that they might already have a patent associated with it.

Q. And with respect to your recommendation for the bi-directional strobe, did you have an understanding one way or another at the time as to whether that could avoid the Rambus patent?

A. We didn't have any knowledge that there were any patent issues relating to the bi-directional strobe.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Go ahead.

BY MR. OLIVER:

Q. Mr. Lee, I've given you a document marked as RX-920. I will give you a moment to look at that

document.

A. (Document review.) Okay.

Q. Now, just to set the understanding here, this appears to be a series of email exchanges. Is that right?

A. Yes.

Q. Did -- or were you one of the recipients of these various emails?

A. Yes.

Q. If I could direct your attention to what appears to be the second email, to about a quarter of the way down the first page, it is from Weinstock, Keith D.

Do you see that?

A. Yes.

Q. Who is Mr. Keith Weinstock?

A. Keith Weinstock was with our sales department. He was the Intel account representative.

Q. And the date of that email is April 17, 1997. Is that right?

A. That's correct.

Q. And if I can direct your attention to the language in that email, it reads, under Terry, "Yes, Rambus feels DDR for any memory is under their patent coverage. James said that Rambus has more IP than

Intel has seen."

Do you see that?

A. Yes.

Q. Now, at the time, did you have an understanding of who James referred to?

A. Yes.

Q. Who did that refer to?

A. That's James Akiyama.

Q. Now, Mr. Lee, if we could, I'd like to put this email in the context of events at the time.

Approximately how long after you had seen the presentation for the loop-back clock at JEDEC did you receive this email?

A. Roughly one month.

Q. And approximately how long after the -- after your own presentation in which you distinguished a bi-directional strobe from the loop-back clock which might have intellectual property issues, how long after that presentation did you receive this email?

A. Approximately two weeks.

Q. Now, when you received this email in April of 1997, what, if anything, did you do?

A. I called James Akiyama to try to get the technical details for some simulations I was going to perform. I was trying to get some simulations ran,

some circuit simulations ran in preparation for future meetings.

Q. Did you follow up at all with respect to the rumor that Rambus feels it has patent coverage on DDR?

MR. PERRY: Your Honor, I'll object to the reference to a "rumor." I don't see that word used in the document.

JUDGE McGUIRE: Sustained.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Did you follow up at all with respect to the reference in the email with respect to Rambus feels DDR is under their patent coverage?

A. No.

Q. Why not?

A. It wasn't credible.

Q. Why not?

A. Others -- really a number of reasons at that time. First of all, it was hearsay. It wasn't actually communicated to us by Rambus. It was third party. Intel said themselves they haven't seen Rambus' IP.

Also, it was kind of typical -- there were some events going on at that time. There was some misinformation going around in the industry, and this

was consistent with that.

Also, we had just -- the time frame here, we had just completed our licensing agreement with Rambus for direct RDRAM a month prior, and in the course of those negotiations, they never claimed or disclosed that they had patents that would relate to any other technology at that time.

And then also, Rambus was a JEDEC member. They would have had a responsibility to disclose patents that may have related to the SDRAM or DDR work at the time when they were a member.

Q. I'd like to follow up on those points, if I could, to get, again, your understanding as of April 1997.

First of all, you mentioned that you thought that this was hearsay. Could you please elaborate as to how that affected your thinking at the time?

A. Sure. I think I probably need to describe some background events to make that clear. Is that all right?

Q. Okay. Could you please describe the background events that you had in mind that affected your thinking at the time?

A. Sure. At this time, Rambus was getting ready to go public, launch their IPO, and there was a lot of

information going around in the, say, approximately last six months prior to that time that seemed misleading. We were seeing things either in the press or through what could be called carefully worded press releases that had a misleading -- that seemed to mislead us.

Also, we heard different statements from them as to what market share they expected to achieve in that time frame, and they were -- also had made overstatements of the progress of their technology to us and to Intel. And we felt that they were doing a lot of pumping up of their company value prior to the IPO. So, the fact that -- that they would state that to Intel was -- was consistent with some of the behavior that had been going on.

Additionally, James was part of the graphics group at Intel, and the graphics group had not decided to use Rambus, as is shown in this statement as well, that they were using DDR SGRAM. So, Rambus would be motivated to try to convince them not to do that, and I believe it was just consistent with them overstating how important they were and how they had -- how Intel had no other alternative but to use them. We felt they were just trying to support that position.

So, it was -- it was really just a very large

amount of overstatement and misinformation going around the whole industry at that time through a variety of sources, and this kind of technique was consistent with that.

Q. You also referred to the fact that Rambus and Micron had recently completed licensing negotiations. Can you please explain how that affected your thinking as of April 1997?

MR. PERRY: There is no foundation he was at all involved in the licensing negotiations, Your Honor.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, I believe that you testified this morning that Mr. Mailloux had some discussions with you in December of 1996 with respect to licensing negotiations between Micron and Rambus.

A. Correct.

Q. I believe you also testified this morning that Micron, in fact, signed a license agreement with Rambus in 1997.

A. Correct.

Q. Do you recall when Micron signed the licensing agreement with Rambus?

A. It was in March, I believe.

Q. And can you please explain what involvement you

had, if any, in connection with the negotiation or preparation for negotiation of that license agreement between December of 1996 and March of 1997?

A. Sure. There was two-way information flow. I was providing primarily technical input, market input, and receiving information back in terms of progress of the negotiations and what's been offered and what's been said. And I think at some point I had seen some -- some preliminary documents, a contract.

Q. Okay. Now, based on -- based on the understanding that you gained during that process, what, if any, relevance did that understanding have on your thinking in April of 1997 in response to the email, RX-920?

MR. PERRY: There is certainly no foundation for him to say what Rambus did or didn't say in those negotiations.

JUDGE McGUIRE: Noted.

MR. OLIVER: Your Honor, I am simply --

JUDGE McGUIRE: He can answer the question, but I take it in the context of the objection.

MR. OLIVER: Thank you, Your Honor.

THE WITNESS: My information is based on information that was provided to my by my management. They were providing interim summaries, the status of

what's going on, what's been offered, what's been counter-offered. Although I wasn't in the room during the actual negotiations, they were giving us feedback or some input.

And based on that feedback, they had never brought up any possibility of having patents beyond this. They never disclosed during the course of negotiation that they had patents that would apply to something besides direct RDRAM.

My state of mind, if you will, at that time was that they would have had a self-interest to do so, because if that were the case, they could have used that to negotiate a higher license fee or a higher royalty, but instead, we received a copy of the email from Geoff Tate to Steve Appleton -- we called it the "put all your wood behind one arrow" email, if you will -- that sought to actually offer us a discount if we were to terminate all of our other high bandwidth DRAM efforts.

So, to me, it didn't make sense that they would have IP on other technologies for high bandwidth DRAMs if they're willing to offer us a discount if we would terminate those efforts.

MR. PERRY: I'll move to strike the two sentences I think that were in there about what Rambus

did or didn't say as lacking a foundation.

JUDGE McGUIRE: Sustained.

MR. OLIVER: Your Honor, could I be heard on that?

JUDGE McGUIRE: Go ahead.

MR. OLIVER: Your Honor, this goes simply to Mr. Lee's state of mind in terms of his reaction to this email, and for that --

JUDGE McGUIRE: But he doesn't know what they said, so to that extent, that objection is sustained. Now, he can testify as to his understanding, but, you know -- and I -- at this point, I can't recall exactly what he did say, so I'm a little confused now, but his answer has been heard, and I'll give it its proper context, but he can't testify as to what he has not heard.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Based on your understanding in the April 1997 time frame, I believe in your last answer you stated that you understood that Rambus might be able to negotiate a higher royalty or a higher fee had they disclosed that they believed they had license -- excuse me, had they disclosed that they had patents and patent applications that might extend beyond RDRAM. Can you

please explain what you meant by that?

MR. PERRY: Objection, leading and misstates the testimony.

JUDGE McGUIRE: Overruled. I'll let him answer so he can help clarify the prior answer.

So, can you do that, Mr. Lee?

THE WITNESS: Sure. If -- if their patents would have had coverage on other products, it would have been more valuable to us. We would have probably been willing to pay more for such a license fee because it would have covered other products.

BY MR. OLIVER:

Q. And finally, I believe the fourth factor that you mentioned that affected your thinking at the time was that based on your understanding, Rambus had not disclosed within JEDEC. Can you please explain how that factor affected your thinking in April of 1997?

A. Sure. They would have had an obligation to disclose, so I think we would have taken it very serious if Rambus would have disclosed at that time or disclosed to us directly that they had patents that would relate to other work or other technology we were doing.

The only context we received this kind of information in was through this -- this hearsay or this

third-party information. So, when they had an opportunity and a motivation and a responsibility to disclose that to us, they did not.

Q. Now, if we could turn to JEDEC work in the 1995 to late 1997 time frame, during that time period, to the best of your knowledge, did JEDEC ever consider any alternatives to dual edge clocking?

A. Yes.

Q. Again, based on your understanding, what alternatives to dual edge clocking did JEDEC consider during that time period?

A. We considered single data rate clocking, and we -- we did it in the context of just a higher speed clock. And also there was some discussion of using a slower speed single data rate clock and using a frequency doubler on chip, to create a higher frequency, dual edge clock for capture. I think there were some discussions about wider buses at the time, but I don't think any proposals were brought forward.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-371. I'll give you just a moment to review that document.

A. (Document review.) Okay.

Q. Mr. Lee, do you recognize CX-371?

A. Yes.

Q. What is this document?

A. This is a proposal from Texas Instruments for a -- for a single edge data rate clock using the differential clocks, and there were two versions they were proposing here. One is a high-speed clock and the other is a frequency doubling clock, what I was referring to before.

Q. Okay. You are referring to two versions. Were you referring to a particular page in CX-371?

A. Yeah, the last page, page 3.

Q. Okay, before we plunge into that page, let me just verify that the -- the email to you bears a date of July 28, 1997. Do you recall receiving this document at about this time?

A. Yeah.

Q. And did you review this document at the time you received it?

A. Yes.

Q. And did you have an understanding of the document at the time you reviewed it?

A. Yes.

Q. If I could ask you to turn, please, to page 3,

and you referred to two different proposals. Was that referring to the -- is that referring to two different diagrams on this page?

A. Yes.

Q. If we could look at the top diagram first, can you please explain your understanding as of late July 1997 of what Texas Instruments was proposing in this top diagram?

A. Sure. They were proposing that since we were using differential clocks at that time, they felt that we could operate at a higher frequency. Differential clocks provide you some sort -- some timing benefit, if you will. And so, his idea was to run a high-speed differential clock through a differential receiver and then clock data in on just the positive edge of that clock, which he's denoted here as T0 prime and T1 prime.

Q. And if I could direct your attention to the bottom diagram, could you please explain your understanding in July of 1997 of what Texas Instruments was proposing in the bottom diagram?

A. Yes. He was proposing that in the case that there was not adequate bandwidth on the high-speed clock, that he could run it at half the rate, and after receiving it could use a frequency doubler on chip and

then use the -- just the positive edge of that output, once again noted as T0 prime and T1 prime.

Q. Now, at the time that you received this email in July of 1997, did you have an understanding at that time as to whether these two proposals were adequate technical alternatives to use of a dual edge clock?

A. Yes.

Q. And what was your understanding at the time?

A. I believe -- I think I particularly believed that the frequency doubled version was feasible. I felt on the -- the higher data rate version, that he would probably need to make some changes to the bus topology to make it work at the data rates he wanted to make it work at.

Q. And with respect to the frequency doubling, you are referring to the second or the lower diagram on page 3 of CX-371?

A. Yes.

Q. And with respect to the top diagram on page 3 of CX-371, if the change that you referred to to the bus topology were made, did you have an understanding at that time as to whether the top diagram then would represent an adequate technical alternative to dual edge clocking?

A. Yes.

Q. And again, focusing on your understanding in July of 1997, did you have an understanding as to whether these two proposals represented acceptable alternatives to dual edge clocking from a cost point of view?

A. Yes.

Q. And what was your understanding at that time?

A. We didn't see that this alternative would have any additional cost over what we were doing.

Q. Mr. Lee, if I could ask you to locate JX-40 in the pile of documents in front of you, these are the meeting minutes of September 1997 of the meeting held in Taipei, Taiwan.

Do you have that document?

A. Yes.

Q. Okay. If I could ask you to turn, please, to page 8, I'd like to direct your attention to the heading 8.2, JC-42.3-97-123/124 BDDR Bi-Directional Data Strobe, and if you could please read to yourself the paragraph underneath that heading.

A. (Document review.) Okay.

Q. Now, after the September 1997 meeting in Taipei, Taiwan, is this paragraph under heading 8.2 one of the paragraphs that you reviewed when you saw these minutes?

A. Yes.

Q. Can you please explain your understanding of what was reflected in the paragraph under heading 8.2 on page 8 of JX-40?

A. Yes. The proposal for the bi-directional data strobe passed, and it was agreed to go on to council.

Q. Now, based on your understanding at the time, did that involve any decision with respect to using a single edge clock or a double edge clock or any other type of clock?

A. The data strobe was -- used both edges.

Q. Now, were you involved in any discussions within Micron during the 1996 to 1997 time period in terms of whether Micron should support inclusion of dual edge clock in the DDR SDRAM standard?

A. I'm sorry, the question was whether there was discussion within Micron on whether we should support dual -- I'm sorry, could you repeat it?

Q. The question is whether you were involved in any such discussions within Micron.

A. Yes.

Q. And based on your recollection, do you recall what position Micron took with respect to a dual edge clock?

A. We were in support of the dual edge strobe. We

were pretty closely aligned with Samsung on this issue. I believe they were -- they were sponsoring the ballot, and I think the only difference that we had between them is whether it would be center aligned or edge aligned.

Q. Okay. Now, focusing --

MR. PERRY: Objection, Your Honor, the question was about dual edge clock, and he answered as to dual edge strobe.

JUDGE McGUIRE: Mr. Oliver?

MR. OLIVER: Your Honor, I think he answered my question to the best of his abilities.

JUDGE McGUIRE: Overruled.

BY MR. OLIVER:

Q. Now, Mr. Lee, focusing on your particular position at the time, did you recommend that Micron support using both edges of the clock to transfer data?

A. Yes.

Q. Now, Mr. Lee, if -- if Rambus had disclosed while it was a member of JEDEC that it had patents or patent applications relevant to using both edges of the clock to transfer data, what effect, if any, would that have had on your recommendation at the time?

MR. PERRY: Same objection as I made this morning, Your Honor, calls for speculation. This one

also assumes facts not in evidence, I think as did the earlier one.

JUDGE McGUIRE: Well, I don't know what facts you're saying are not in evidence, but to the extent that it calls for speculation, it's going to go back to the same opinion I had this morning, that it goes to the question of the but for scenario, so on that basis, it's overruled.

MR. OLIVER: Thank you, Your Honor.

THE WITNESS: Okay, so the question was what effect it would have on our recommendation?

BY MR. OLIVER:

Q. On your recommendation if Rambus had disclosed at JEDEC that it had patents or patent applications relating to transferring data on both edges of the clock.

A. I would have opposed it. We have a responsibility in JEDEC to try to avoid the use of patents whenever possible in creating a standard, and also our company has a similar policy, as we try to avoid the use of patents whenever possible. Particularly I'd have to say in the case where Rambus is not a manufacturer, it wouldn't have even been a situation where we could have cross-licensed. So, we would have been strongly opposed.

Q. Mr. Lee, I'd like to switch topics now and discuss a number of Micron's technology roadmaps and other documents from the 1998 and 1999 time frame.

Let me ask first, are you familiar with the concept of technology roadmap?

A. Yes.

Q. And focusing on how you understand that term to be used within Micron, could you please explain your understanding of that term?

A. Sure. Within Micron, the use of that term is about some documents that we prepare for customers that show what our future plans are for memory technology, usually on a product basis, but sometimes also on where our process is going, what kind of future processes we'll have.

Q. Are these documents that you ever use in the course of your work?

A. Yes, they are.

Q. Can you please explain how you use these documents in the course of your work?

A. Sure. My -- I work with the customers quite a bit, and primarily on a technical basis, but often they would request that I also bring some information about what our roadmap looks like going forward in terms of products or process. So, I would in those cases bring

this presentation along and go through the presentation with them.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document that's been marked 2718. It bears a caption Micron DRAM Update, and underneath that, March of 1998.

Mr. Lee, do you recognize CX-2718?

A. Yes.

Q. Can you please explain just very briefly what CX-2718 is?

A. Sure. This is a sales and marketing tool to describe our products, also some market conditions, and also what we're doing in the future, in this case where it says "next generation DRAMs," and it's a communication tool to inform our customers of where we're headed with products and technology and where we see the market at that time. This kind of document is updated on a -- roughly a quarterly basis, sometimes a monthly basis. So, this is I would call an example of one of those documents.

Q. If I could ask you to turn, please, to page 26, and could you please explain just in very general terms what is reflected on page 26?

A. Sure. This is what we call the DRAM product roadmap, and this shows what kind of products are going to be available at certain time frames from a technology standpoint and also a density and sometimes device organization in terms of the device data width. And it shows when we're going to be in production and when we're going to sample and in some cases when we're going to discontinue the product.

Q. Okay. If I could ask you to walk through a couple of examples just to explain how this chart or how to read the information reflected in this chart. If I could ask you to look at what I believe is the seventh line, a bit difficult to read, but I believe it reads "16-meg SDRAM."

A. Okay.

Q. Do you see that line?

A. Yes.

Q. And it's -- looking across, it says, Y42, Y52 and Y72.

Do you see that?

A. Yes.

Q. Can you please explain just in general terms what is reflected by that line?

A. Sure. The Y42 is a 16-meg DRAM that's on a particular process technology, and it shows that --

more sampling towards the beginning of the year and would be in production probably sometime second quarter of that year, and it shows -- it later gets replaced by the Y52, which is the same functional device on a process shrink, on a next process technology, and it shows that continuing on to the Y72.

Q. Just to clarify one point, looking within Y42, there's a sloped line before it becomes a flat line.

A. Yes.

Q. Can you please explain what that sloped line indicates?

A. That means that we're sampling and we're getting ready to go to a volume production, and there's kind of an assumed production ramp somewhere at that time.

Q. And then once the line becomes flat, what does that indicate?

A. It indicates that we're either in high-volume production or we're ramping up to that level.

Q. Okay. And if I could direct your attention to the next to last line, it reads, I believe, "64-meg DDR SDRAM."

Do you see that?

A. Yes.

Q. Could you please explain what was indicated in

that line?

A. Yes, it shows that we plan on sampling about the middle of '98 with this 64-meg DRAM device and are expecting production sometime in the fourth quarter.

Q. Now, does that indicate, then, that at this time, Micron expected to begin work on the 64-meg DDR SDRAM part in mid-1998?

A. No.

Q. Can you please explain why that's not true?

A. This is strictly for when products -- when we anticipate having the products available for the customer. We would have started our design team -- typically, it depends on the part -- but I think in this case about a year earlier and would have started actual work on the part before we started the design team, anywhere from, you know, six to 18 months maybe prior to that.

Q. If I could direct your attention to the last line, again, difficult to read, but I believe it reads "64-meg RDRAM."

Do you see that?

A. Yes.

Q. Can you please explain what is indicated in that line?

A. Sure. At that time, we were projecting to have

64-meg RDRAM samples available towards the beginning of fourth quarter and production sometime in the first quarter.

Q. If I could ask you to turn, please, to page 44 of CX-2718, could you please explain in general terms what is reflected on page 44?

A. Sure. This -- this is a summary of some next generation DRAM products that we're doing, and it summarizes some of the features of the product. Also, it gives some estimates of when we would have samples and production available.

Q. And if I could direct your attention to the third to the last line and second to the last line, which is samples and production, do you see those -- do you see those lines?

A. Yes.

Q. And then under the columns DDR SDRAM and SLDRAM and Direct RDRAM, do you see those columns?

A. Yes.

Q. Generally speaking, do the figures that are -- that are filled in there correspond roughly with the information reflected on page 26?

A. They should.

Q. Okay. If I could direct your attention to the last line, please, Estimated Costs.

Do you see that line?

A. Yeah.

Q. And looking first in the DDR SDRAM column, the estimated cost reads 1.05.

Do you see that?

A. Yes.

Q. Can you please explain what that means?

MR. PERRY: Your Honor, I don't think there's a foundation that he worked on this chart at all. If he's just telling us what it means, I don't think that's relevant.

JUDGE McGUIRE: Sustained, Mr. Oliver.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, is -- referring generally to CX-2718, is this a document that you used in the course of your responsibilities during 1998?

A. Yes.

Q. Can you please explain how you used this document in the course of your responsibilities at that time?

A. It was used to communicate to customers some of the summary of features of next generation products that we had.

Q. Now, in the course of your responsibilities in

1998, did you develop an understanding of the information reflected on page 44?

A. Yes.

Q. And specifically with reference to the last line, Normalized Estimated Cost, during the course of 1998, did you have an understanding of the information reflected in that line?

A. Yes.

Q. Referring again to the figure 1.05 in the DDR SDRAM column, can you please explain your understanding at the time of what was reflected by that figure, 1.05?

MR. PERRY: Your Honor, there is still no foundation for him to say this is what the costs were at the time or what they were projected to be. I think he's only asking for what he understood from being a reader of it, but I want to make clear that there is no foundation for him to say these were --

JUDGE McGUIRE: All right, noted. The objection is noted, and you can ask the question in that proper context.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Again, focusing on your understanding, Mr. Lee, can you please explain your understanding at the time of what was meant by the figure 1.05 in the Normalized

Estimated Cost row under DDR SDRAM?

A. Sure. We gathered information from our design teams and test teams and stuff and tried to come up with our best estimate of the relative cost of that technology compared to using -8 SDRAM as a baseline.

Q. In your previous answer, what did you mean by "-8 SDRAM"?

A. This was 100-megahertz SDRAM, sometimes called PC100.

Q. And that's what's reflected in the first column on page 44?

A. That's correct.

Q. If I could direct your attention to the third column, SLDRAM, first of all, what was your understanding at the time of what was meant by SLDRAM?

A. That's the SyncLink DRAM definition which was developed in the SyncLink Consortium.

Q. And looking again at the last line, it contains a figure of 1.15. Can you please explain your understanding at the time of what was meant by the figure 1.15?

A. Sure. Again, working with our design and test teams, we established our estimate of what the cost increase for that kind of part was relative to the baseline of the PC100 SDRAM.

Q. And if I could direct your attention to the third column, Direct RDRAM, and within that column, the last line has a figure of 1.30. Can you please explain your understanding in the 1998 time frame of what was meant by the figure 1.30 in that line?

A. Sure. A similar process, again, for establishing the number, and we projected a 30 percent cost increase for direct RDRAM relative to an SDRAM.

Q. If I could ask you to turn, please, to page 45, and on this page, there's a table toward the top part of the page reading "Main Memory," and then toward the bottom part of the page reading "Graphics."

Do you see that?

A. Yes.

Q. Can you please explain just very briefly your understanding at the time of the difference between the table for main memory versus the table for graphics?

A. Sure. Main memory is generally referred to as memory that's used for programmable data store, so it -- it either communicates directly with the CPU or through a controller; whereas graphics memory is primarily used for manipulating graphics on the screen, on the display.

Q. Can you please explain just in very general terms your understanding in the 1998 time frame of the

information that was conveyed on page 45?

A. Sure. We were building a matrix. Going across the top, these are different market segments or also different what we call platforms of applications in which the memory would be used in, and then just focusing -- staying on main memory right now, the rows there, low end, mid-range, high end are different price/performance points for that kind of product.

For example, a consumer desktop would be a PC that would be used typically by somebody in their home, and the low end would be a very inexpensive machine.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2728. It consists of an email from J. Mailloux dated December 15, 1998 to a number of individuals, including yourself.

Do you recognize CX-2728?

A. Yes.

Q. What is this document?

A. This is a survey that Dell had asked us to fill out and return to them, and they were -- from this survey, they were trying to get a general feel for the availability of future product and get a feel of what

pricing was and what kind of support there were for complimentary products for that memory type.

Q. Let me ask you to turn, if you could, please, to page 2, and let me direct your attention first to the first column, Chip Set Compatibility, and further direct your attention down to the third row reading "Rambus," and it reads there, "Intel Camino and Carmel do not know of other chipset support available in 1999."

Do you see that?

A. Yes.

Q. Now, at the time that you received this in December of 1998, what was your understanding, if any, of the import of that statement?

A. Intel -- Camino and Carmel were chipsets from Intel, and historically Intel has a very large market share of chipsets for the whole market, so it showed that they supported Rambus for use in certain applications.

Q. The row below that reads "DDR," and in the Chip Set Compatibility box, it reads, "PC133 chipset players are looking at DDR as the next step, 2H99 schedules. Several PC/Server/WK companies already in progress with internal chipset designs."

Again in the 1998 time frame, what was your

understanding, if any, of the import of that statement?

A. There were several chipset companies that were working on or had worked on PC133 chipsets at that time, and they were looking at including DDR on that chipset or migrating that chipset in the future to support DDR.

Q. Now, as of December 1998, had Micron actually begun production of DDR SDRAMs?

A. No, I don't believe we were producing it yet.

Q. Was it your understanding, then, that as of December 1998 that certain chipset companies had begun internal designs before Micron began to manufacture any of the DDR SDRAMs?

A. Yes.

Q. If I could direct your attention to the third column, Est. Pricing vs. PC100.

Do you see that column?

A. Yes.

Q. And then within the third row, Rambus, it begins, "RDRAM cost."

Do you see that?

A. Yes.

Q. And then in the fourth row, under DDR, it begins, "Cost is about."

Do you see that?

A. Yes.

Q. Now, did you have an understanding as of December 1998 why when Dell asked about pricing, Micron responded in terms of cost?

A. Yes.

MR. PERRY: Your Honor, there has been no foundation laid that he participated in the preparation of this chart. I don't mind the answer if he participated in the preparation, but that wasn't asked.

JUDGE McGUIRE: I have to sustain that if he hasn't been involved in the preparation of the chart. So, restate, Mr. Oliver.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, during the 1998 time frame, were you involved in responding to customer questions with respect to future Micron products?

A. Yes.

Q. During the 1998 time frame, did customers ever ask you questions with respect to cost of future products?

A. Yes.

Q. And in the 1998 time frame, did customers ever have some questions about pricing of future Micron products?

A. Yes.

Q. Now, with respect to customer questions to you, how did you respond to customer questions with respect to pricing future Micron products?

A. Normally, in terms of pricing, we would make that part of our sales function, to communicate price, so I primarily provided input as to what the cost would be, so I tended to communicate cost more as part of my role.

Q. Looking at page 2 of CX-2728, in the Rambus row, the third column, the entry reads, "RDRAM cost is about 50% higher than SDRAM in 1999, about 30% in 2000."

Do you see that?

A. Yes.

Q. Now, based on your understanding at the time that you received this in December of 2000 -- excuse me, in December of 1998, can you please explain your understanding of what this meant?

A. Sure. Again, this is a similar process as we went through before. Myself and Kevin Ryan would work with the design team and test team and try to understand what the relative costs were for the product produced and come up with an estimate of what we thought the cost of the product would be to produce

relative to in this case the bench -- the baseline was PC100 again.

Q. Now, focusing first on the year 2000, did you have an understanding as to why Micron was projecting the RDRAM cost to be 30 percent higher than SDRAM in the year 2000?

A. Yes.

Q. Can you please explain your understanding of why?

A. Sure. There were a few components to cost for the RDRAM that were higher than the PC100 that composed the aggregate increase. The -- the first and dominant component was the increased die size. For us, that was roughly in the range of 30 percent on its own. And there was also some higher packaging costs due to the use of FBGA and then -- and then micro BGA was actually even more expensive than that package. And then also, there was some concern about increased test costs.

Q. Can you please explain in a little bit more detail your understanding in the 1998 time period as to why the die size led to a higher projected cost for RDRAM?

A. Okay, can I clarify the question? You're asking why the die size was larger or why the die size leads to a higher cost?

Q. Let me break it up into two questions, please.

Let me ask first your understanding in the 1998 time frame as to why RDRAM would have involved a larger die size.

A. Okay, sure. There were several factors. One big factor, a little hard to explain, but the number of data bits that we had to bring out of the core or what we call the array was much larger relative to SDRAM. In the case of RDRAM, we were bringing out 128 bits out of the array, and just as a benchmark, SLDRAM was 64 bits and DDR was 32 bits and PC100 was 16 bits. So, that increased the actual size of the physical array.

And then, because we were bringing out so many bits, they eventually had to funnel down to a small number of outputs, and that required a lot of logic and additional circuitry needs to perform that function. So, that impacted the die size.

And in the RDRAM case, it also required a fairly sophisticated DLL, something that PC100 didn't have.

Q. Now, could you please explain your understanding in the 1998 time frame as to why that larger die size led to projections of higher costs for RDRAM?

A. Sure. The die size -- the way we produce and

manufacture product, we manufacture them on wafers, and a larger die size will give you less devices per wafer. We have a fairly constant cost to process, for a given process technology, for a wafer, so if you have a larger die size, you will amortize that cost among a smaller number of devices.

Q. Now, I believe that you also referred to packaging as one of the factors. Is that right?

A. Yes.

Q. Can you please explain your understanding in the 1998 time frame as to why the RDRAM packaging led to estimates of higher costs for RDRAM?

A. Sure. At that time, we were using for SDRAM a package called -- TSOP was the common package, and that package was fairly insured from a manufacturing standpoint, so both the equipment and the materials to develop that package were quite inexpensive.

The RDRAM required a micro BGA package or in our case we were trying to fulfill most volume with an FBGA, because it was somewhat cheaper, but that package required -- which was relatively immature for manufacturing -- required some additional equipment investment and was going to -- we were going to be more inefficient, at least earlier on, in producing a part in that package.

Q. I believe the third element that you mentioned referred to test costs. Is that right?

A. Yes.

Q. Can you please explain your understanding in the 1998 time period as to why test costs associated with RDRAM led to estimates of higher costs for RDRAM?

A. Sure. To test the RDRAM device, it required higher speed testers with greater timing accuracy than, say, PC100, and first of all, we had a lot of capital investment to buy those testers, which were not -- we had some difficulty in buying enough testers to get the volume we needed, and one of the challenges with those testers is we couldn't get as much what we call throughput. We couldn't test as many devices in parallel. And some of the tests were fairly intensive because of the nature of the accuracy and the speed. So, there was some uncertainty on the test cost adder.

We knew for sure early on it was going to be more expensive to test. What wasn't clear to us was further out in time whether the higher speed operation of the device would allow faster test time to offset some of these other challenges. So, there was some uncertainty over the test number, although we believed early on it would definitely be higher.

Q. Focusing again on the Rambus row, third column

on page 2, there's a reference there to the RDRAM cost is about 50 percent higher than SDRAM in 1999, about 30 percent in 2000.

Focusing again on your understanding of that statement in the December 1998 time frame, can you please explain your understanding as to why the costs -- the RDRAM cost would be about 50 percent higher in 1999 but about 30 percent higher in 2000?

A. Sure.

MR. PERRY: Your Honor, excuse me, I believe the question should be what -- his understanding of why the projections were this way as opposed to why the costs should actually be that way. I believe he misstated himself.

JUDGE McGUIRE: Mr. Oliver?

MR. OLIVER: I'll restate it, Your Honor.

JUDGE McGUIRE: All right, go ahead.

BY MR. OLIVER:

Q. Can you please explain your understanding in the December 1998 time period as to why the projections of the costs for RDRAM would be about 50 percent higher than SDRAM in 1999, whereas the projections of the costs of RDRAM would be about 30 percent higher than SDRAM in 2000?

A. Sure. Initially -- so, in that time frame, we

would be just ramping up the product, and so we would be in fairly low-volume production early on, and our yields at various steps of the process would be lower, which is normal, what we call the yield maturity curve. So, we would have lower yields for things like packaging and for test and various steps of the process. So, basically that means we'd throw out more devices. So, we'd end up amortizing the cost amongst a fewer number of devices.

Some of those costs will improve as we increase volume, as we climb up the yield maturity, so we anticipate the yields of the device and the yields of test and packaging would improve, but then it approaches a point where it essentially flattens out, and the cost increase is dictated by the increase in die size, which is something that doesn't change with volume.

Q. All right. Now, going back to the three factors that you mentioned, I believe the increase in die size, the packaging and the test cost, which, if any, of those factors would decrease with volume?

A. The -- the package cost and the test cost would.

Q. If I could ask you to look at the fourth column, First Volume Availability, and if I could

actually direct your attention first to the last row, DDR. There's a reference there to 64-meg samples, now 64-meg 2.5 volt samples, second quarter 1999, 128-meg samples, second quarter 1999.

Do you see that?

A. Yes.

Q. Now, did you have an understanding in the December 1998 time period as to whether that reflected any change in Micron's projections compared to earlier projections as to when volume availability of DDR parts would be online?

A. I believe it would represent a slight delay in schedule.

Q. Do you have any recollection as to why in the December -- or in the time period between March and December of 1998 there was a slight delay in the projection of when DDR parts would become available?

A. Sure, and by "available," I assume you mean production volumes or samples?

Q. I mean production volumes.

A. Okay. Yeah, at that time frame, I think our samples came out just a little bit later on the 3.3 volt part than we had hoped. We were having some trouble meeting design schedules at that time. We followed that with another design, so we didn't expect

that to go into volume production by then. So, we followed that with another design that was a two and a half volt part at 64-meg. We also followed it with a 128-meg part. So, we didn't really expect to -- by this time, we didn't expect to ramp volume until we went to the 2.5 volt parts.

Q. And if I could direct your attention to the third line, Rambus, in the fourth column, under First Volume Availability, it reads, "Samples 2Q99, low volume 3Q99, high volume 4Q99."

Do you have any recollection as of the December 1998 time period as to whether that represented any change with respect to earlier Micron projections?

A. I'd have to go compare it to the earlier one. I think this was either pretty close on schedule at this time or slight delay.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

THE WITNESS: (Document review.)

BY MR. OLIVER:

Q. Mr. Lee, I have handed you a document that's marked as CX-2735. It bears the caption Micron DRAM Update dated April of 1999.

Have you had a chance to take a quick look through this document?

A. Okay, I have had a quick look.

Q. Okay. Do you need any more time to look at the document?

A. That's okay, I'm acquainted with the general contents of these documents.

Q. Okay. Do you recognize CX-2735?

A. Yes.

Q. Can you explain in general terms what CX-2735 is?

A. This is a sales tool, again, with a similar kind of information as we talked about before, updated monthly -- no, I'm sorry, a year and a month later. This one, because of the second bullet there, I believe this one we were preparing for a visit with HP Grenoble.

Q. If I could ask you to turn, please, to page 25. I don't want to belabor this, but if I could just simply ask in general terms, would the table on page 25 be interpreted in the same way as the table that we saw on the previous document?

MR. PERRY: Your Honor, given Friday's discussion, there's been no showing made that this witness has ever seen this before. I assume I'll be given the same leeway tomorrow in examining him without having to establish that he's seen it before or --

JUDGE McGUIRE: Well, let's establish that so you don't have to assume that you're going to have that leeway.

MR. OLIVER: Thank you, Your Honor.

MR. PERRY: I know it was Mr. Royall who was here, not Mr. Oliver, but that's --

JUDGE McGUIRE: No, let's just establish the foundation first, and then I'll entertain the objection if there is one.

MR. OLIVER: Sure, Your Honor, and I apologize. I'm trying to move a little too quickly here.

BY MR. OLIVER:

Q. Mr. Lee, with respect to CX-2735 generally, is this a document that you saw in the 1999 time frame?

A. You know, can I explain the background as to how these documents get generated? I think that will help clarify here.

MR. PERRY: Your Honor, I don't need it for my objection.

JUDGE McGUIRE: I'm sorry?

THE WITNESS: I think it might clarify.

JUDGE McGUIRE: All right, just one at a time, Mr. Lee.

MR. PERRY: I was just saying if he was doing that because of my objection, I don't need it. He was

offering to explain how they are --

JUDGE McGUIRE: All right, thank you, I understand.

All right, thank you, Mr. Lee.

Mr. Oliver, you may proceed in that context that we have just discussed.

MR. OLIVER: All right, thank you.

BY MR. OLIVER:

Q. Mr. Lee, let me see if I can ask one or two other questions that might help short-circuit this.

Is this a document that you used in the course of your official responsibilities during the course of 1999?

A. I used these types of documents.

Q. Did you use certain pages of this document in the course of your responsibilities?

A. Yes.

Q. If I could ask you to turn, please, to page 25, now, is this a page that -- that you understood as of 1999?

A. Yes.

Q. And again, I don't want to belabor this point, but would the diagram here on this page be interpreted in the same manner as the diagram that we reviewed in CX-2718?

A. Yes, it's just an updated version.

Q. Mr. Lee, if I could ask you to turn, please, to page 29, and if I could refer you to the two main bullet points here under the caption Micron's RDRAM Plans. First, "Decided not to develop the 64-meg/72-meg," and then second, "144-meg on 0.18," and I'll let you determine that figure, "process taped out on 4/5/99."

Now, before I proceed, let me ask, did you have an understanding of what that referred to in the 1999 time frame?

A. Yes.

Q. Could you please explain your understanding of what that referred to in the 1999 time frame?

MR. PERRY: Your Honor, there's been no showing that he ever saw this document or that he had any role in preparing it, and I just think that the rules ought to be the same for everybody.

JUDGE McGUIRE: I agree with that, and I'm trying to do that. I think I issued an order not too long ago on the chart in the Dr. Oh order. So, Mr. Oliver, can we stay consistent with this? I mean, he's jumping up on this every other time, so --

MR. PERRY: I apologize.

JUDGE McGUIRE: No, that's fine, you can do

that. I'm just saying, though, you ought to understand at this point what he's going to be saying each and every time, so let's lay the foundation, and if you can't, let's move on.

MR. OLIVER: Okay, thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, with respect to -- in fact, let me take page 29 and page 30 together, if I could, please. Did you review pages 29 and 30 of CX-2735 during -- during 1999 in the course of your responsibilities?

A. I would have provided input to those pages.

Q. Based on your understanding, then, can you please explain what is being described in the main bullet points on page 29?

A. Sure. We're informing the customer that we decided not to develop a 64-meg RDRAM and move directly to the 128-meg RDRAM instead and that we just at this time recently taped the part out, which means send it off for fabrication.

Q. Now, did you have an understanding in the 1999 time frame as to why Micron was moving to the 144-meg part?

A. Yes.

Q. Can you please explain your understanding at that time?

A. Sure. I was involved with that decision. We were looking at where we saw the market at the time frame. We thought Intel would have their chipsets available in support of this part, and we were also looking at a general migration of customers to higher density systems.

We also felt that RDRAM was suited for the workstation market, well suited for that, and that market in particular wanted a higher density device. That was based on feedback from our customers.

We also felt that if we continued to work on the 64-meg first and then went to the 128-meg, that our 128-meg part would be later than our customer requirements, so we short-circuited the 64-meg, if you will.

Then finally, we saw that there was some manufacturing cost advantages for us to go to that higher density part. It allowed us to produce more product given our fab resources. Due to limited resources we had for things like test and packaging, we felt we could produce more RDRAM products -- more RDRAM bits, I should say, and get more revenue by moving to this density.

Q. If I could ask you to turn to the next page, page 30, and looking at the last bullet point, "Lower

relative cost," is that what you're referring to in the final part of your previous answer?

A. It's -- yeah, it's referring to relative to the 64-meg. Okay, I'm sorry, can I qualify that? Per bit. So, lower relative cost per bit.

Q. Okay.

A. If that makes sense.

Q. If I could ask you to turn, please, to page 34. This is a page with the caption RIMM Issues.

Now, is this a page that you saw in the course of your official responsibilities during 1999?

A. Yes.

Q. Is this a page that you understood during -- at that time in 1999?

A. Yes.

Q. If I could direct your attention to the first bullet point under RIMM Issues, it reads, "Additional module costs."

Do you see that?

A. Yes.

Q. Can you please explain your understanding of the -- in the 1999 time frame of what was meant by additional module costs?

A. Sure. Regardless of the cost of the component itself, many of our customers buy the components in

modules, and the modules have maybe eight or 16 devices on the module, and so this is referring strictly to the -- some cost premiums for building a RIMM versus building an SDRAM type DIMM, and so this was strictly regulated to module cost increases.

Q. If I could ask you to turn, please, to the next page, page 35. This is a page with the caption Rambus Testers.

Do you see that?

A. Yes.

Q. Now, is this a page that you reviewed in the course of your official responsibilities during 1999?

A. Yes.

Q. And did you understand this page at that time?

A. Yes.

Q. If I could direct your attention to the second bullet point, it reads, "Limited tester availability."

Can you please explain your understanding in 1999 of what that referred to?

A. Sure. In order to produce and test the Rambus -- the direct Rambus DRAM, we had to buy testers that we didn't have. They were different, more higher performance testers than we had for S -- needed for SDRAM. So, we had to purchase these testers, and also other manufacturers had to purchase these testers, and

so there became somewhat of a waiting list, if you will, to receive testers, and there was some concern whether the industry had enough test capacity to test the RDRAM volumes that Intel was projecting.

Q. Now, underneath that, there are two sub-bullets, which read, "Requires we use multiple suppliers; Learning curve for each is different."

Can you please explain your understanding in 1999 of what that referred to?

A. Sure. In order to meet the total capacity that we felt would be our part of the market share of RDRAM product based on Intel's, you know, forecast of what kind of volumes they would need overall, we had to provide -- buy these testers, but we couldn't get enough from one particular supplier to meet the amount of production capacity, so we had to find multiple suppliers to purchase from.

There was also some concern that these testers were very immature, and I wasn't sure how well they would work yet and whether they adequately test the accuracy that was initially stated. So, we had mitigate some risk by buying more than one suppliers' tester in case the tester was not adequate.

And then the learning curve was that each tester has its own programming language, and it's

entirely different from a another tester. So, there is really no compatibility. So, the switching costs from one tester to another is quite high. So, we had to put different people doing software on different testers to test the same part.

Q. If I could ask you to turn next, please, to page 37. This is a page with the caption Direct RDRAM Packaging Strategy.

Do you see that page?

A. Yes.

Q. Now, is this a page that you saw during the course of your official responsibilities in 1999?

A. Yes.

Q. Can you please explain in general terms what is reflected on page 37?

A. Sure. We're describing Micron's strategy for packaging direct RDRAM product. Much of the industry was offering a micro BGA package, which we were also going to offer, but our primary package that we were going to deliver the product in was an FBGA.

Q. Based on your understanding at the time, why was Micron offering primarily an FBGA rather than a micro BGA package?

A. We felt that it would provide a cost advantage for us to do so, and we also felt that we could get --

deliver more product that way. We felt that we had more resources in place to deliver FBGAs versus micro BGAs.

JUDGE McGUIRE: Mr. Oliver, we've been going for about two hours. Would this be a good time for a break?

MR. OLIVER: This would be fine, Your Honor.

JUDGE McGUIRE: Let's take a ten-minute break.

(A brief recess was taken.)

JUDGE McGUIRE: We're on the record.

At this time, you may proceed, Mr. Oliver.

MR. OLIVER: Thank you, Your Honor.

May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked as CX-2737. I'll give you a minute to look through that document.

A. (Document review.) Okay.

Q. CX-2737 is a document with the caption Micron Technology, Inc., DRAM Product Update, May 1999.

Mr. Lee, have you seen CX-2737 before?

A. Yes.

Q. Is this a document that you saw during the course of 1999?

A. Yes.

Q. Is this a document that you saw in the course of your responsibilities at Micron?

A. Yes.

Q. If I could ask you to turn, please, to page 9. Page 9 has the caption Worldwide DRAM Units by Type and some information, and then if I could direct your attention to the lower left-hand corner, "Source: Semico Research Corporation, 04/99."

Do you see that?

A. Yes.

Q. In 1999, did you have an understanding of what Semico Research Corporation was?

A. Yes.

Q. And what was your understanding in 1999 of what Semico Research Corporation was?

A. They are third-party analysts, and they cover the semiconductor industry, including the DRAM industry.

Q. Now, during the course of your responsibilities at Micron in 1999 and thereafter, did you ever rely on outside sources of information?

A. Yes.

Q. And what sources of information did you rely on?

A. We collected market share projections and, you know, volume, revenue forecasts from various market analysts in composing -- that, along with input from customers and some of the complimentary suppliers, like the chipset people. We used that to come up with a basis of what we anticipated our market forecast would be.

Q. Now, was Semico Research Corporation one of the sources of that information that you collected in the course of your responsibilities?

A. Yes.

Q. And referring to the information set forth on page 9 of CX-2737, is that information that you relied on in the course of your responsibilities in 1999?

A. Yes.

Q. If I could ask you to turn, please, to page 10 of CX-2737, again, if you see the information in the lower left-hand corner, "Source: Semico Research, 5/99."

With respect to the information set forth on page 10, is this also information that you relied on in the course of your responsibilities in 1999?

MR. PERRY: Objection, leading.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, with respect to the information set forth on page 10 of CX-2737, what, if any, use did you make of this information during the course of 1999?

A. We used this as one of our inputs for projecting market share of different -- in this case in different technologies in the future.

MR. PERRY: Your Honor, if I could, he keeps responding with a "we." Mr. Oliver is asking about you, and I'm not sure it's clear to the witness that he's being asked about his own personal information.

JUDGE McGUIRE: Let me caution you, Mr. Lee, when he's speaking about you, you have to speak to your own personal knowledge of the question. So, try not to create any ambiguity when you say "we," because we don't know who you're talking about.

THE WITNESS: Okay.

JUDGE McGUIRE: So, to the extent you can, say "I" or whatever, and if you're not sure, you can ask Mr. Oliver.

THE WITNESS: Okay.

JUDGE McGUIRE: All right.

BY MR. OLIVER:

Q. Mr. Lee, in the course of your work at Micron, do you work together with other people?

A. Yes.

Q. Perhaps just then with respect to questions, if your answer refers to work that you do together with other people, if you could please indicate that specifically in your answer. Is that okay?

A. Sure.

Q. Referring to page 10 of CX-2737, focusing on your understanding of the 1999 time frame, can you please explain in general terms your understanding of what was reflected on page 10?

A. Sure. This is Semico Research's forecast at that time of the market share that different technologies of DRAM would reach, forecasted out to 2003.

Q. I was wondering if it was possible for you to explain in a little more detail exactly what's depicted in the chart, and perhaps -- perhaps we could take as an example 16-meg sync.

Do you see that on the chart?

A. Yes.

Q. If you look towards the upper left-hand part of the chart, 16-meg sync.

Do you see that?

A. Yes.

Q. Could you please explain your understanding in 1999 of what this chart reflects with respect to 16-meg

sync?

A. Sure. In 1999, it looks like 16-meg sync SDRAM was forecasted to be roughly 10 percent market share.

Q. I'm sorry, my question probably wasn't clear.

Focusing on your understanding in 1999 when you saw this page, could you please explain your understanding at that time of what this chart indicated with respect to 16-meg sync from 1996 to 2003?

A. Okay, I think I understand the question. My understanding at that time was that they were forecasting the percentage of the market that 16-meg sync would achieve over that time frame, and it shows some percentage increase or growth from '96 to '97 and slowly decreasing percentage of market share down to, say, 1999 and rapidly decreasing after that.

Q. And then do you see the reference to 64-meg sync?

A. Yes.

Q. And again, could you please explain your understanding of what was depicted in this diagram with respect to 64-meg sync?

A. Sure. Over the same time frame?

Q. Yes, please.

A. Okay, so '96 shows very little market share for 64-meg sync. Growing substantially, it looks like it

reaches its peak in 1999, and then it starts decreasing its market share over time after that.

Q. And if I could then direct your attention to the reference to 256-meg DDR toward the upper right-hand corner.

Do you see that?

A. Yes.

Q. Could you please explain your understanding at the time of what was depicted in this table with respect to 256-meg DDR?

A. Okay, at the time it was depicted it was a forecast of 256-meg DDR starting in around year 2000, an increasing market share on out through the forecast period of 2003.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2747 with a caption Micron DRAM Update, September 1999. I'll give you some time to look through this document.

A. (Document review.) Okay.

Q. Mr. Lee, have you seen CX-2747 before?

A. Yes, I provided input to the document.

Q. Is this a document that you saw in the late

1999 or early 2000 time frame?

A. Yes.

Q. And is this also a document that you used in your professional responsibilities at Micron?

A. Yes.

Q. Can you please explain in general terms what CX-2747 is?

A. It's an updated version of the previous documents we looked at, called Micron DRAM Update, and again, provided information to our customers on market conditions and on our product availability and our future products and technology roadmap.

Q. If I could ask you to turn, please, to page 40, I'd like to direct your attention to lines 3, 4, 5 and 6 on this table, beginning with 64-meg SDRAM through 512-meg SDRAM.

Do you see those lines?

A. Yes.

Q. And can you please explain just in general terms your understanding in the late 1999 time frame of what was illustrated in those lines?

A. Sure. This shows our plans for product availability on 64-meg, 128 and 256-meg SDRAM at that time. The code that's used for this chart, if you will, is similar to what we described in the previous

documents.

Q. Now, with respect to the 64-meg SDRAM part, what does that show?

A. It shows it's in production at that time, and it's a Y74A.

Q. Okay. If I could direct your attention to the next four lines, 64-meg DDR, 128-meg DDR, 256-meg DDR and 512-meg DDR, could you please explain in general terms what is reflected in those four lines?

A. Yes. It shows our plans for product availability on various DDR SDRAM products, once again using the similar code for identifying the sample and production dates of the products.

Q. And then two lines below that refer to two -- two lines referring to RDRAM. Do you see that?

A. Yes.

Q. Can you explain in general terms what's reflected in those two lines?

A. Yes, this is similar information, this time covering the 144 and 288-meg RDRAM products.

Q. If I could ask you to turn, please, to page 58, this is a document or a page of the document with a caption of DDR SDRAM Market Developments. The first bullet point reads, "DDR SDRAM is next step in SDRAM performance." Underneath that, a sub-bullet,

"Evolutionary improvement to SDRAM architecture."

Do you see that?

A. Yes.

Q. Now, in the late 1999 time frame, did you have an understanding of those bullet points?

A. Yes.

Q. Can you please explain what your understanding of those bullet points was in late 1999?

A. My understanding was that evolutionary improvement to the architecture referred to the fact that it's a relatively simple change from SDRAM, and the relevance of that is it was -- could be supported with a chipset that supported both DDR and SDRAM.

Q. Now, what, if any, was the relevance of the fact that a chipset could support both SDRAM and DDR SDRAM?

A. This was important to our customer, which was why we were communicating it. They have strong preference that as we have a new technology, they have to be able to have what they call a transition strategy, and during that time, they prefer to have a technology that they can develop a chipset that could support the old technology and the new technology simultaneously.

Q. If I could ask you to turn, please, to the next

page, page 59, and under the caption DDR SDRAM Design Transition, there's a diagram, SDRAM, with an arrow to the right, and DDR SDRAM, and underneath that, the first bullet point, "Same package as SDRAM; 66-pin TSOP-II."

Do you see that?

A. Yes.

Q. Again, the 1999 time frame, did you have an understanding of that first bullet point?

A. Yes, I did.

Q. Can you please explain your understanding in the 1999 time frame of that first bullet point?

A. Sure. It states that the DDR used the same package as the SDRAM and that the benefit of that is that in production we were -- we have adequate capacity or we already had capacity in place to produce it. It was a similar package, if you will.

To the customer, some of the importance of that is certain reliability in mechanical testing, they already had experience with that package.

Q. If I could ask you to turn, please, to page 65, and that is a page with the caption DDR Chipset Status. Again, is this a page that you understood as of late 1999?

A. Yes.

Q. Now, could you please explain in general terms your understanding of this page as of late 1999?

A. Sure. It was describing various companies' support of DDR with their chipsets.

Q. Now, to your understanding in late 1999, what, if any, was the relevance to chipset support for DDR?

A. The chipset is a complimentary product, that you need to have the chipset in place typically for -- at least for the computing market to use the memory, and so it showed that there was available complimentary product.

Q. If I could ask you to turn, please, to page 68 of CX-2747. This is a page with a caption RDRAM vs. SDRAM Cost, and underneath that is a table.

Now, did you have an understanding of page 68 as of the late 1999 time frame?

MR. PERRY: Your Honor, if I could, please, I've just noticed that if you look at the pages in the document itself, pages 66 through 68 of the document are missing, and since we're now into the part about RDRAM, I just want to note that for the record.

JUDGE McGUIRE: Well, let's get that straightened out. Is it only, you know, from your copy that it's missing or why don't you all check and see?

MR. PERRY: It's in the exhibit copy, Your

Honor, that's part of the system. I'm talking about the page numbers that appear in the Power Point presentation itself.

MR. OLIVER: Your Honor, it appears that those pages are missing in all of our copies. I would propose we continue with this document, and in the meantime, we will see if we can find a document with those pages.

JUDGE McGUIRE: That will be fine, and we can take it up on Tuesday.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, with respect to page 68, and here I'm referring to the page number appearing in the lower right-hand corner, CX-2747-068, and it's a page bearing the caption RDRAM vs. SDRAM Cost and a table.

Do you see that?

A. Yes.

Q. In the late 1999 time frame, did you have an understanding of this page?

A. Yes.

Q. And could you please explain in general terms your understanding of this page as of late 1999?

A. Sure. It was to represent the relative cost of two products, RDRAM and PC133 SDRAM, relative to PC100

SDRAM, and it was to indicate how the relative cost would change or decrease over time in this case.

MR. PERRY: Your Honor, just for clarification, could we find out if he's talking about Micron's manufacturing cost when he says "cost"?

MR. OLIVER: I'll --

JUDGE McGUIRE: Well, if not, you can take it up on cross.

MR. PERRY: I just thought it would be easier.

JUDGE McGUIRE: If you want to accommodate him, Mr. Oliver, it's up to you.

MR. OLIVER: I'm willing to, Your Honor.

MR. PERRY: Thank you.

BY MR. OLIVER:

Q. Mr. Lee, in your previous answer, when you were referring to cost, what were you referring to?

A. Micron's manufacturing cost.

MR. PERRY: Thank you.

BY MR. OLIVER:

Q. Now, Mr. Lee, I note that the chart on page 68 ends as of 2H00. As of late 1999, did you have an understanding as to projections for RDRAM versus SDRAM costs after the second half of 2000?

A. Yes.

Q. And what was your understanding at that time as

to what the RDRAM versus SDRAM cost would be after the second half of 2000?

A. From our analysis, it appeared that it was going to approach about the 28 to 30 percent cost adder for our product.

Q. In other words, that that would continue on?

A. Yes.

Q. If I could ask you to turn to the next page, this is CX-2747-069, please. That's a page with the caption at the top RDRAM Die Size Adder.

Is this a page that you understood as of late 1999?

A. Yes.

Q. Can you please explain in general terms the information that's conveyed in the table in the top part of this page?

A. Sure. This looks at both SDRAM and RDRAM for a couple different device densities and also on a couple different process technologies, and it -- in this case, it looks at the die size as well as the increase relative to a baseline. In this case, the top half of the table, the baseline is 128-meg SDRAM, and the bottom half of the table, the baseline is 256-meg SDRAM.

Q. If I could direct your attention to the

right-hand column with the caption Die Size Adder, and the second line, 144-meg RDRAM, if you read across, it reads 40 percent, and underneath that, 128-meg RDRAM, if you read across, that says 27 percent.

Do you see that?

A. Yes.

Q. Could you please explain your understanding in the late 1999 time frame of what those figures meant?

A. Sure. For the 128-meg, I'll start with that one because it's easier, that shows that our die size adder is 27 percent larger than our 128-meg SDRAM.

Q. Now, if I could direct your attention to the bullet point at the bottom of the page, "Die size adder appears to be constant at ~25-30% for standard RDRAM."

Do you see that?

A. Yes.

Q. Again, could you please explain your understanding in 1999 of what that meant?

A. Sure. The question at hand was whether the increased die size for RDRAM relative to SDRAM would change over time, whether it would change if we increased the density of the device or whether it would change as we shrunk the device, went to a subsequent new process technology, and from our analysis, you see that we both looked at it at a smaller process

geometry, 0.15, and we also looked at going from a 128 to a 256-meg density, and in that case, we came back to roughly the same figure, on the order of 27-28 percent for the 128 and 256-meg device, or the 144 or 288-meg device would be about 40 percent.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2773. It bears the caption Micron Technology Overview, and in the lower left-hand corner, it reads, "4Q00."

Have you had a chance to look through this document?

A. Yes.

Q. Do you recognize this document?

A. Yes.

Q. Have you seen this document before?

A. I have -- I recognize this as foils from a larger document.

Q. Okay. I have questions only about one page. Why don't we turn directly to that page. It's page number 9.

Have you seen page number 9 before?

A. Yes.

Q. Is that a page that you've seen in the course of your professional responsibilities?

A. Yes.

Q. Can you please explain your understanding of what is meant by a designer's toolbox?

A. Sure, this is a location on our website that's meant to be a centralized resource of information. It's made available for our customers so they can -- essentially it's one-stop shopping, so they can go to one place and get access to all the information they need to design our product into their system.

Q. If I can direct your attention under the second bullet point, "Comprehensive source of information," the third is sub-bullet, "Standards and specifications," and underneath that, "JEDEC specifications, industry specifications."

Do you see that?

A. Yes.

Q. Now, do you have an understanding as to why that is included in the designer's toolbox?

A. Yes.

Q. What is your understanding for why that's included in the designer's toolbox?

A. That's meant, again, to benefit our customers. Many of our customers rely on the JEDEC specifications

to do their design, and so we put it there, a link to that, for their convenience.

Q. Mr. Lee, I'd like to shift topics, if we could, and talk a bit about the DDR2 standard.

Are you familiar with the term "DDR2"?

A. Yes, I am.

Q. Could you please explain your understanding of the term "DDR2"?

A. Sure. It's the next generation technology after DDR, and it follows from DDR.

Q. Now, how did you become familiar with DDR2?

A. I worked on the definition of DDR2. I was involved with JEDEC as they were defining that device.

Q. Now, do you recall when JEDEC began work on DDR2?

A. To my knowledge, it was roughly the 1998 time frame.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Go ahead.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked 2717. It bears a title of JEDEC Memory Futures Issues, March 1998, Bill Gervasi.

Have you had a chance to look through this document?

A. Yes.

Q. Have you seen CX-2717 before?

A. Yes.

Q. Can you please explain in what context you've seen this document before?

A. It was a JEDEC proposal.

Q. Did you observe that proposal?

A. I don't recall if I was at the meeting, but I've seen the data from it. I should qualify this. I don't think it was a proposal as much as an informational showing.

Q. Do you recall having received the document at some point?

A. Yes.

Q. At the time, did you have an understanding of the contents of CX-2717?

A. Yes, I did.

Q. If I could ask you to turn, please, to page 8, the caption reading, "Compatibility Between Generations," and the first bullet point reads, "Need to overlap generations, e.g., SDR to DDR, therefore, change must be evolutionary."

Do you see that?

A. Yes.

Q. Now, did you have an understanding of what Mr.

Gervasi was explaining in that bullet point?

A. Yes.

Q. What was your understanding at the time of what was reflected in that bullet point?

A. He was addressing me to have the overlap generations to cover what I talked to before about the transition strategy, so they could build chipsets that would support both the old technology and the new technology.

Q. If I could then ask you to turn, please, to page 13, this is a page with the caption Summary.

Again, at the time, did you have an understanding of what was being reflected on this page?

A. Yes.

Q. First of all, do you see there are a couple of references on this page to DDR++?

Do you see that?

A. Yes.

Q. What was your understanding at the time of what was meant at the time by DDR++?

A. It was meant as the next technology beyond DDR, which ultimately became DDR2.

Q. The first bullet point there reads, "Evolution, not revolution."

Do you see that?

A. Yes.

Q. And what was your understanding of what was meant by that bullet point?

A. He was -- he was stating that it needed to be an incremental change to DDR, needed to be something that looked fairly similar to DDR.

Q. Then the next bullet point reads, "One controller supports DDR and DDR++."

What was your understanding of what was meant by that bullet point?

A. He was expressing the requirement to have a controller that could support both technologies, the older one and the newer one.

Q. The next bullet point reads, "Compatible modules with DDR and DDR++ at low performance level."

Do you see that?

A. Yes.

Q. What was your understanding of what was meant by that bullet point?

A. He was expressing a desire to try to improve the transition ease by developing a module that was pin-compatible with DDR, that may have a lower performance level to start out with, but would help ease that transition strategy going to the new technology.

Q. Now, what, if any, involvement did you have with respect to DDR2 after March of 1998?

A. I worked on DDR2 with JEDEC and in turn with Micron for some time after that.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2745. Have you had a chance to look at this document?

A. Yes.

Q. And do you recognize this document?

A. Yes.

Q. What is it?

A. This is an email that covers -- has an attachment, and the attachment is a summary of a Future DRAM Task Group meeting that is a subcommittee within JEDEC working on DDR2.

Q. Did you receive this email in about August of 1999?

A. Yes.

Q. Did you review the attached document at the time you received it?

A. I was in attendance at the meeting, I believe, so I don't recall if I -- I probably scanned it, but I

was watching it as it was getting created.

Q. Oh, okay. At the time that you were watching the document being created, did you have an understanding of the contents of the document?

A. Yes.

Q. If I could ask you to turn, please, to page 7 of CX-2745, and there's a page with the caption Current Task Group Consensus.

Do you see that?

A. Yes.

Q. Can you please explain just in general terms your understanding at the time of what was reflected on this page?

A. Sure. The task group consensus was the consensus of the task group at that time as to what features would be included or excluded from the DDR2 part.

Q. Now, what, if anything, happened between March of 1998 and July of 1999 with respect to the items listed on page 7 of CX-2745?

A. I'm not sure I understand the question, what happened to the items?

Q. Well, I guess I'm trying to understand whether the consensus that's listed on page 7 represented a consensus that existed as of March of 1998 or a

consensus that developed between March of 1998 and July of 1999 or some other factor.

A. It's a consensus that developed from March '98 to July of 1999.

Q. If I could direct your attention to the first bullet point, it reads, "DDR Based."

Do you see that?

A. Yes.

Q. Now, can you please explain your understanding at the time of what that bullet point meant?

A. Yes, it means it's based on DDR and would be double data rate.

Q. If I could ask you to turn to the previous page, page 6, there's a caption there that reads, "Concerns List Status."

Do you see that?

A. Yes.

Q. Can you please explain in general terms your understanding of what was reflected on page 6 of CX-2745?

A. Sure. These were items that either were concerns for us now that we either had solved or concerns that we needed to do further work on.

Q. Now, if I could ask you to turn, please, to page 5 of CX-2745, and again, if I can ask you for a

description of your general understanding at the time of what was reflected on page 5.

A. Yeah, these were the schedule targets for completion of various milestones in the standardization.

Q. Did JEDEC, in fact, meet those various milestones?

A. I believe they were -- the schedule was delayed somewhat.

Q. Now, Mr. Lee, if we could, I'd like to turn to the year 2000 time frame, and let me ask first, at some point, did you become aware that Rambus was asserting that it had patent rights with respect to certain technologies contained in SDRAM and DDR SDRAM products?

A. I became aware at -- towards the end of '99 that Rambus claimed that -- they were asserting their patents against DDR and SDR against Hitachi.

Q. And how did you become aware of that?

A. There was information out I believe in the press, and then in early 2000, there was announcement of a lawsuit, and then there was more information available at that time.

Q. Did you have an understanding in the year 2000 time frame as to what particular features in SDRAMs or DDR SDRAMs Rambus claimed fell under the patent rights?

A. After the litigation became official in 2000, they announced they were pursuing Hitachi, then there was information available as to what features -- what patents in particular that they were trying to assert.

Q. And what was your understanding of what those features were?

A. Those features were programmable burst length and programmable CAS latency for both SDR and DDR, and it was on-chip DLL and double edge clocking for DDR.

Q. Now, during the year 2000 time frame, did you consider what alternatives might be available for those four features?

A. Yes.

Q. Based on your understanding in the year 2000, did Micron take any steps to propose alternatives to JEDEC for those -- those four features?

A. Yes, we made some proposal at JEDEC to try to change those features.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2758. It has a caption that says Simplifying Read Latency for DDR II, and in the lower left-hand corner, "JEDEC, March 2000, Kevin Ryan."

Mr. Lee, do you recognize this document?

A. Yes.

Q. What is this document?

A. This was a JEDEC proposal that Kevin Ryan prepared that I reviewed to go to JEDEC to try to offer some alternatives to programmable latency for SDR, DDR and DDR2.

Q. Now, when you say you reviewed this, did you review it in the March 2000 time frame?

A. Yes.

Q. Did you provide any feedback to Mr. Ryan with respect to this document?

A. Yes, I believe I did some minor edits.

Q. Now, what was your understanding, if any, of the purpose of this presentation?

A. The purpose of this --

MR. PERRY: Your Honor, excuse me, I just want to make sure -- and I'm basing this on the deposition testimony of this witness and the objections made at the time by Micron's counsel -- I want to make sure that his understanding is not based on any information he got from counsel, because we were generally barred from getting into his understanding if it was a design-around issue. So, I just want to make sure that we're at least not inadvertently getting into

privileged information.

JUDGE McGUIRE: Mr. Oliver, do you want to --

MR. OLIVER: I'll withdraw the question, Your Honor.

JUDGE McGUIRE: Okay.

BY MR. OLIVER:

Q. Mr. Lee, if I could ask you to turn to page 2 of CX-2758, the first bullet point on page 2, "The objective of this presentation is to propose an approach for reducing the complexity and cost associated with read latency operation described in the current DDR II specification."

Do you see that?

A. Yes.

MR. OLIVER: Your Honor, and I will have a question after this.

BY MR. OLIVER:

Q. The second bullet point reads, "The first part of the presentation discusses possible methods for eliminating programmable read latency from existing SDR and DDR devices; this discussion serves as useful background for the DDR II proposal."

Mr. Lee, what I'm trying to understand is that on the cover, it refers to DDR2, and yet here on page 2, it makes reference to SDR and DDR as well as DDR2,

and actually, let me ask one clarification question first.

The reference to SDR on page 2, that refers to the SDRAM standard. Is that right?

A. Yes.

Q. And what I'm trying to understand is whether this presentation was directed at the SDRAM and DDR SDRAM standards as well as DDR2 or was it directed just at the DDR2 standard?

A. It was directed at all three.

Q. If I could ask you to turn, please, to page 3, and under the caption Avoiding Programmable Latency in SDR/DDR SDRAMs," the second bullet point reads, "Users typically operate a device at the lowest (fastest) read latency possible at a given operating frequency."

Do you see that?

A. Yes.

Q. Can you please explain your understanding at the time of what was meant by that bullet point?

A. Yes. It meant that for a given clock rate that they were using the device, they would try to operate at a CAS latency that was the lowest acceptable for that clock rate given the device capabilities.

Q. Now, what, if any, was the relevance at that point to his presentation?

A. The relevance was that for a given clock rate, they normally didn't change the latency. They worked with a latency -- one common latency for that clock rate.

Q. If I could direct your attention to the next bullet point, it reads, "DIMMs are typically designated as being for one combination of operating frequency and read latency."

Do you see that?

A. Yes.

Q. Can you please explain your understanding of that bullet point at that time?

A. Sure. What he's referring to is that there was a trend for, say, a PC100 DIMM, there would be typically say a CAS latency of two module, and that's what we typically shipped, and then similar trend with DDR. So, he's saying that typically, although these things were programmable, there was really one operating frequency and latency that was being used for a given system.

Q. And then if I could ask you to look at the fourth bullet point, it reads, "Vendor testing at multiple latencies for a given operating frequency adds unnecessary cost."

Again, could you please explain your

understanding as of the March 2000 time frame of what was conveyed by that bullet point?

A. Sure. What he was conveying was that as a manufacturer, we had to test all combinations of frequency and latency, a similar concern we had all the way back to the SDRAM-Lite days, and I testified to that earlier. So, he was saying this adds costs for us to test this if it's not being used and that, therefore, it would be unnecessary.

Q. If I could ask you to turn to the next page, page 4, again with a caption Avoiding Programmable Latency in SDR/DDR SDRAMs, and the top bullet point reads, "One approach: offer devices with a fixed read latency."

Do you see that?

A. Yes.

Q. Can you please explain your understanding at the time of what was being proposed here?

A. Yes. What was being proposed was that there would be one latency but not be programmable.

Q. So, in other words, that would be a fixed latency?

A. Correct.

Q. If I could ask you to turn, please, to page 6 of CX-2758. Again, under the caption Avoiding

Programmable Latency in SDR/DDR SDRAMs, the first bullet point on page 6 reads, "Another approach: offer devices with programmable operating frequency; each operating frequency range has a fixed read latency associated with it."

Can you please explain your understanding at the time of what was meant by that paragraph?

A. Yes. My understanding was that the proposal was to have a programmable frequency instead of a programmable latency, and for a given operating frequency it would -- it would have a latency associated with it.

Q. Now, if we could ask you to turn, please, to page 8, and this is a little bit difficult to read in the hard copy. I don't know if we can make it out or not, but I'd like to direct your attention in the diagram to the -- the next to bottom box that consists of about three rows.

MR. PERRY: I think that's the worst we've seen. Eight weeks.

JUDGE McGUIRE: And we've seen some bad ones.

BY MR. OLIVER:

Q. Mr. Lee, are you able to make that out on the computer screen?

A. Not from the computer screen, no.

Q. Okay. Can you make it out on the page in front of you?

A. I can't read it well from this page. I know what the nature of this foil was, though, if that helps.

Q. Okay. Well, based on your recollection, I was trying to understand what is being depicted generally in this diagram, but with particular reference to the box that's been highlighted, and if you could explain that based on your recollection, please.

A. Sure. He was --

MR. PERRY: Your Honor, I will just object for the record to the use of the illegible documents with this witness.

JUDGE McGUIRE: Unless you can put it in some sort of proper context, Mr. Oliver, I mean, how can we tell what it's saying?

MR. OLIVER: Your Honor, if you will bear with us just a minute, we might be able to find a more legible copy.

JUDGE McGUIRE: All right.

(Pause in the proceedings.)

MR. OLIVER: Your Honor, maybe I'll just move on. If we're able to locate the document, then we'll come back to it. If not, perhaps Mr. Perry would allow

me just a few minutes tomorrow morning to --

JUDGE McGUIRE: All right, very good.

MR. OLIVER: -- come back to this point.

BY MR. OLIVER:

Q. Mr. Lee, if I could ask you to turn, please, to the next page, page 9, and here there's a -- the caption The real problem: DDR II -- hold on just a minute.

If we could please pull up CX-2758, page 9.

Mr. Lee, with respect to page 9, the caption The real problem: DDR II, can you please explain just in general terms your understanding at the time of what the proposal meant on this page?

A. Yeah, he was trying to explain the CAS latency issue as it related to DDR2, and he was providing some discussion of the issues behind CAS latency as exists for DDR2.

Q. Based on your understanding, what was the reference to "the real problem" with DDR2 on this page?

A. My understanding, the reason Kevin worded it this way, he was concerned about bringing -- trying to bring changes for SDR and DDR and even DDR2 to the committee at this point of the process. He was concerned that the committee would -- would strongly reject it, perhaps with some hostility. So, he was

trying to -- I believe in his words -- trying to ease into it.

Q. Now, based on your understanding, what, if anything, happened with this proposal at JEDEC?

A. My understanding was --

MR. PERRY: Objection, lacks foundation. We haven't established he was present.

JUDGE McGUIRE: Sustained.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2766. It bears the caption Pin Selectable Posted CAS for DDR II, JEDEC, July 2000, Kevin Ryan.

Do you recognize this document?

A. Yes.

Q. What is this document?

A. This was another JEDEC proposal, this one Kevin Ryan also put together, to make a posted CAS pin selectable, and as you get into the proposal, it's also about tying latency to that.

Q. Is this a document that you reviewed in the July 2000 time frame?

A. Yes.

Q. And did you provide any input or any feedback

with respect to this document?

A. I think I just reviewed it.

Q. Did you understand this document at the time that you reviewed it in July of 2000?

A. Yes.

Q. If I could ask you to turn to page 3, please, under the caption DDR Proposal, the first bullet point, "Use a dedicated pin (or pins) on DDR II SDRAMs to select read latency (and therefore write latency as well)."

Do you see that?

A. Yes.

Q. And if I could also ask you to look at the last sub-bullet point on this page, "Multi-pin: Could be used to select specific latency values as well as whether to use Posted or normal CAS operation. Trade-off: Higher overhead for pins/traces; lower overhead associated with the mode register."

Do you see that?

A. Yes.

Q. I'm interested in the aspect of this related to select specific latency values. Now, could you please explain in a little bit more detail how this proposal would select specific latency values?

A. Sure. The idea was instead of using -- in the

multipin case, instead of using the mode register, the DC level of a pin coming into the device could be used to detect which latency to operate at, and also in one form of the proposal, whether to use posted or normal CAS operation.

Q. Now, how, if at all, did this proposal differ from the proposal of March 2000, CX-2758, that we looked at a moment ago?

A. In this proposal, he's suggesting using an external pin to control it with a level. In the prior proposal, there was -- there was really two proposals. There was just have a fixed latency, and then the other one was to program frequency.

Q. Now, do you have an understanding as to why Mr. Ryan was making a different proposal in July of 2000?

MR. PERRY: Yes or no, Your Honor. I'll object if he starts a narrative.

MR. OLIVER: Could you please answer that yes or no?

JUDGE McGUIRE: All right, I am going to ask you, Mr. Lee, as often times in the course of your answers, try to answer only the question and let's not go into anything else other than just what he's asked, okay?

THE WITNESS: Okay, sorry.

BY MR. OLIVER:

Q. If you could simply answer yes or no, as of July of 2000, did you have an understanding as to why Mr. Ryan was making a different proposal than the one that he made in March of 2000?

A. Yes.

Q. Can you please explain your understanding as of July of 2000 as to why Mr. Ryan was making a different proposal in July of 2000?

MR. PERRY: I think it calls for hearsay, Your Honor.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Lee, in the time period between March and July of 2000, were you involved in any discussions within Micron with respect to what, if any, proposal should be made to JEDEC concerning determining latency?

A. Yes.

Q. Can you please describe in a little more detail your role in discussions of that sort within Micron?

A. Sure. I was involved in discussions with Kevin Ryan of alternatives for -- or options for programmable CAS latency, and we described --

MR. PERRY: Your Honor, excuse me. I believe that there were objections on privilege grounds to

these very discussions and our going into them, and I may be mistaken, but I just want to make sure that -- because believe me, we are going to drive a truck through this door if it gets opened, so I just want to have everybody on notice that these are conversations where Micron's counsel were present about what we can do to design around Rambus' --

JUDGE McGUIRE: Micron has their counsel here. If there's a problem, he can state them. If there's not, I assume there is no problem.

MR. PERRY: I just want to put everybody on notice.

MR. BOBROW: Your Honor, this is Jared Bobrow from Micron. I do not know whether the question is calling for information that's privileged or not. I had understood it to be a question directed to technical discussions with his colleagues.

JUDGE McGUIRE: Well, I'm not here to determine whether it's privileged. That's -- you are going to have to ask the Court to ask if this question indicates if it is going into that type of information. So, it's going to be up to you, Counselor, to decide what's privileged and what isn't.

MR. OLIVER: Your Honor, perhaps I could withdraw the question and see if I can rephrase the

question in a manner that hopefully will avoid these problems.

JUDGE McGUIRE: Okay.

BY MR. OLIVER:

Q. Mr. Lee, I'd like to ask about any discussions that you participated in within Micron, but I would like you to exclude from your answer any discussions that occurred in the presence of counsel as well as any discussions that occurred pursuant to instructions from counsel.

Is that clear?

A. Yes.

Q. Okay. Now, excluding those two categories, did you participate in any other discussions within Micron concerning what, if any, proposals Micron should make to JEDEC for the -- with respect to determining latency in the DDR2 standard?

A. I'm sorry, I got lost in the question. Just the second part of it after excluding the other types of discussions.

Q. Sure, and feel free to take your time to consider the answer.

My question is, excluding discussions with attorneys and excluding discussions resulting from instruction from attorneys, apart from that, did you

participate in any discussions within Micron concerning what proposals Micron should make to JEDEC concerning how to determine latency in the DDR2 standard?

A. Yes.

Q. Can you -- and again, without referring to any discussion with counsel present or at the instruction of counsel -- can you please explain what discussions you participated in within Micron for the purpose of determining what Micron should present to JEDEC relating to determining latency in the DDR2 standard?

A. Sure. We worked together to try to identify some technical solutions, some alternatives that would work we felt for the application, and then Kevin prepared a presentation and brought those proposals in.

Q. Now, when you said "we" worked together, who are you referring to?

A. I'm sorry, Kevin Ryan and I.

Q. Okay. Now, again, excluding any discussions you had with counsel or excluding any -- excluding any discussions following instructions from counsel, did you have any discussions between March and July of 2000 as to whether Micron should present a second time its proposal to use a fixed CAS latency at JEDEC?

A. Not regarding fixed CAS latency.

Q. Did you have any discussions between March and

July of 2000 as to whether Micron should repeat the proposal it made to JEDEC of March 2000?

A. I had a discussion with Kevin related to what he felt should happen.

Q. Now, as part of that, did you also -- did you provide a recommendation as to whether you thought Micron should repeat its March of 2000 presentation?

A. I didn't make a recommendation.

Q. Did you have a belief at that time as to whether Micron should repeat its March of 2000 presentation?

A. I did.

Q. What was your belief at that time?

A. Based on Kevin's report of how the first showings went, my belief was that there was no opportunity there to be able to change that at JEDEC.

Q. During the year 2000 time frame, were you still involved in having customer contacts?

A. Yes.

Q. Can you please explain in a little more detail what types of customer contacts you were having during the year 2000?

A. Sure. It's similar to the prior years. I would have customer visits, either I would attend at the customer's location or they would attend at our

location. My scope was typically technical in nature; however, as part of that, we would exchange technology roadmaps and also discuss future DRAM issues and also discuss sometimes issues going on at JEDEC related to future DRAMs.

Q. Can you please explain a little bit more about the purpose of those meetings with customers from your point of view?

A. Sure. The purpose was to -- it's a two-way communication flow, for us to share our plans with the customer and also for them to share their plans with us, their requirements for their future systems, their needs and how our devices or our roadmap would line up with their needs.

And in the case of some of the companies, they were also interested in what was going on, the kind of activities going on at JEDEC relating to future memory technology.

Q. Now, during the course of your discussions with customers in the year 2000, did you develop an understanding as to reactions of customers to proposed changes in the SDRAM and DDR SDRAM standard?

A. Yes.

Q. And what was the understanding that you developed during the year 2000?

A. They --

MR. PERRY: Your Honor, excuse me, it calls for hearsay if he's being asked to testify about what people said to him who weren't in the courtroom, and I don't think his state of mind on this issue is relevant to anything.

JUDGE McGUIRE: Mr. Oliver, do you want to respond?

MR. OLIVER: Yes, Your Honor. It does go to his state of mind. It goes to his state of mind in terms -- at the time that he was discussing with others in Micron and making recommendations in terms of what proposals, if any, Micron should make to JEDEC with respect to changing the SDRAM and DDR SDRAM or the DDR2 standards.

MR. PERRY: But the problem is, Your Honor, he just told Mr. Oliver that he hadn't made a recommendation on the CAS latency proposal, and now he's trying to get around that.

JUDGE McGUIRE: Sustained.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-2769. It bears the title Considerations for DDR-II

Clocking Scheme and Data Capture, and the lower right-hand side reads "Terry Lee," and underneath that, "September 13, 2000."

Mr. Lee, do you recognize this document?

A. Yes.

Q. What is this document?

A. This is a JEDEC proposal for a clocking scheme for DDR2.

Q. Is this a presentation that you made?

A. Yes.

Q. If I could ask you to turn, please, to page 13, and on that page, under the caption Single Data Rate May Be Possible, the first bullet point reads, "Pre-fetch and data rate is the same as DDR, but with a full bandwidth single-edge clock."

Do you see that?

A. Yes.

Q. What did you intend to convey with that bullet point?

A. I was proposing no change to the architecture and data rate of the device. I was proposing to increase the clock frequency.

Q. And with respect to the reference to the single edge clock, what did you mean by that reference?

A. That the proposal was to use a single edge

clock as opposed to a double edge clock.

Q. If I could ask you to look at the next to the last bullet point on that page, the bullet point reads, "Today's silicon can handle single data rate frequency." Underneath that, the last bullet point, "400 megahertz clock chips are already available."

Do you see that?

A. Yes.

Q. Now, what did you mean by those two bullet points?

A. At the time, the target for the design was 400 megabits per second, and in a DDR type of clocking, that would correspond to a 200-megahertz clock used for data capture, but in this proposal, I was proposing a single data rate clock, which would be 400 megahertz, and I was -- I was pointing out that the process technology today could handle those kind of operating frequencies for the clock, and there were also clock chips available at those kind of speeds.

Q. Now, if I could ask you to turn, please, to page 21, and under the caption Recommended Action, the last bullet point reads, "Single data rate clocks."

Do you see that?

A. Yes.

Q. And again, what were you proposing here?

A. This was kind of the conclusion andy recommendation based on the proposal that we eliminate strobes and we go with single data rate clocks with a different clocking scheme, which is described inside the document.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: You may.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document marked CX-426. Do you recognize this document?

A. Yes.

Q. What is this document?

A. This is an email chain, but essentially it's the meeting minutes from a conference call, a JEDEC task group, to look at the clocking proposal that I had proposed earlier.

Q. And did you participate in this conference call?

A. Yes.

Q. And can you please explain in general terms the results of this conference call?

A. Sure. We analyzed technical details of the proposal, further explanation, discussed some concerns and some analysis and tried to identify different companies' preferences for this scheme and kind of what

to do next.

Q. Now, based on your recollection, do you recall whether there was any consensus as to whether a single data rate clock was technically feasible?

A. Yes, I recall.

Q. And what was your recollection?

A. It was generally considered feasible by most of the companies but not all.

Q. Now, do you have a recollection as to whether there was a consensus from the call in terms of what should be done next?

A. Yes, I recall.

Q. And what is your recollection?

A. We felt there was still a little further work that needed to be done, and we were going to try to explore the idea a little bit further, and we were going to prepare a summary at the next JEDEC meeting on the progress of our call.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. OLIVER:

Q. Mr. Lee, I've handed you a document that's been marked as JX-52, although on your copy, like mine, the number has been cut off at the bottom. It's difficult to read. In any event, this document is a set of the

minutes of the 42.3 committee meeting from December of 2000 in Hawaii.

Mr. Lee, do you recognize JX-52?

A. Yes.

Q. And were you at this meeting?

A. Yes.

Q. If I could ask you to turn, please, to page 45 of JX-52, and if I could ask you to look in particular at pages 45 through 50, do you recognize those pages?

A. Yes.

Q. What are those pages?

A. These pages are -- this is a presentation I did at JEDEC following the conference call to report the summary of the results of the call.

Q. If I could ask you to look also at pages 51 through 56, please -- excuse me, 51 through 58, this is a set of pages, in the upper right-hand corner it reads "Attachment I," and the first page has the caption DDR II Concerns List -- it's difficult to make out, but the first page has the caption DDR II Concerns List, and it's difficult to make out, but I believe the lower right-hand corner contains a logo of Samsung.

Do you recognize these pages?

A. Yes.

Q. Can you please explain in general terms your

understanding of what was reflected on these pages?

A. Sure. This was a presentation by Samsung, and they were actually addressing a number of issues concerning DDR2, some of the concerns and some of the preferences.

Q. Now, focusing on the issue of single versus double edge clock, do you have a recollection as to what Samsung was proposing with respect to the DDR2 standard?

A. Pardon me while I review this if that's okay.

Q. Certainly.

A. (Document review.) Okay. Yeah, I believe I recall what Samsung's proposal was.

Q. And what do you recall about the clocking scheme they were proposing?

A. Regarding the clocking, their proposal was somewhat based on our prior proposal, and they were trying to get a way -- with regards to clocking, two issues. They were trying to go to a single edge strobe and they were trying to go to a free running clock, single edge.

Q. Now, Mr. Lee, after this time, after December 2000, did you pursue further at JEDEC your proposal to use a single edge clock in the DDR2 standard?

A. Yes.

Q. And can you please explain what you did after December of 2000 with respect to your proposal?

A. Yeah, there were further discussions on it, and at one point a straw vote was taken, a straw poll, and there was not a lot of support, and eventually I believe there was a ballot for the use of strobes, which my proposal would have eliminated, and that use of strobes proposal passed or that ballot passed, so...

Q. Did you pursue the issue further after that?

A. No, at that point it became clear the consensus was to stay with the original strobe scheme for DDR2.

Q. Now, based on your understanding at the time, this would be the late 2000 to early 2001 time frame, what was your understanding of the advantages of using a single edge clock in the DDR2 standard at the time?

A. The advantages of a single edge clock?

Q. Yes.

A. For DDR2? There were several that were listed in my original presentation, but they included -- we felt it would have been easier to test using that and not having a burst through strobe. We felt that we would gain some benefits in the timing budget by not having to worry about duty cycle control of the dual edge clock.

Q. Now, focusing on the late 2000, early 2001 time

frame, what was your understanding at that time of the potential disadvantages to using a single edge clock in the DDR2 standard?

A. One of the challenges was to get adequate data rate or get a high enough clock frequency using a single edge clock. Perhaps the biggest disadvantage was that it wasn't like DDR, and so it didn't have a direct migration path. That was fed back to us from some customers.

Q. Can you please explain in more detail your understanding of why it was a disadvantage that using a single edge clock in DDR2 was not like DDR?

A. Sure. There was concern that it would be difficult to design a controller that would support DDR and then this new scheme as well.

MR. PERRY: Your Honor, excuse me, if he's talking about other people's concerns, we ought to have those people come in. I don't think that's what the question was calling for. Lacks foundation and hearsay.

JUDGE McGUIRE: You're talking about his answer, is that right, Mr. Perry?

MR. PERRY: Yes, I'm talking about the answer, Your Honor.

JUDGE McGUIRE: Are you asking then that it be

stricken or just noted?

MR. PERRY: Yes, Your Honor.

JUDGE McGUIRE: Mr. Oliver, do you want to respond to that?

MR. OLIVER: Yes, Your Honor. I asked him for his understanding. He provided his understanding.

JUDGE McGUIRE: Well, his understanding of what, other people's concerns?

MR. OLIVER: His understanding at the time as to what the potential disadvantages were of using a single edge clock. He at the time was proposing to JEDEC that JEDEC use a single edge clock in the DDR2 standard. He recognized in making that proposal that there were certain advantages, but he would have to overcome certain disadvantages, and I was trying to get to an understanding of what disadvantages he thought he would have to overcome in order to propose that JEDEC use a single edge clock.

JUDGE McGUIRE: Mr. Perry?

MR. PERRY: Your Honor, I understood the question to be asking for the technical disadvantages to this feature as opposed to asking him to speculate about why people might not like to do it or why they --

JUDGE McGUIRE: All right, restate the question, because now I'm not sure what you're asking.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, focusing again on the late 2000, early 2001 time frame, at the time that you were proposing that JEDEC adopt a single edge clock for use in the DDR2 standard, can you please explain why you identified that one of the disadvantages of using a single edge clock in the DDR2 standard was that it was not like DDR?

A. Sure.

MR. PERRY: Your Honor, my objection is that he is not qualified to talk about the state of mind of other people. If that's what he's going to tell us about, I am going to have to move to strike it, because there is no foundation for it.

JUDGE McGUIRE: All right, let's hear the answer.

THE WITNESS: Okay, the other -- I'm a little confused at the question now, but I think you're talking about the second disadvantage.

BY MR. OLIVER:

Q. Yes, that's right.

A. Okay. It is difficult to design a controller to support the future technology and the old technology with this kind of clocking scheme because it's so

different from the old technology's clocking scheme. It's a very difficult design to accommodate.

Q. Mr. Lee, I believe that you had testified earlier that during the 2000 time period, you continued to have various meetings with customers. Is that right?

A. Correct.

Q. And did that continue in early 2001?

A. Yes.

Q. Now, during the course of your meetings with customers in that time period, what, if any, understanding did you gain as to customers' desires with respect to the DDR2 standard?

MR. PERRY: Objection, Your Honor, calls for hearsay unless we have the customers come in. In fact, we have had a whole parade of them already.

MR. OLIVER: Your Honor, this --

JUDGE McGUIRE: Overruled. I'll hear the question.

MR. OLIVER: Thank you, Your Honor.

THE WITNESS: We had made customer visits, and they wanted to have one standard that they felt could be designed and controlled to deal with the transition strategies for DDR and DDR2 simultaneously.

BY MR. OLIVER:

Q. Now, Mr. Lee, with respect to -- if I could return for a moment to the issue of CAS latency, again with respect to the -- to the customer visits that you had during the course of 2000 and 2001, what, if any, understanding did you gain with respect to customers' desires concerning what they wanted with respect to the determination of CAS latency in the DDR2 standard?

MR. PERRY: Your Honor, my objection to that very question was already sustained on the CAS latency point.

JUDGE McGUIRE: Well, if it was, I guess I will have to do so again, right?

MR. PERRY: It was, Your Honor, the record will reflect.

JUDGE McGUIRE: Sustained.

MR. OLIVER: Your Honor, to the extent that any of the testimony calls for hearsay, I would submit that this is particularly reliable hearsay given that this falls directly within the scope of Mr. Lee's job responsibilities, and he was making decisions within his job responsibilities as well as decisions with respect to what to do with respect to JEDEC based on the information, and therefore, I would submit that that -- that the testimony should be admissible.

JUDGE McGUIRE: Well, it can't be reliable

hearsay. I mean, that's an oxymoron, is it not?

MR. OLIVER: I disagree, Your Honor. Hearsay -- there is different types of hearsay, and the reliability differs depending on the type of hearsay that it is, and this is hearsay that is not a casual communication, but rather, something that Mr. Lee relied on during the course of his job description.

MR. PERRY: Your Honor, I don't know if I need to re-argue it --

JUDGE McGUIRE: I can't hear you, Mr. Perry. Do you want to get closer to the microphone?

MR. PERRY: Your Honor, I don't know if I need to re-argue it or not, but we had AMD, one of his customers, Dell, Compaq, IBM. We had all the customers in here. If complaint counsel could have gotten this testimony from them, presumably he would have, and that's why the lack of it to me is suspect, because we are done now with all the customer witnesses. They should have been asked this question.

JUDGE McGUIRE: All right, that objection is sustained, as I held earlier, regarding CAS latency.

MR. OLIVER: Your Honor, pursuant to Rule 3.43(g), if I could, I'd like to proffer with this witness some testimony.

JUDGE McGUIRE: Go ahead, yes.

MR. OLIVER: I think it won't take long.

JUDGE McGUIRE: Go ahead.

MR. OLIVER: Thank you, Your Honor.

JUDGE McGUIRE: You will make it as an offer of proof, is that what --

MR. PERRY: Do you plan to ask the witness to testify?

MR. OLIVER: Yes.

JUDGE McGUIRE: The offer of proof is that you ask the question to preserve it on the record.

MR. OLIVER: Yes, that's right, Your Honor.

JUDGE McGUIRE: You're not trying to preserve the answer.

MR. OLIVER: Actually, yes, Your Honor, I would like to preserve the answer in the record. It would not be anything we could cite to based on Your Honor's rulings, but the answer would be there such that if the issue were appealed, it would not be necessary to call the witness back at some point in the future.

MR. PERRY: Well, you're not suggesting that this would be the basis for any proposed findings of fact or that you would argue this in any way.

MR. OLIVER: No, Your Honor, based on your rulings, we would not be able to cite to this in findings.

JUDGE McGUIRE: All right, I will hear it only on that basis, that it's being offered as an offer of proof and I guess preserved as a point of error for purposes of appeal.

MR. PERRY: Thank you, and I don't need to make objections during the course of this whatever it is.

JUDGE McGUIRE: Right.

MR. OLIVER: Thank you very much, Your Honor.

BY MR. OLIVER:

Q. Mr. Lee, during the course of your customer visits during the year 2000 and early 2001, did you develop an understanding as to customers' desires concerning determination of latency within the DDR2 standard?

A. Yes.

Q. And can you please explain what understanding you developed with respect to what customers desired with respect to determination of latency in the DDR2 standard?

A. Yes, they wanted to be as compatible as possible with DDR1.

Q. Focusing again on your understanding in the 2000 time period --

JUDGE McGUIRE: Okay, now Mr. Oliver, so that I'm clear, is that -- are you -- have you completed

your offer of proof and are you now going to other areas?

MR. OLIVER: No, Your Honor, this is a continuation of the offer of proof.

JUDGE McGUIRE: Then I need to know as to the point in time you're done with that.

MR. OLIVER: Yes, Your Honor.

JUDGE McGUIRE: How many questions do you intend to inquire about on that basis?

MR. OLIVER: Your Honor, I believe that the rest of my questions -- it won't be long, but I believe the rest of my questions today will be as part of the offer of proof.

JUDGE McGUIRE: All right, go ahead.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Based on your customer communications in the 2000 time period, do you have a -- any understanding as to -- actually, let me withdraw that, please.

Based on your customer communications during the year 2000, do you have any understanding of customer reactions to the proposal that Mr. Ryan made to JEDEC in March of 2000?

A. Yes.

Q. Can you please explain your understanding in

the year 2000 of customer reactions to Mr. Ryan's presentation?

A. My understanding is that it wasn't supported by the customers.

Q. Again, focusing on your understanding gained through customer contacts during the year 2000, can you please explain that?

A. Yes, the -- in the context I had with customers where that was discussed, there was just a preference to continue -- they already were designed in on all of these products, and they wanted to continue with the standard as it was.

Q. Now, focusing on Mr. Ryan's presentation of July of 2000, again, based on customer communications that you had in the course of your job responsibilities during the year 2000, did you have any understanding as to customer reactions to Mr. Ryan's presentation of July 2000?

A. I'm sorry, I'm going to have to have you read that back. I'm sorry.

Q. Certainly.

Did you gain any understanding through customer communications during the year 2000 as to how customers reacted to Mr. Ryan's presentation at JEDEC in July of 2000?

A. I don't recall if I gained any from customers on that particular presentation or not.

Q. Okay.

Your Honor, that ends the offer of proof, and that ends my questioning of the witness at this time.

JUDGE McGUIRE: Okay, thank you, Mr. Oliver.

Then this hearing will be adjourned this afternoon until Tuesday morning at 9:30 a.m., at which time we'll undertake the cross examination of the witness.

(Whereupon, at 5:20 p.m., the hearing was adjourned.)

C E R T I F I C A T I O N O F R E P O R T E R

DOCKET NUMBER: 9302

CASE TITLE: RAMBUS, INC.

DATE: JUNE 23, 2003

I HEREBY CERTIFY that the transcript contained herein is a full and accurate transcript of the notes taken by me at the hearing on the above cause before the FEDERAL TRADE COMMISSION to the best of my knowledge and belief.

DATED: 6/24/03

SUSANNE BERGLING, RMR

C E R T I F I C A T I O N O F P R O O F R E A D E R

I HEREBY CERTIFY that I proofread the transcript for accuracy in spelling, hyphenation, punctuation and format.

DIANE QUADE