The D0 Silicon Tracker

Ronald Lipton
For the D0 Collaboration
Fermilab, P.O. Box 500, Batavia, Illinois

1. Introduction

The D0 Silicon Tracker will be installed in the D0 experiment as a part of the upgrade of the Fermilab collider experiments for Tevatron Collider Run II. Major upgrades to the collider experiments are required to accommodate the increased luminosity and reduced bunch spacing to be provided by the Tevatron in Run II. The Upgrades to D0 will substantially improve our physics capabilities by providing precise tracking in a central magnetic field. Major components to the D0 Upgrade include:

- A two Tesla superconducting central magnet
- Scintillating fiber /silicon tracking system
- New trigger systems
- Improved muon identification

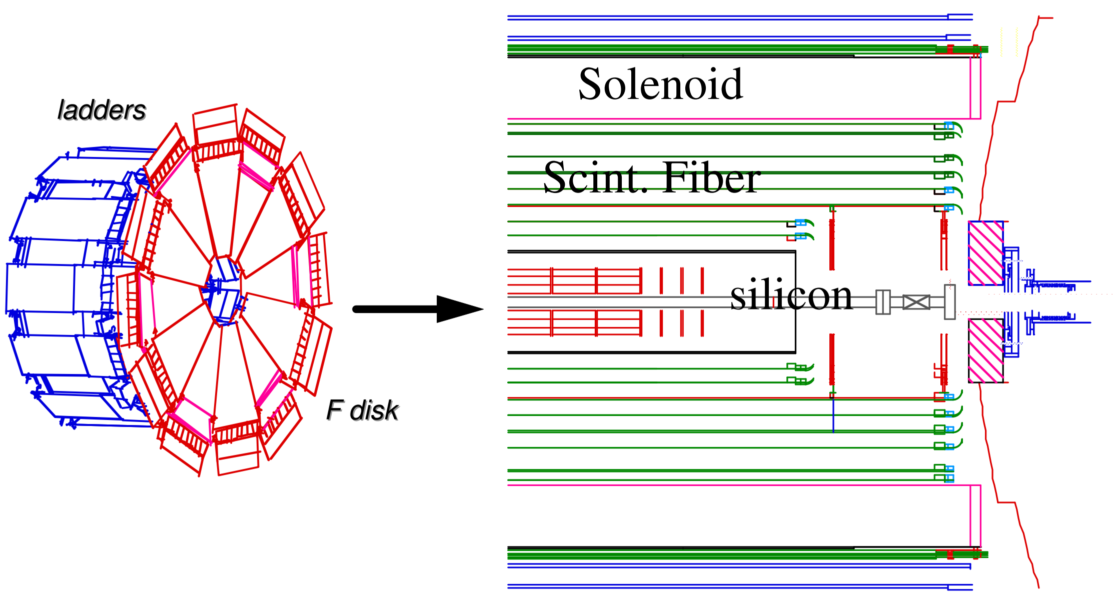

FIGURE 1. Schematic view of one half of the D0 tracking system showing the solenoid magnet, scintillating fiber and silicon systems. Also shown is an isometric view of a disk/barrel module

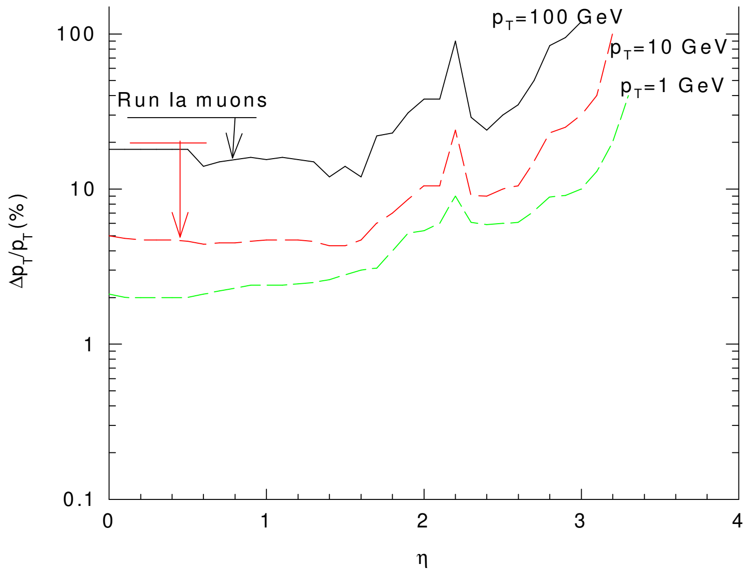

Figure 2. Momentum resolution for the D0 tracking system as a function of pseudorapidity.

Construction of the D0 Silicon Tracker is now underway. We will discuss physics and mechanical design considerations, experience with the electronics and detectors, as well as fabrication techniques and plans.

2. Silicon Tracking Design

Design constraints for the silicon tracking systems for D0 and CDF differ substantially from the existing silicon vertex detectors, which are primarily deployed at e^+e^- colliders. A major design consideration at Fermilab is the extended luminous region, which is expected to have a length (1σ) of 25 cm in Run II. This forces us to build an extended detector to provide reasonable acceptance for centrally produced particles. If, in addition, we want accurate tracking in the higher pseudorapidity regions (η~3) we have to accommodate tracks at a variety of angles. Optimum resolution for these tracks is achieved if the tracks traverse the detectors near normal incidence.
Our solution to this is the disk/barrel design shown in Figure 1. Tracks at low rapidity are measured primarily in the barrel detectors while the more forward tracks are measured in the disks. This preserves efficient tracking and secondary vertex reconstruction to η=3 while keeping good efficiency for the low η tracks from Top decay. To achieve this without sacrificing acceptance the barrel-to-barrel spacing must be kept as small as possible. There are several important features to the design:

1. The barrels are short (12 cm). This keeps the extrapolation for high η tracks passing though the disks reasonable and provides good rz vertex resolution for tracks with η>1.5. The short barrel length also keeps the preamp load capacitance small.
2. A barrel consists of 4 layers, each with two sublayers offset by ~ 6mm. The cooling channel runs between the sublayers. This design allows for the cables to the detectors to be routed between the sublayers, reducing the inter-barrel spacing. In addition there is substantial overlap between detectors in the sublayers and among layers. This should simplify the alignment process. The staggered arrangement also means that there is a 1-2 μm variation of the impact parameter resolution as a function of phi.
3. Interspersed disks are made of double sided detectors alternating around a thin cooling channel. The total barrel-to-barrel gap is about 8 mm.
4. All barrel readout electronics is mounted inboard.
5. Tracks at pseudorapidity greater than 1.5 will leave the tracking volume before passing through the full radial magnetic field. Momentum resolution for these tracks rapidly becomes unacceptable. The only way to recover resolution given a fixed tracking volume is increased precision of the track measurements. To achieve this large area "H disks" are mounted at the extreme end of the tracking volume. These disks provide precise $r\phi$ points on tracks with

rapidity between 2 and 3.5. The effect of these disks is shown in Figure 2. With the H disks the region of useful momentum measurement is extended from rapidity values of 2 to 3.5.

The baseline design of the silicon tracker consists of six disk/barrel modules, two 3 plane end disk modules, and four large area H disk modules. There are 793,000 channels of electronics.

3. Detectors

Detectors used in the D0 silicon tracker are summarised in Table 1. The outer two barrel/disk modules have single sided detectors on layers 1 and 3 the inner modules have 90-degree views as well as 2 degree stereo. All of the single sided devices have been received and tested. First article production detectors for the 2-degree and H disk types have been received.

View	Number	Type	Pitch	Comment
rφ	144	SS	50μm	polyimide passivation
rφ,2	336	DSSM	50μm, 62.5μm	Single p implant
rφ,90	144	DSDM	50μm, 153μm	2x multiplexing
±15	144	DSSM	50μm, 62.5μm	variable length strips
±7.5	384	SS	40μm	80μm readout pitch

Table 1. Detector types used in the D0 Silicon Tracker.

Figure 3 shows the results of testing for the single sided devices. Depletion voltage was measured in each detector using an alpha source. Devices with depletion voltages below 20V are rejected.

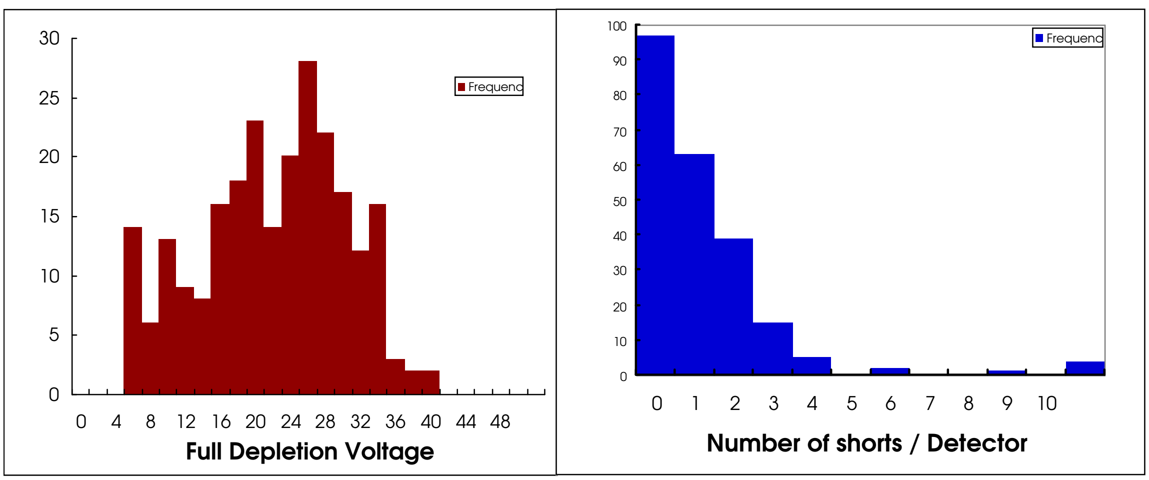

FIGURE 3. Results of probe testing of single sided D0 detectors. a) Full depletion voltage as measured by an α source. b) Distribution of the number of capacitor shorts per detector.

All detector types are tested for radiation hardness in the 8 GeV booster test facility at Fermilab. Single sided detectors with a single guard ring are quite robust. A ladder irradiated to 1 Mrad which initially depleted at 15V could be operated beyond 220 volts with no sign of breakdown. On the other hand early prototypes of F disks with a single guard ring showed signs of anomalous current draw at 100Krad. These currents typically had decay time constants of a few hours after exposure[1]. Detectors with multiguard

[1] R. Gomez

structures show no sign of these currents and all double-sided devices used in D0 will use a multiguard ring structure.

Bias for the double-sided detectors will be split, with the readout electronics operating at ground potential. Integrity of the coupling capacitors and immunity to the "black hole" effects (large areas of strips affected by shorted capacitors) are important considerations. We have had some indications of reduced capacitor breakdown voltage after wirebonding for ~5% of the capacitors tested. Studies are underway for optimisation of bonding parameters and wire thickness to minimise these effects.

4. SVX II E Chip and Readout System

The SVXIIE is a CMOS amplifier/analogue delay/ADC chip fabricated in the 1.2µm UTMC radiation hard process. It features a 32 cell pipeline, programmable test patterns and downloadable settings for ADC ramp, pedestal, bandwidth and polarity. The chip was designed to read out on each edge of a 53 MHz clock and operates beyond 70 MHz. Protection against "black holes" has been built into the preamplifier[2]. The chip has been fabricated and all die have been tested. Yields for the on-line digital test is 77%, an additional 13% fail more precise offline analysis of analog performance.

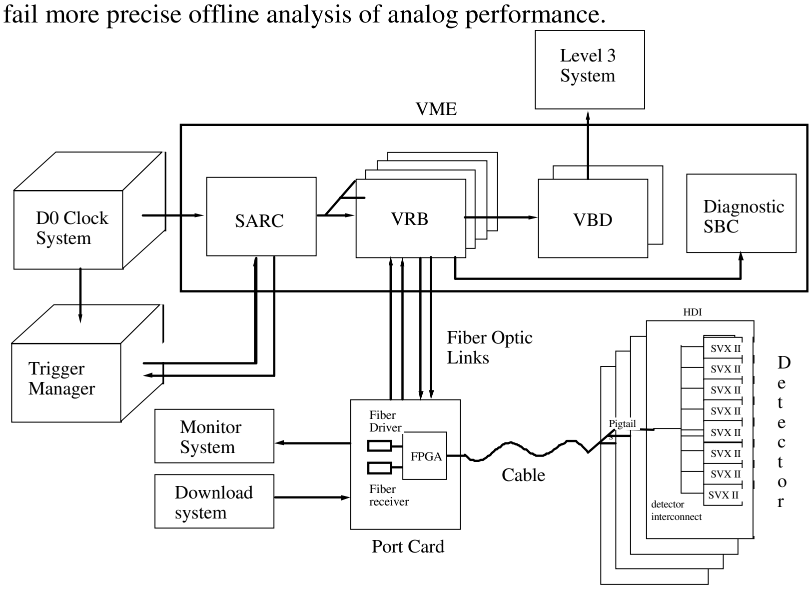

FIGURE 4. Readout system for the SVX II chip at D0.

The SVXIIE readout system is shown in Figure 4. SVX IIE chips are mounted on a mutichip module consisting of a two-layer flex circuit mounted on a beryllium metal substrate. The flex circuit (HDI) has 5 mil pitch and 3 mil via size and includes a "tail" which brings signals outside the barrel region. Connections at the outside of the carbon fiber support are made by a 0.5 mm pitch edge connector to a low mass cable which brings the signals to a transition card mounted on the central calorimeter cryostat. Signals are then sent via optical fiber to the VME buffer modules in the counting house.

With the exception of the low mass cable, this system was completely tested in the test beam in the summer of 1997. There are some important considerations to working with such a high speed analog/digital system. Careful attention must be paid to impedance matching and termination, data strobes must be properly timed, and the supplies, especially the detector bias supplies, must be properly bypassed. We found that the chip has a tendency to draw high current until properly initialised. In addition if the chip is put into a 'forbidden" state by failure of the control system it is possible to draw enough current to vaporise wirebonds. Fuses will be added to these lines in D0.

[2] R. Lipton, Vertex 96.

5. Mechanical Design and Assembly

The primary mechanical constraints imposed by the physics on the D0 tracker are the familiar ones of minimal mass, and precise alignment, in addition there are challenges imposed by the disk/barrel design which force us to move all electronics and cables inboard. Figure 5 shows the design of a D0 barrel ladder. Positioning of the ladder is achieved by precisely machined notches in the ladder beryllium heat spreaders which fit into posts on the bulkheads. Ladders are held to the posts by pins and can be removed if necessary. This design requires precise machining of the bulkheads and heat spreader as well as precise matching of bulkhead pairs. Figure 4 shows the deviation from nominal of the bulkhead post positions as well as the front to back offset of the posts on a bulkhead pair. We expect to place the ladders to 20μm and measure their positions to 9μm.

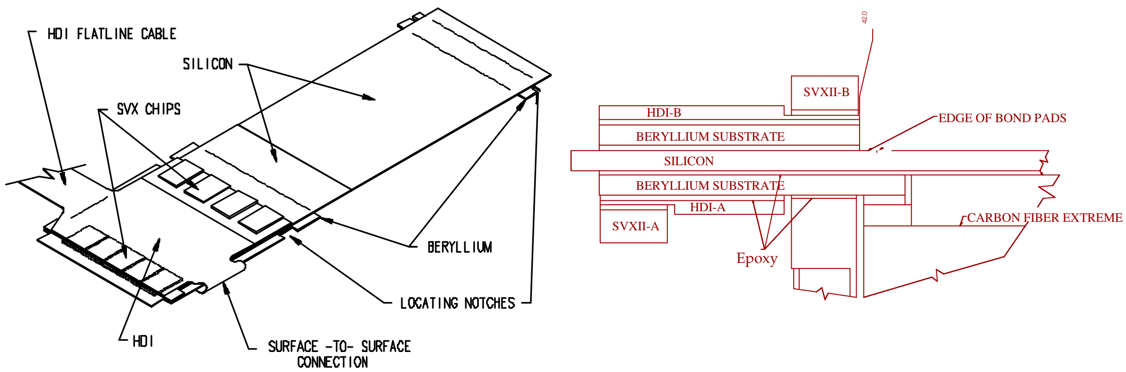

FIGURE 5. Isometric and elevation views of the D0 ladder.

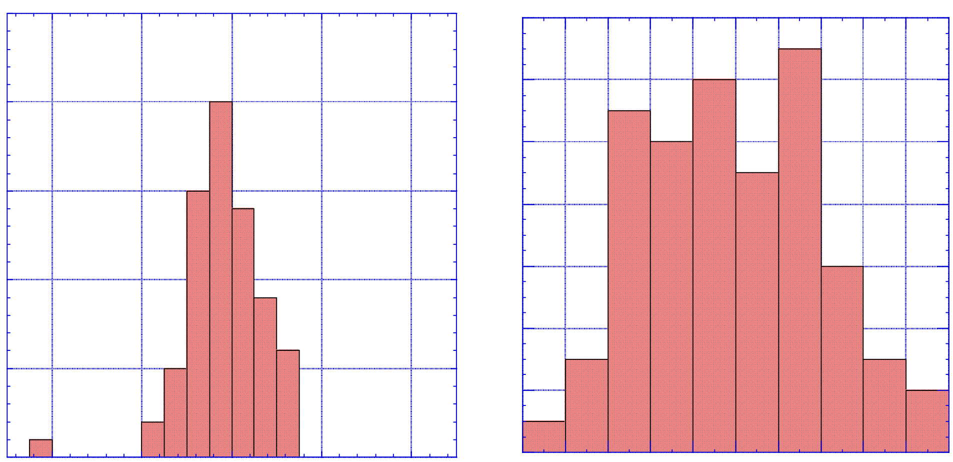

FIGURE 6. Measurements of the absolute (b) and relative (a) location accuracy for the ladder location features of the D0 bulkhead pairs.

Disks are staggered around a thin beryllium cooling pipe/support. The interspersed ("F") disks have their readout mounted at the outer radius whereas the "H" disks have inboard readout. All detectors are expected to operate at ~10 C, about 10 degrees above the temperature of the cooling water. The system has the capability to operate to -10 C with a water/glycol mixture.

The tracker will be produced in the Fermilab Silicon Facility. Production infrastructure, including wirebonders, coordinate measuring machines, and test equipment is now being commissioned. Tested detectors and HDIs are assembled into a ladder under a coordinate measuring machine. Trace alignment

accuracy is typically 1-2µm. Assembled ladders are then measured on an automated optical CMM to determine the relation of the location of strips to the mechanical features. These features are then measured with a touch probe after the ladder is installed in the barrel. Each ladder is burned in for 3-4 days and then every channel is tested using a 1064 nm LASER.
The detector support is in the form of a carbon fiber half-cylinder. Completed modules are placed into the half-cylinder and tested. The top half shell is then attached to complete the support. When the disk/barrel assembly is complete, the beam pipe is threaded through the center of the assembly.

6. Conclusions

The D0 Silicon Tracker is now under construction at Fermilab. The detector is intermediate in size between the previous generation of collider detectors and those being designed for the LHC.