Fermi National Accelerator Laboratory

Board Design Guide
For CDF
VME64 Extensions Modules
& VIPA Subracks

Draft 0.4

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(add VME64x mechanics problems solutions)

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I. Introduction

The purpose of the CDF Board Certifying Panel is to help the designer supplying Modules to CDF Run II insure that the experiment can maintain those Modules over the life of the experiment. The Panel is also trying to detect any inconsistencies between Modules from different groups which interconnect.

At the review the Panel will: a) provide the designer with immediate feed-back on any problems with the design, b) work with the designer in resolving any issues which may arise, and c) aid the designer with any potential problems which could cause the Module to fail the safety review.

A. Review Documentation

The designer shall supply the CDF Board Certifying Panel with document describing the purpose and theory of operation of the Module to be certified. This documentation should be provided to the Panel at least one week prior to the review.

1. Module Description & Block Diagram

The documentation should include: a) an overall description and block diagram of the Module, b) the operation of the Module as viewed from the VME bus, and c) a description of external data and/or control paths. The external data/control path description should include the following: a) signal levels, b) pinouts, c) connector and cable type, d) protocol, and e) timing diagrams. A complete schematic set for the Module is also to be furnished. If any Transition Module or other ancillary hardware is used with the board, documentation on it should be included following the guide lines set forth above for the main Module.

2. Maintenance & Support

The long term maintenance and support of all installed Modules at CDF is a priority issue. The review of the Module will require a description of the maintenance procedures and the person(s) responsible. Any special equipment or software required should be included.

3. External Requirements

The designer should describe any external requirements for the Module. These can include cooling, power, safety interlocks needed, etc. which require hardware external to the Module. These requirements can have impact on the infrastructure and need to be known as soon as possible.

4. Test & Acceptance

The designer should provide a general description of the proposed testing required to certify that the Module is functioning properly. Issues such as conversion of analog pulse input to digital voltage, time, charge, etc. with expected tolerance should be addressed. Also, any registers or other interrogations which when accessed from VME indicate that the Module is alive.

B. Other Documentation

The following documentation is not required for the review, but, needs to be provided to the Panel on a schedule to be mutually agreed upon at the review.

1. Documentation

Complete documentation is necessary for all Modules which operate in CDF. These documents will reside in the vicinity of the experiment control room and provide the operators and experimenters to diagnose problems which arise during data taking runs. The documentation should have title, identifying numbers, group responsible, and the designer and reviewers name.

2. Production Documents

A list of contracts for the construction of the Module needs to be furnished to the Panel when available. This documentation will potentially let someone other than the original designer construct additional units at a later date. Since people do not necessarily stay at an experiment for the duration this information can be critical.

3. Test Stand

If any test stands are required for the maintenance and calibration of a Module which will reside at FNAL this equipment needs to be documented. The documentation should include all hardware necessary for testing. Some standard hardware is available for testing and is included in the document list in section IX.

4. Diagnostic Software

Any software used to operate the test stand or test the Module in situ should be furnished and documented as to its use.

5. Calibration & Testing

The procedure for testing and calibrating the Module both on-line and off-line should be documented and included in the operator reference material.

6. Acceptance Test

The designer shall describe the detailed procedures used to test and verify the operation of the Module to the stated specification. This information should be sufficient so the Module can be tested at FNAL.

7. As-built Drawings

The designer shall supply drawings showing the actual construction of the Module. Any IC changes, trace cuts, added wires, etc. shall be indicated on the furnished drawings in a manner such that someone other than the original designer can build a copy of the Module. This is a long term operation issue for the experiment.

II. Implementation Check Lists

Sections **III through XII** can be used by the designer as a reference and check list for the Module to be reviewed by the CDF Board Certifying Panel. All items may not apply to all Modules. Other items can be added where necessary to document the device.

A. Check List — See sheet at end

III. Modules - Mechanical

Add various places differentiate between 6U and 9U Modules

A. Board

1. Thickness (6U & 9U Modules) — VIPA, Section 5.3, VITA23, Section 4.2

Board edge thickness shall be 1.6 ± 0.2 mm along the card guide edge and extending 2.5 mm from that edge. If milling is required to meet edge thickness it shall be milled on the solder side.
9U boards should be 2.4 mm thick elsewhere for greater stability. 6U boards can be 1.6 mm thick.

2. **Stiffeners (6U & 9U Modules)** **VIPA, Observations 5.3-j & 7.2-l**
VITA23, Sect. 4.3, VITA23-S Chapters 7 & 8

Two stiffener main designs are at FNAL. The first is a straight bar which attaches to the board behind the backplane connectors. This bar has a relief to clear the PCB except at the three attachment points. (Contact Terri Shaw for details.) The second design takes advantage of the mounting holes at the ends of the P1 and P2 connectors (and P3 if used). Two extra holes are added near the ends of P5/P6 (which do not have mounting ears). This bar is mostly over the connectors and does not interfere with the bus interface chips. (Contact Bill Haynes {ESE Department} for details)

3. **Warpage** **VITA23-S Chapters 7 & 8**

The board warpage at the connector edge must be controlled to keep the connector within ± 2.0 mm and ± 2º of true position. Elsewhere the warpage has to be controlled so no part of the board of components extend beyond the inter Module separation plane.

4. **Chamfers** **Standard Practice**

1.5 ± 0.5 mm top and bottom of connector edge at approximately 45°.

5. **Clearances** **IEEE 1101.10**

The maximum lead length from the component side is 3.1 mm (0.122 in). The back side shield is at 4.0 mm from the component side which clears the interboard separation plane by 0.07 mm. On the component side the maximum component height should not exceed 13.71 mm (0.540 in).

6. **RFI Fingers & Solder Side Covers** **IEEE 1101.10 & VME64x, Section 5.2.2**

Solder side cover necessary to avoid abrasion of EMI gasket on insertion or withdrawal. See pointers for other details. These covers can be purchased from Rittal.

7. **Area To Omit Circuitry (6U & 9U Modules)** **IEEE 1101.10**

No components are to extend into the top and bottom 2.5 mm along the board edge. ESD strips only are allowed along the edge inside this 2.5 mm band.

B. Connector Types

The part numbers given were believed to be accurate at the time of publication. Manufacturers periodically add new parts and/or change old part numbers. Before ordering connectors the designer is advised to contact the manufacturer to obtain the latest parts numbers.

1. **0.1 in (DIN)** **VME64x, Section 3.2.1 & VIPA, Annex A**
VITA23-S, Chapter 1

See also Harting catalog for new 160 pin VME connector.

2. **2 mm Hard Metric** **IEC 1076-4-101 & VME64x, Section 4.2.1 - 4.2.5**

See also AMP, ERNI and FCI catalogs for 2 mm connectors. Be careful to check pin lengths; see especially VME64x Rule 4.4. Do not mix manufacturers when configuring connectors P5/J5 and P6/J6.

3. **Specials** **9U x 400 mm**

For special connectors in the hard metric series see AMP, ERNI and FCI catalogs.

C. P0 Shields

1. Top — IEC 1076-4-101

Recommend top shield (row f) for better grounding.

2. Bottom (check interference) — IEC 1076-4-101

Bottom shield (row z) must be type which doesn't extend beyond the interboard separation plane.

3. Connections To Digital Common — VIPA, Chapter 9; VITA23-S, Chapter 5

D. Front Panel

1. Injector/Extractor/Locking Handles — 1101.10

Locking feature is not part of the IEEE 1101.10 standard. See Rittal catalog for this feature.

2. Rules When Using Injector/Extractor/Locking Handles (Modules & Transition Modules)

a) A front panel must always be used.

b) Lock washers must be used to secure the handles to the printed circuit board and front panel. Note that these may not be in the kit from the manufacturer.

c) A mounting bracket with lock washer must be used at or near the middle of the front panel to secure it to the printed circuit board.

d) The dimension given in IEEE 1101.1 for the separation between the top and bottom handle must be strictly adhered to prevent possible handle failures.

3. Front Panel Components & Electrical Isolation — VIPA, Chapter 9;

General rule is to only ground the driver end.

4. Ground — VME64x, Section 5.2.1 & VIPA, Section9.2 VITA23-S, Section 5.2

5. Indicators — VIPA, Section 5.4; VITA23-S, Section 7.4

6. Labels — VME64x, Section 5.2.3

7. Gaskets — IEEE 1101.10

8. Feedthroughs — VIPA, Section9.2; VITA23-S, Section 5.2

9. EMC Front Panel — IEEE 1101.10

10. Cable Shield Connections — Digital Links Document

Isolated & Not Isolated From Front Panel

11. Key Code (no duplicates) — VIPA, Chapter 10; VITA23, Appendix C

E. Subrack

1. **Grounding** **VIPA, VITA23, VITA23-S**

2. **Cable Routing & Support** **CDF, Design Specific**

   This item and the following one should be checked with the experiment (Steve Hahn) to avoid any unforeseen problems.

3. **Special Mechanical Requirements** **CDF, Design Specific**

4. **Cable Latch Shrouds** **9U x 400 mm**

   See data sheets from AMP, ERNI and FCI for optional rear latching mechanisms. These are only on the designer defined backplane.

F. Test & Repair

1. **Extenders** **Designer Specified**

   a) **Standard Connectors** **Designer Specified**

   b) **Special Connectors** **Designer Specified**

   c) **Split Unit (1&2 w/ special 3)** **Designer Specified**

2. **Test Fixtures**

   a) **Hardware** **Designer Specified**

   b) **Software** **Designer Specified**

   c) **Special Hardware** **Designer Specified**

   d) **Open Side Subrack** **Designer Specified**

IV. Modules - Electrical

Some of below may belong elsewhere.

A. Subrack

1. **Voltage Requirements** **VIPA, Section 8.4; VITA23, Section 6.3**

   9U CDF subracks have recommended P0 power pins.

2. **Current Requirements** **VIPA, Section 8.7; VITA23, Section 6.5**

B. Power Pins

1. **VME Power** **VME64x, Section 3.2.2 & VIPA, Table 8.4-2**
   VITA23, Table 6.3-2

DIN connector pins are rated at 1.25 A @ 60°C, 1.5 A @ 30°C. The hard metric signal connector pins are rated at 1.2 A @ °C, 1.4 A @ 30°C and the shield pins are rated at 1.0 A @ 30°C. Both ratings are for non-isolated pins.

C. Pin Outs

1. **VME64** — **VME64**
2. **VME64x** — **VME64x**
3. **Front End** — **CDF Note, Design Specific**
4. **Special** — **Design Specific**

D. Auxiliary Backplane

1. **Connector Types** — **VIPA, Annex A; VITA23-S, Chapter 1**
2. **PCB Connections** — **VIPA, Annex A; VITA23-S, Chapter 1**
3. **Shrouds** — **VIPA, Annex A; VITA23-S, Chapter 1**
4. **Cable Latch Shrouds** — **VIPA, Annex A; VITA23-S, Chapter 1**

   Direct attachment to the rear of the backplane can have cooling/air flow implications if Transition Modules are used.

5. **Backplane Thickness** — **VME64x**

   Cannot be greater than 6 mm thick. Should be at least 2.4 mm for stability.

E. Front Panel Connectors

1. **Grounding & Isolation** — **VIPA**
2. **Front Panel Attachment** — **Digital Link Document**
3. **EMI/EMC** — **VIPA, Chapter 9; VITA23-S, Chapter 5**

F. ESD Strips & Discharge Resistors

1. **Component Side** — **IEEE 1101.10**

   Along component side in card guide area. End 70 mm before front to disconnect from clip. Eliminates potential of ground loop.

2. **Two - 1 MΩ Resistors** — **VME64x, Chapter 8**

   Used to connect from ESD strip to board ground.

G. Inter-Module EMI Shielding

1. **Solder Side Shields (Modules & Transition Modules)**

   a) Use solder side shields whenever EMC gaskets are used on front panels or subracks.

   b) Can use metallic shield if insulated properly.

   c) Use Velcro if necessary to hold shield to printed circuit board in the center or other places as necessary. The corners and rear edge of the PCB have holes for brackets and connectors which are also used by the cover.

   d) Solder side shields for both Modules and Transition Modules are available from Rittal.

2. **Other Shields**

   Component side shield is easier to implement, however, needs insulation also. Possibly use FR4 with copper plane as shield and plated through holes at connection points. Be careful not to obstruct air flow.

H. Clocks

1. Clock Source	**CDF Doc?**
2. Crossing Counter	**Design Specific**
3. Synchronization	**Design Specific**
4. Error Detection	**Design Specific**

V. Modules - Power, Cooling & Protection

A. Power Density

1. **Component Location**

   Try for even distribution of power. Avoid hot spots.

B. Power Distribution

C. Power Dissipation Limits	**VIPA, Section 5.6; VITA23, Section 4.3**
D. Die & Module Temperatures	**VIPA, Section 5.7; VITA23, Section 4.5**
E. Air Flow	**VIPA, Section 8.10, Section 13.3** **VITA23-S, Section 10.10**

1. **Blockage**

2. **Air Deflectors for Hot Spots**

3. **Filler Panels**

F. Overvoltage & Overcurrent Protection	**VIPA Section 5.9; VITA23, Section 4.6**

Bill Haynes is currently writing up technical notes and conducting tests for proper overvoltage and overcurrent protection.

1. Proper Overvoltage Protection

Even though more tests are needed, it appears that to properly protect modules from overvoltage during a power supply failure, if you are using pico fuses one transorb is required to be paralleled at the downstream end of the fuse(s) per every five amps of fuse rating. Thus if you require 10 amps of +5 volts and choose to use a single 15 amp pico fuse, you must put three ICTE-5 equivalent transorbs in parallel to digital common (circuit ground) at the downstream end of the fuse. If you use two 10 amp pico fuses in parallel, you must use four ICTE equivalent transorbs in parallel, etc. Since ICTE-5 equivalent transorbs react in a few hundreds of picoseconds, this guarantees that the energy required to blow the fuse is less than the energy to destroy the transorbs.

2. Fusing Boards By Sectioning

Since tests have shown that ICTE-5 equivalent transorbs can sustain enough power for sufficient time (enough energy) to both protect circuitry from overvolatges and do so until five amp pico fuses open, fusing boards by sectioning is strongly recommended if no other problems are introduced by doing so.

Sectioning is dividing up the board circuitry into parts and fusing (and overvoltage protecting) each part individually. For example, if a board's +5V current draw is 14 amps the board's circuitry can be divided into four approximately equal current draw 'sections', each fused with a single 5 amp picofuse and each overvoltage protected with an ICTE-5 equivalent transorb on the load side of the fuse.

A potential problem exists with fusing boards by sectioning, especially if the board contains some MOS circuitry. Destruction of certain types of MOS components can occur if they are unpowered but have powered inputs. This can occur, for example, when a fuse opens in the section with these MOS components but other fuses in other sections don't open. These types of MOS components should also not be driven directly from external inputs.

3. Paralleling Pico Fuses

Initial studies and tests indicate no problem with paralleling pico fuses. Further tests on the effect of paralleling fuses during turn-on current surges are required.

4. Using Other Than Pico Fuses

Because other fuses may require more energy to blow than do pico fuses, it is strongly recommended that only pico fuses be used in conjunction with transorbs.

5. Current Rating Of PC Board Power & Ground Plane Traces

(To be added later.)

6. High Speed Signals and Sectioning Issues

When cutting power or ground planes there may be an effect on "high" speed signals. A signal which is over a plane induces a current in that plane which must arrive at the receiver in time with the driven signal, If these two current arrive out of time noise is generated and spurious signals may be generated by the receiver. Likewise, the driver has to receive the return current in time or signal distortion can occur.

These problem can be avoid by installing capacitors (typically 0.01 µF) across the cuts in the planes. Also, these capacitors are needed from each plane which has induced currents to the ground plane of the driver and receiver near these ICs. The spacing of the capacitors depends on the rise time of the signals. For a signal of rise time t_r the path difference between the driven signal and the induced signal should be less than l where $l = t_r/(4v_d)$ and v_d is the velocity of the signal on the board. For a 1 ns signal, a 1 in grid will provide an acceptable solution.

VI. Modules - Logical

A. Interface

1. Use of ETL Components	**VITA 2**
2. Bus Trace Length	**VITA 2; VME64x**
3. VME Bus Signals - Edge Killer Circuits	**VME64x**

B. Address & Address Modifier Latching — VME64; VITA23, Section 3.2

C. Interface Logic

1. Geographical Addressing, CRs & CSRs	**VME64x, Chapter 10**
a) SVX Module Addressing	**CDF Note**
b) Calorimeter Module Addressing	**CDF Note**
2. CR/CSR's	**VME64x, Chapter 10; VIPA, Section 4.4** **VITA23-S, Section 6.4**
3. VME64 Protocols	**VME64**
4. VME64x Protocols	**VME64x**
5. Non-standard Protocols	**Design Specific**

D. Event Data VME Readout

1. Data Mode	**CDF Note**
2. Diagnostic Mode	**CDF Note**

E. Initialization

1. Procedure	**Module Documents**

F. Required Registers

1. CSR

a) Base Address Register (BAR)

2. CR

a) Board ID: FNAL OUI is 00-80-55

G. Module Diagnostics

1. Registers	**Module Documents**
2. Test Logic	**Module Documents**
3. Calibration	**Module Documents**

VII. Modules - Software

A. VITA 25-199x API

B. Data Mode Code	**Module Documents**
C. Diagnostic Code	**Module Documents**

D. Module Characteristics

1. Read back	**Module Documents**
2. Register (Bit) Interaction	**Module Documents**
E. Initialization	**Module Documents**

VIII. Modules - Implementations

A. Low-Level Analog	**VIPA Annex G, VITA23-S, Chapter 3**
B. Powering & Shielding Recommendations	**?**

1. High-Current

2. High-Speed Digital

C. DC-DC Converters	**VIPA Annex H, VITA23-S, Chapter 4**

IX. Transition Modules - Mechanical

Refer to sections III, IV and V except where specific items are listed below

A. Alignment During Insertion Into Subrack

1. J2 Connector Shells

Need to use a J2 connector (can be empty) to properly align Transition Module.

2. J5/J6 Hard Metric Connector With & Without Self-Alignment

J5/J6 connectors come in both center keyed/alignment and no key versions. See Hard Metric data from AMP, ERNI and FCI.

X. Transition Modules - Electrical

Same as VME Modules

XI. Transition Modules - Power, Cooling & Protection VIPA, Section 7.4, VITA23, Section 4.4

Same as VME Modules except power is limited.

XII. Transition Modules - Logical

Connection to VME bus is not allowed.

XIII. Module & Transition Module Overcurrent & Overvoltage Protection

A. Overcurrent Protection (Fusing)

B. Overvoltage Protection (Transorbs)

C. Segmenting Voltage Planes On A PC Board Layout

XIV. Subracks

A. J3 (J5/J6) Backplane Manufacture

The auxiliary backplane should be a minimum of 0.125 inch thick for rigidity. It is not important to match the thickness of the J3 (J5/J6) backplane to that of the VME64x 6U backplane. The reference mounting surface is the front surface. The shrouds are manufactured with for different thicknesses of backplane and make shimming unnecessary. Special care must be taken that proper connector spacers, shrouds and pin lengths are chosen for J3 (J5/J6) backplane. **(give VME or IEEE spec references)**

XV. Useful Documentation

A. IEEE 1101.1 & IEEE 1101.10 Standards & IEEE P1101.11 Draft Standard

B. VME & VME64 Standards

C. VITA 1.1-199x - VME64 Extensions Draft Standard

D. VITA 1.3-199x - 9U x 400 mm Module Format Draft Standard

E. NIM/VME-P 9612 (VIPA) sometimes referred to as the “Green Book”

F. VITA 23-199x - VMEbus for Physics Applications Draft Standard (VITA23)

G. VITA 23-199x Supplement (VITA23-S)

H. VITA 25-199x - Software API Draft Standard

I. CDF Front End Module Design Information

See: www-cdf.fnal.gov/upgrades/front-end/general/eral.html or at the ftp site: ftp:roadrunner.gov

Important: CDF Doc #2388

J. Grounding Information

Engineering Technical Letter, CDF Doc #3868 (power distribution)

CDF Grounding and Shielding Working Group Report (possible alternate to I below)

K. Cable Grounding

Digital Link Document (being prepared)

L. Electrical Design Guidelines for FNAL Experiments

Research Division, Electronics / Electrical Department, Rev. 2.1, 22 Dec. 1994.

M. FNAL ES&H Manual - Electrical Safety

See: www-esh.fnal.gov go to FESHM

Important: Section 5040

N. Test Stand & Documentation Requirements

1. Test Modules, Cables

2. Test Software

3. Miscellaneous Test Apparatus

Special subracks, backplanes, etc.

4. Power Requirements

O. Other Documents

1. Heat Transfer Study for Flat Cable

3M Heat Transfer Study by Mitchell and Sullwold

Ampacity Tests of 28AWG cable by Drennan, FNAL Doc: TM #1657.

P. Special Tools

1. Press-Fit Connector Tools & Techniques

a)	**Hard Metric Connectors**	**AMP, ERNI, FCI Application Notes**
b)	**DIN Connectors**	**Harting Application Notes**

2. **Gasket Tool** — **Rittal Catalog**
3. **Subrack Covers** — **Rittal Catalog**
4. **Vw, Vx, Vy & Vz Power & Return Bridges** — **Rittal Catalog**
5. **Front-Panel PC Board Attachment Brackets** — **Rittal Catalog**
6. **Dummy Plug-In Units (Air Resistors)** — **From CDF Stock**
7. **Module & Transition Module Stiffeners** — **VIPA, VITA23**

Q. IEEE Mechanical References

1. IEEE 1101.1

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4. VME, VME64 and VME64x Connector Insertion and Extraction Forces

Board Height	Standard	Connector(s)	Total Pins	Insertion Force	Extraction Force
3U	VME/VME64	J1	96	90 N	20 N
6U	VME/VME64	J1/J2	192	180 N	40 N
6U	VME64x	J1/J0/J2	435	395 N	89 N
9U	VME64x-9U	J1/J0/J2/J4/J3	746	650 N	146 N
9U	VME64x-9U	J1/J0/J2/J4/J5/J6	905	780 N	175 N

Table F.4.1
Insertion and Extraction Forces
for
3U, 6U and 9U Boards