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# Analog CMOS peak detect and hold circuits. Part 2. The two-phase offset-free and derandomizing configuration<sup>☆</sup>

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## Abstract

An analog CMOS peak detect and hold (PDH) circuit, which combines high speed and accuracy, rail-to-rail sensing and driving, low power, and buffering is presented. It is based on a configuration that *cancel*s the major error sources of the classical CMOS PDH, including *offset* and common mode gain, by re-using the same amplifier for tracking, peak sensing, and output buffering. By virtue of its high *absolute* accuracy, two or more PDHs can be used in parallel to serve as a data-driven analog memory for derandomization.

The first experimental results on the new peak detector and derandomizer (PDD) circuit, fabricated in 0.35  $\mu\text{m}$  CMOS technology, include a 0.2% *absolute* accuracy for pulses with 500 ns peaking time, 2.7 V linear input range, 3.3 mW power dissipation, 250 mV/s droop rate, and negligible dead time. The use of such a high performance analog PDD can greatly relax the requirements on the digitization in multi-channel systems. © 2002 Elsevier Science B.V. All rights reserved.

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## 1. Introduction

A common problem in scientific instrumentation is to measure charge impulses from a multi-channel detector. The first element of the electronic chain in such a system is a low-noise, charge-sensitive preamplifier, followed by circuit blocks that perform further processing such as

filtering (pulse shaping), peak detection, and determining the time of occurrence. The most flexible method of pulse processing is to digitize the signal directly after the low-noise preamplifier. Once the waveform has been recorded as a series of digital samples of sufficient precision and sampling frequency, the subsequent operations can be performed very efficiently by modern digital signal processing hardware.

For systems with many channels, however, a fully digital signal processing chain can be impractical. Since only the most cost- and power-insensitive applications can allocate an ADC per channel, usually the events of interest are

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multiplexed into a more limited number of ADCs. In order to identify the events to digitize, a trigger of some type is necessary. An auxiliary detector may generate the trigger, or it may be formed from the charge measurement channels themselves. The trigger can be global, in which case it signals only the occurrence of an event somewhere in the detector, or it may identify the occupied channels as well.

In response to the trigger, the system may sample the analog waveform (*track-and-hold* configuration) for later digitization, or activate a multiplexer, which sends the waveform of the occupied channel directly to an ADC.

Triggered systems suffer from two sources of inefficiency and inaccuracy. First, uncertainty in the time of occurrence means that precise peak samples are not always acquired. The timing uncertainty may arise from the method of generating the trigger or from propagation delays throughout the detector. To deal with this time uncertainty, some systems employ multiple sampling of the waveform to capture pre- and post-peak information; the precise timing and peak height are recovered in offline analysis (typically 4–16 samples are recorded per trigger). Second, global triggers require that samples from all channels be recorded, even those that are not occupied. Usually the unoccupied channels are identified and eliminated (sparsified) after digitization.

The ADC resources needed to support a globally triggered, multiply sampled readout system are high. If the channel count is  $N_{\text{ch}}$  and the number of time samples recorded per trigger is  $n_t$ , then the total number of digital samples to be acquired is  $N_{\text{ch}}n_t$  (note that the system can contain many ADCs operating in parallel by means of a suitable multiplexing arrangement). Since most systems cannot simultaneously acquire new data and read out old data, they are blocked or “dead” during readout; the readout must be completed before new data can be acquired. Hence, the digitization must be completed in a time  $t_{\text{block}}$ , the maximum tolerable dead time. This requires the digitization system to work at a rate  $R_{\text{trg}} = N_{\text{ch}}n_t/t_{\text{block}}$  samples/s. The requirements of the digitization system can be greatly relaxed by the

availability of a fast and accurate *peak detect and hold* (PDH) circuit.

With an ideal PDH, the uncertainty in timing is minimized and a precise peak sample is always obtained, so  $n_t = 1$  (an interesting property of PDH circuits is that they provide both the amplitude and the timing information). The PDH automatically sets a flag when it is occupied, making sparsification feasible before digitization. Furthermore, the hold capacitor of the PDH acts as an analog memory; hence two or more PDH circuits can be placed in parallel and operated alternately, providing a derandomizing capability that practically eliminates readout dead time. We refer to this as a *peak detector and derandomizer* (PDD) configuration.

With the PDD, the number of samples per trigger is only  $N_{\text{occ}}$ , where  $N_{\text{occ}}$  is the number of occupied channels, and the sampling can occur at a rate equal to the average event rate  $1/t_{\text{event}}$ . A system implemented with PDDs thus requires an overall digitizing rate  $R_{\text{PDD}} = N_{\text{occ}}/t_{\text{event}}$ . The reduction in required rate compared with a triggered, multiply sampled system is given by

$$\frac{R_{\text{PDD}}}{R_{\text{TRG}}} = \left(\frac{1}{n_t}\right) \left(\frac{N_{\text{occ}}}{N_{\text{ch}}}\right) \left(\frac{t_{\text{BLOCK}}}{t_{\text{EVENT}}}\right) \quad (1)$$

where the first factor comes from the precise peak timing, the second is due to self-sparsification, and the last factor is from the buffering and derandomizing function of the PDD. Overall, the PDD can reduce the digitizing requirement by several orders of magnitude. In the case of a trigger identifying the occupied channel, the second factor in Eq. (1) becomes one ( $N_{\text{ch}} = N_{\text{occ}}$ ), but the PDD can still greatly relax the digitizing requirement due to the two remaining factors. In addition, the peak detector eliminates the need for a trigger. Indeed, the PDH itself can signal the time of occurrence of the peak.

Several analog PDH circuit solutions were proposed during the past years, all based on a feedback loop and a rectifying element, and ranging from the classical diode to the current mode and current conveyor approach [1–5]. Among the integrated circuit realizations, the one originally proposed by Kruiskamp and Leenaerts

[1,6–8] is particularly attractive. The Kruiskamp–Leenaerts circuit, which uses a current mirror as rectifying and loop-stabilizing element, can be considered as the current state-of-the-art. Both this and the other CMOS compatible PDH circuits, while being promising, were not widely adopted in multi-channel CMOS front-ends for higher precision measurements because they suffer from significant limits when high accuracy, speed, and wide dynamic range are required at the same time (analyzed in a companion paper in this issue [9]). These limits can be only partially alleviated by direct solutions such as in-loop buffering and proper MOSFET sizing, as each of these direct solutions introduces further errors.

In this paper, we propose and experimentally demonstrate a new CMOS PDH circuit solution that overcomes these drawbacks. It is based on a two-phase approach that cancels the offset (the major error source) by re-using the peak-sensing amplifier as an output buffer. By employing a fast and stable amplifier with rail-to-rail sensing and driving capability, it provides a substantial improvement in speed, accuracy, and dynamic range over the current state-of-the-art. In addition, we show that it is possible to use multiple PDH circuits in parallel for high-rate operation and derandomization without introducing appreciable error.

The operation and limits of the classical state-of-the-art CMOS PDH were discussed in a related paper [9]. The proposed two-phase CMOS PDH is discussed in Section 2 while the derandomizing configuration (PDD) is discussed in Section 3. Section 4 reports on the experimental results.

## 2. The two-phase CMOS PDH

What we propose is a solution (the *two-phase* CMOS PDH) that overcomes the major limits of the classical CMOS PDH [9]. In particular, the proposed configuration exhibits the following improvements:

- It is *offset-free* (i.e. the accuracy is not affected by the offset  $V_{\text{off}}$  of the amplifier).
- Its accuracy is not affected by common-mode errors of the amplifier.

- The input MOSFETs can be properly sized to minimize the impact of their parasitic capacitances on the accuracy, without regard to mismatch effects.
- A rail-to-rail input and rail-to-rail output operational transconductance amplifier (OTA) is implemented so that it can *accurately process rail-to-rail pulses*.
- The MOSFET  $M_1$  can be properly sized to minimize its impact on the accuracy.
- It is characterized by rail-to-rail *high driving capability*.

In this section, the operation (A), accuracy and stability (B), amplifier and logic realization (C) of the proposed two-phase PDH are discussed.

### 2.1. Two-phase PDH operation

In Fig. 1, a simplified schematic of the two-phase PDH for positive peak detection is shown. In the first phase (WRITE phase, W), switches S3, S4 and S5 are open while S1 and S2 are closed. The OTA supplies current to the current mirror  $M_1$ – $M_2$  so as to charge the hold capacitor,  $C_h$ . In this configuration, the circuit provides tracking, peak detection and hold [9]. In the second phase (READ phase, R) switches S1 and S2 open, breaking the loop and isolating the PDH from any additional input signal. Switch S5 closes, shutting off  $M_1$  to ensure that no currents other than leakage disturb the peak voltage  $V_h$  stored in the hold capacitor  $C_h$ . Switch S3 in closed position turns the OTA into a unity gain buffer, with  $V_h$  as its input signal. Finally, S4 connects the buffered peak sample to the read-out system, represented by the load impedance  $Z_L$ . Once the read-out has been completed, the reset switch S6 closes momentarily to reset  $V_h$  to a chosen baseline  $V_{\text{BL}}$ . The PDH can then be returned to the W state, ready to process the next pulse.

To see how the two-phase configuration leads to offset cancellation, refer Fig. 2a. In the WRITE phase, the amplifier offset  $V_{\text{off}}$  corrupts the peak voltage stored on  $C_h$ . During the second phase (Fig. 2b), the amplifier acts as a follower of the voltage held on  $C_h$ . The offset voltage  $V_{\text{off}}$  is now subtracted from the held peak value, canceling the error.

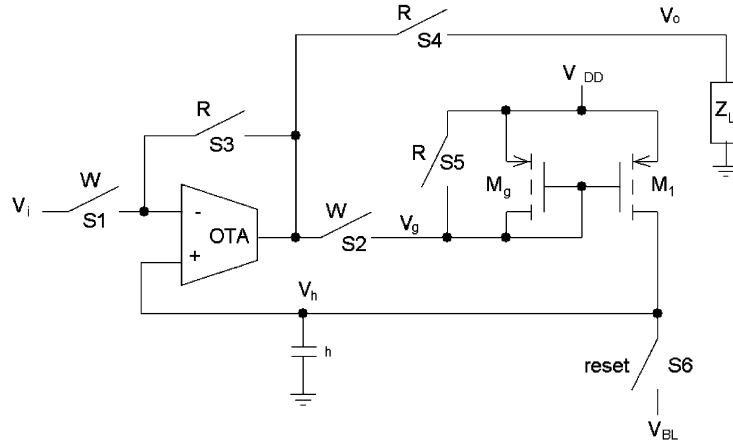


Fig. 1. Simplified schematic of the two-phase PDH.

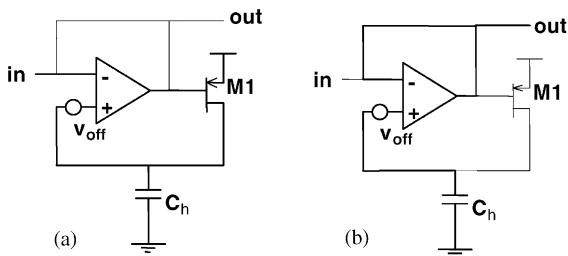


Fig. 2. Simplified schematic of the two-phase peak detector: (a) WRITE phase and (b) READ phase.

We can make the circuit switch automatically from the WRITE state to the READ state by sensing the signal at node  $V_g$  in Fig. 1. When a pulse is being tracked,  $V_g$  falls to a level at least  $|V_T|$  below  $V_{DD}$  to provide current to charge the hold capacitor  $C_h$ . After the peak  $V_g$  makes an upward transition to switch off the current into  $C_h$ , this low-to-high transition can be detected with an appropriate comparator and used to put the circuit into the R state to await read-out. Moreover, the upward  $V_g$  transition serves as an accurate time maker to indicate the time of arrival of the pulse for those systems requiring such an information.

It is important to note that no switch is directly connected to the hold capacitor, other than the reset switch (not active during the sensing and readout of the pulse). The sensitive hold node is thus isolated from switching noise. The only

design criterion to be applied for the switches is related to minimizing the parasitic time constants introduced in the loops.

To acquire the baseline, the reset level  $V_{BL}$  can simply be set to a voltage lower than the input signal baseline. In the W state, the PDH can be easily stabilized as discussed in Section 2.3 of Ref. [9], while in the R state, the stabilization of the unity gain configuration may require the simple addition of a compensation capacitor parallel to  $Z_L$ .

### 2.2. Residual error

Concerning the accuracy, in the W state, the PDH is subject to all the limits discussed in Section 2.2 of Ref. [9], due to  $M_1$  ( $C_{gd}$ ,  $Q_{ch}$ ,  $C_d$ ) and OTA ( $V_{0,cm}$ ,  $A_0$ , CMRR,  $C_c$ ,  $C_i$ , speed).

The rail-to-rail output capability of the OTA, by Eq. (2) of Part 1 allows the use of minimum values for the size of  $M_1$ , thus improving the accuracy. The positive impact on the equations for the stability should also be considered with respect to the configurations in Fig. 13 of Ref. [9] (see also Sections 2.3 and 2.5 of Ref. [9]).

The input stage of the OTA (see Fig. 3) uses two differential pairs in parallel (one NMOS and one PMOS) to achieve rail-to-rail sensing. The two major consequences are an offset  $V_{off}$  (mainly due to the mismatch between the differential couple, and different for the two couples), which depends

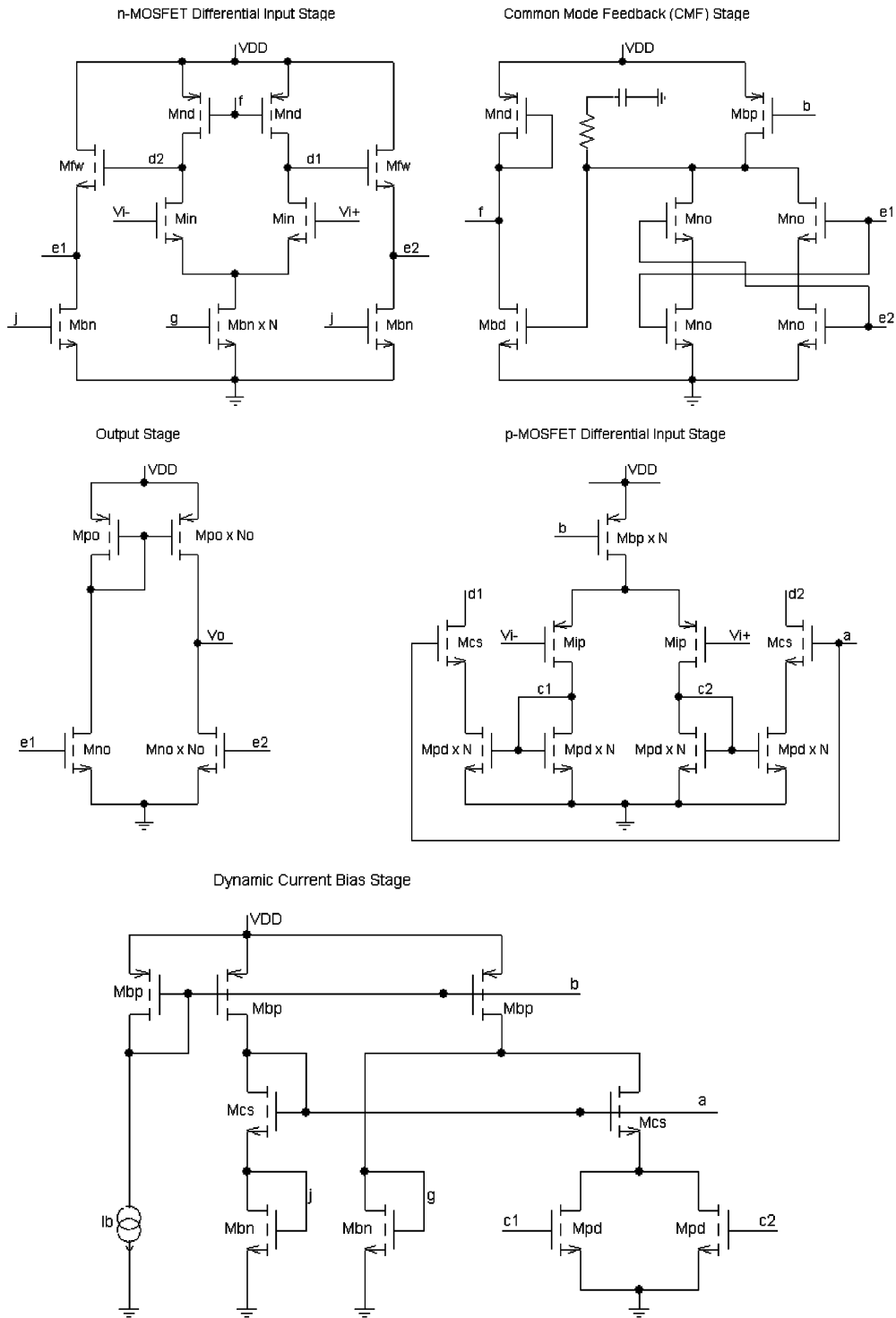


Fig. 3. Schematic of the OTA.

on the input voltage, and higher values for  $C_c$  and  $C_i$ .

On the other hand, the impact of  $V_{off}$  on the accuracy of the two-phase PDH is zero: the error  $V_{e,DC,W} = V_{hp} - V_{ip}$  in the W state is given by [9]

$$V_{e,DC} \approx \frac{V_{GP} - V_{o,CM}}{A_0} + V_{OFF} - \frac{1}{CMRR} \frac{2V_1 - V_{DD}}{2} \quad (2)$$

where  $V_{0,cm}$  is the common mode output reference for  $V_i^+ = V_i^- = V_{DD}/2$ ,  $V_{gp}$  is the gate voltage in proximity of the peak and  $A_0$  is the open-loop DC voltage gain.

The error  $V_{e,DC,R} = V_0 - V_{hp}$  in the R state is easily calculated as

$$\begin{aligned} \langle /sc \rangle \langle sc \rangle V_{e,DC,R} &\approx -\frac{V_{IP} - V_{o,CM}}{A_0} - V_{OFF} \\ \langle /sc \rangle \langle sc \rangle &+ \frac{1}{CMRR} \frac{2V_1 - V_{DD}}{2} \end{aligned} \quad (3)$$

where we assumed that  $A_0$  is negligibly affected by  $Z_L$ . The total error  $V_0 - V_{ip} = V_{e,DC}$  is given by

$$V_0 - V_{IP} = V_{e,DC} \approx \frac{V_{GP} - V_{IP}}{A_0}. \quad (4)$$

The errors introduced by  $V_{off}$ ,  $V_{0,cm}$ , and CMRR are thus *anceled*, while the residual error from Eq. (4) can be minimized by maximizing the DC voltage gain  $A_0$ . This result also indicates that it is now possible to minimize the size of the input MOSFETs of the double differential stage disregarding any mismatch and the consequent offset. In this way, the minimization of  $C_c$  and  $C_i$  is obtained.

Under these conditions, the accuracy of the two-phase PDH is to some extent limited only by  $A_0$  as from Eq. (4), and by the finite speed of the OTA (see Eq. (15) of Ref. [9]).

### 2.3. Rail-to-rail OTA

Of the several schemes of OTA available in the CMOS literature [10–12], none seemed to match this requirement in a reasonable amount (few mW) of dissipated power. We have consequently developed an OTA, which matches the needs of the

PDH. A schematic of the OTA is shown in Fig. 3 where, in order to simplify the concept to the reader, each stage has been separated and linked to the others through labels (a–j excluding h and i).

If current-mirror compensation is adopted, the maximum value of the pole  $\omega_{a,max}$  at the output node of the OTA is achieved when the input slope equals  $V'_{i,max}$ . It can be written (see Appendix C and Eq. (A3) of Ref. [9]) as

$$\frac{1}{\omega_{a,max}} \approx \frac{C_G}{\lambda g_{M,MAX}} < \frac{C_H}{A_{0,MAX} g_{M,MAX}} \approx \frac{V_{DD} - V_T}{V'_{i,MAX} A_{0,MAX}} \quad (5)$$

where  $A_{0,max}$  is the DC voltage gain in the proximity of the peak, i.e. the value to be used in Eq. (2). When fast pulses need to be processed, the condition (5) may become so stringent that the secondary poles of the OTA start to play a role in the stability of the loop. In practical cases, the influence of the secondary poles will force us to choose values for  $W_g$ , relatively larger than the mere equality in (C8) of Ref. [9]. The resulting increase in the value of  $C_g$  has negative impact on the power dissipated by the OTA or on its speed. In order to minimize this impact, an OTA with secondary poles located at a frequency, as high as possible, should be implemented.

The two (n-MOSFET and p-MOSFET) differential stages sum their current at nodes d1 and d2. A DC voltage gain of about 10 is achieved at these nodes, with the time constant located at a very high frequency. The two followers  $M_{fw}$  drive the output stage (slightly simplified in Fig. 3), which provides an additional DC voltage gain of the order of 100 for a total DC voltage gain (i.e.  $A_{0,max}$ ) of the order of 1000. The common-mode feedback (CMF) controls the common mode current of the input stage through  $M_{nd}$ . A lead-lag compensation ( $R_{cmp}$  and  $C_{cmp}$ ) for stabilizing the common-mode loop is also included. A cross-connection at the input disables the CMF whenever one of the two  $M_{no}$  is shut off, thus minimizing its impact on the differential gain. The dynamic current bias stage provides DC biasing of nodes a, b and j and dynamic biasing of node g. When, for large signals, the p-MOSFET differential stage approaches the shut off, a current starts to flow through the n-MOSFET differential

Table 1  
Pspice BSIM3v3.1 simulated performance of the OTA

Parameter	Value
GBW	80 GHz
Output resistance	200 k $\Omega$
DC voltage gain	1.45 k
Dissipated power	$3.3 \text{ V} \times 1 \text{ mA} = 3.3 \text{ mW}$
Max output current	500 $\mu\text{A}$
Output pole	56 MHz
Second pole	960 MHz
Third pole	2.6 GHz

stage. This maintains a relatively constant gain over the whole rail-to-rail swing.

In the version that we implemented in the PDH, the value of the bias current  $I_b$  was set to  $\approx 66 \mu\text{A}$ , while the values chosen for the multiplicity factors  $N$  and  $N_o$  were 4 and 6, respectively. Values of  $W_g = 4$  and  $12 \mu\text{m}$  were chosen for the input n-MOSFETs and the input p-MOSFETs, respectively.

Simulation results of the unloaded OTA using BSIM3v3.1 modeling of MOSFETs and including source and drain parasitic capacitors are shown in Table 1. The stabilization of the unity gain configuration requires a minimum capacitive load at the output node of the order of 1 pF. The DC voltage gain is nearly constant up to  $\approx 500 \text{ mV}$  from the rails, then it starts to decrease. A gain of about 100 at  $\approx 250 \text{ mV}$  from the rails was simulated.

### 3. The peak detector and derandomizer (PDD)

The need to measure the amplitudes of randomly arriving pulses is commonly encountered in nuclear electronics. As discussed in Section 1, a PDH system capable of accurately processing and storing several pulses in parallel can greatly relax the requirements on the following ADC, which now needs to convert only one value for each pulse, and at a rate equal to the average rate of the arriving pulses (time-domain derandomization).

In Section 2, we showed how the two-phase PDH can achieve rail-to-rail *absolute* accuracy,

which is independent of process variations. This opens up the possibility of using several two-phase PDHs in parallel without adding the complexity of a separate and voltage-dependent calibration for each PDH. A further possibility is to construct a two-phase PDH with multiple hold capacitors and suitable switches to store and read out more than one peak. By combining the peak detection and analog storage functions of the PDH with suitable control logic, the PDD can be made to behave like a data-driven analog FIFO. In this section, the PDD, based on the use of several two-phase PDHs operating in parallel, is discussed. The first experimental results from a dual version are reported in Section 4.

In Fig. 4, a simplified schematic of the PDD based on  $N$  copies of the two-phase PDH is shown. The block labeled, *PDD Logic*, keeps track of the next empty PDH and maintains an ordered list of occupied PDH cells awaiting readout.

When a new pulse arrives, it is detected and held on the storage capacitor of the  $n$ th peak detector (PDH- $n$ ). The PDD logic opens the input switch  $S_{in}$ , then selects the  $n + 1$ th PDH available for input and closes the corresponding input switch  $S_{in+1}$ . In the mean time, it stores the address in an  $N$ -deep first-in-first-out memory (readout FIFO). Up to  $N$  pulses can be processed and stored without requiring the readout.

When the ADC is ready to convert a value, the external logic sends a signal,  $V_{read}$ , to the PDD. The PDD logic selects the first PDH address from the readout FIFO and closes the corresponding output switch. Once the conversion is completed, the external logic sends a signal,  $V_{reset}$ , to the PDD, resetting the PDH and making it available for a further input processing.

While one PDH is being read out, another can accept input pulses. By choosing a sufficiently large buffer size  $N$ , we can eliminate nearly all dead time while clocking the ADC at the average event rate.

In a more complex system, channel ID and timing information for every hit can be combined with the PDH address and stored in the readout FIFO. Then the data acquisition system can read amplitude, position, and time for every pulse.

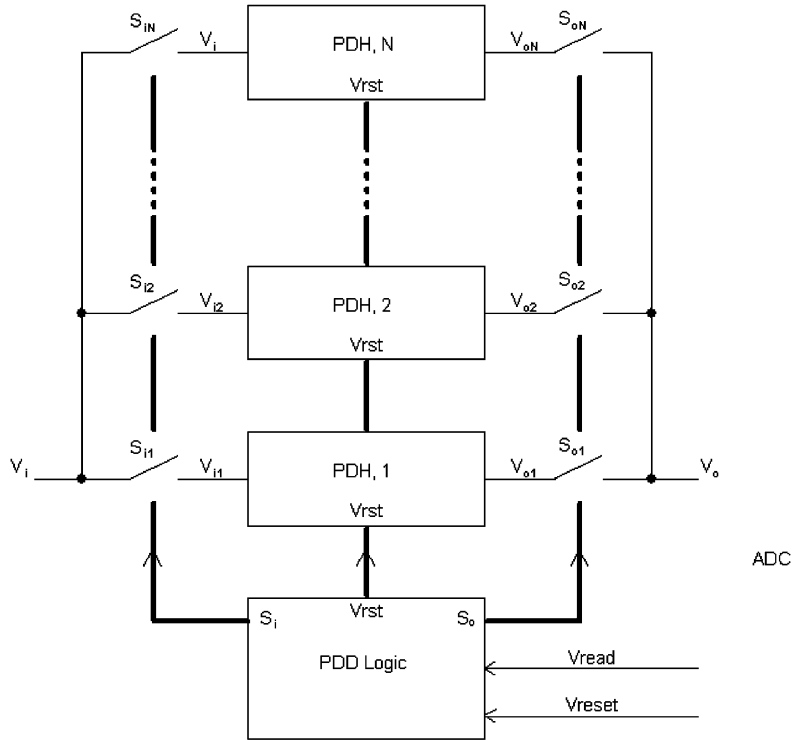


Fig. 4. Simplified schematic of the PDD for storing and derandomizing up to  $N$  samples.

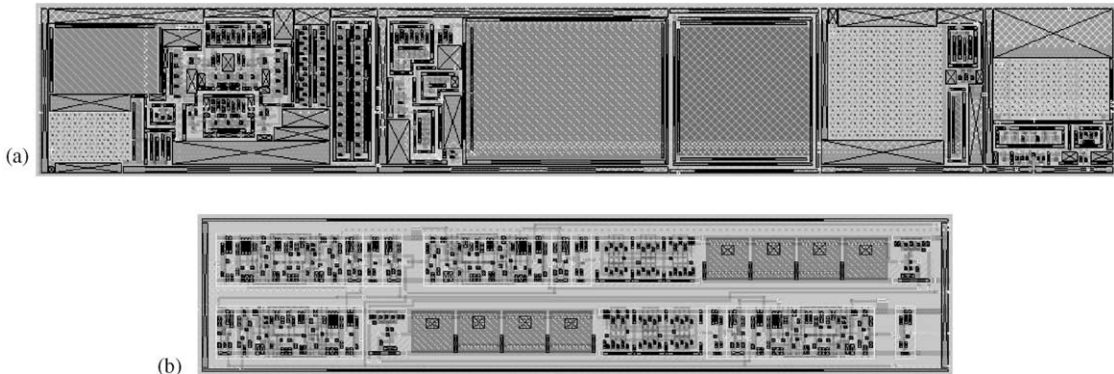


Fig. 5. Layout of the two-phase PDH (a—analogue, b—digital) for a  $0.35\ \mu\text{m}$  CMOS technology.

## 4. Experimental results

In this section, we report on the experimental results on the two-phase PDH (A) and the first experimental results on the PDD.

### 4.1. Experimental results on the PDH

In Fig. 5, the complete layout of the analogue section (a) ( $340 \times 50\ \mu\text{m}^2$ ) and of the digital section (b) ( $245 \times 50\ \mu\text{m}^2$ ) of the PDH are shown. The



0.35  $\mu\text{m}$  CMOS technology from TSMC was used for this realization. Separate grounds and supplies and additional mixed signal-layout techniques were used in order to minimize the digital noise.

In Fig. 6, the measured signals  $V_i$ ,  $V_h$ ,  $V_o$  and  $V_g/V_{DD}$  from two different samples are shown. No averaging was used for these acquisitions. The input signal  $V_i$  (dot-dash) is a semi-Gaussian pulse with peak amplitude  $V_{ip} \approx 600\text{ mV}$  and peaking time  $\tau_p \approx 1.2\ \mu\text{s}$ . The circuit is reset at  $t = 3\ \mu\text{s}$ .

The hold signal  $V_h$  (dash) is read out through a buffer realized by using an OTA identical to the one described in the previous section. The peak amplitude stored at the hold node,  $V_{hp}$ , is strongly

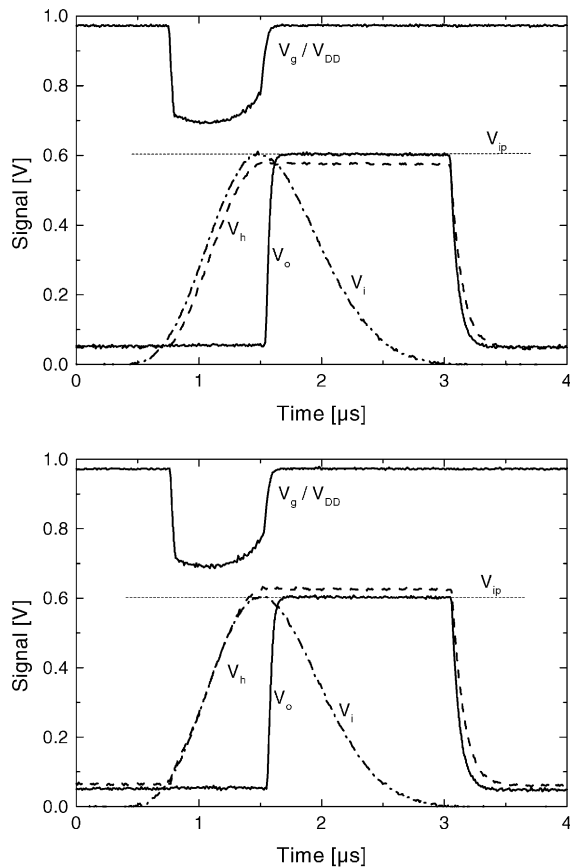


Fig. 6. Measured signals  $V_i$ ,  $V_h$ ,  $V_o$  and  $V_g/V_{DD}$  from identical PDH circuits on two different chips. Note that the two circuits show opposite-sign offset errors at the hold node  $V_h$ , but that these errors are canceled at the output  $V_o$ .

affected by the offset  $V_{off}$  of the OTAs and is strongly different between the two chips. On the other hand, the output signal  $V_o$  (solid) does not seem to be affected by the offset, in agreement with Eq. (4).

As previously discussed, the major consequence of the implementation of a double-differential input stage for the OTA is that the offset  $V_{off}$  becomes voltage-dependent. As an example, in Fig. 7, the DC error normalized to  $V_{DD}$ , measured at the input of the OTA in the buffer configuration as a function of the input voltage for two different samples is shown. From a comparison to PSpice simulations, an offset  $+30\text{ mV}$  for the n-MOSFET and  $-12\text{ mV}$  for the p-MOSFET for case (a) and  $-4\text{ mV}$  for the n-MOSFET and  $-40\text{ mV}$  for the p-MOSFET for case (b) were extracted. Other sources of error are due to the reduction of the gain in proximity of the rail and the CMRR as in Eq. (1).

In Fig. 8, the measured error of the PDH from different chips (solid circles) is shown, for different amplitudes and  $\tau_p \approx 4\ \mu\text{s}$ . The error measured at the hold node through a buffer (open circles) realized by using the OTA is also shown. Even if the measurements were performed on different chips, a 0.2% absolute accuracy was observed for amplitudes 300 mV from the rails, compared to 1.1% in the buffered case. The error showed  $<2.5\text{ mV}$  chip-to-chip variation for the two-phase

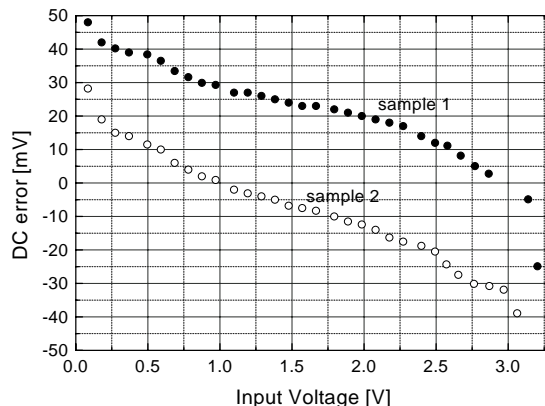


Fig. 7. Measured DC accuracy of the OTA in buffer configuration from two different chips.

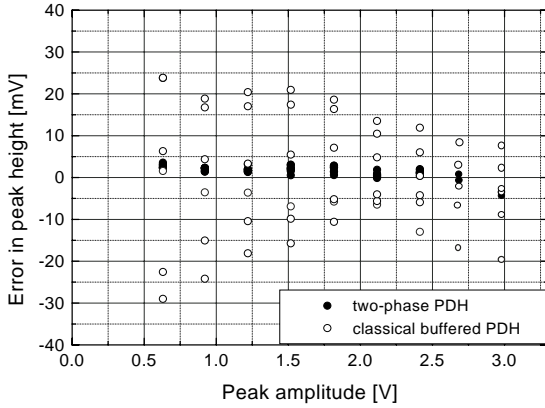


Fig. 8. Measured error of the classical (open circles) and two-phase (solid circles) PDH versus input peak amplitude. For the classical PDH, an on-chip unity-gain follower buffers the peak voltage stored on the hold capacitor. Eight different chips of the two-phase PDH and six of the traditional PDH were measured. Note the dramatic reduction in both the error and dispersion when the two-phase approach is used, due to its offset-canceling property. Semi-Gaussian pulses of 4  $\mu$ s peaking time were used as input.

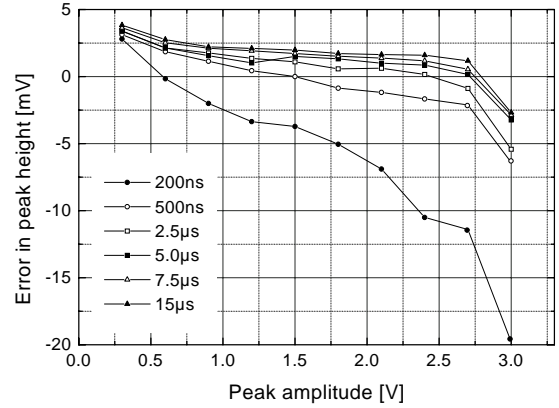


Fig. 9. Measured error of the two-phase PDH, normalized to  $V_{DD}$ , with semi-Gaussian input pulses of different amplitudes and peaking time.

circuit, compared to 53 mV for the single-phase PDH. The dependence of the error on the peak voltage, in agreement with Eq. (4) and with the reduction of the OTA gain in proximity of the rail, can also be observed.

In Fig. 9, the measured error of the PDH for different peaking times  $\tau_p = 200$  ns (solid line), 500 ns, 2.5, 5, 7.5 and 15  $\mu$ s, normalized to  $V_{DD}$ , is shown. Better than 0.2% absolute accuracy can be achieved with this version of PDH for  $\tau_p \approx 500$  ns, while it deteriorates to  $\approx 0.7\%$  for  $\tau_p \approx 200$  ns. This is a consequence of the finite speed of the loop as described in Section 2.2 of Ref. [1] and can be improved by increasing the power dissipated by the OTA for the accurate processing of sub-100 ns pulses.

In Fig. 10, the droop rate of the PDH is shown. The droop, due to the leakage of the reset switch, is of the order of 0.24 V/s. From this value and the value of the hold capacitor  $C_h \approx 2$  pF, a leakage current  $\approx 500$  fA can be inferred.

The dynamic range, intended as the ratio between the maximum and the minimum detectable peak, depends on several factors. Assuming an ideal PDH with infinite absolute accuracy and a

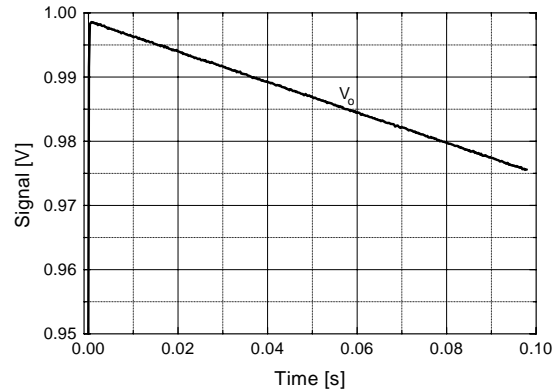


Fig. 10. Measured droop rate of the two-phase PDH.

non-noisy input signal, the minimum detectable peak can be measured by setting the reset level  $V_{BL}$  to a voltage slightly higher than the input signal baseline. The value of  $V_{BL}$  depends on the noise contribution of the OTA to the hold node, which in our configuration is of the order of 80–200  $\mu$ V rms, depending on the value of  $V_g$ . The reset level can be consequently set at 1.2–2 mV above the input-signal baseline (offset from the OTA can be compensated). The discrimination of a small peak above 1.2–2 mV depends on the capability of the comparator to detect the low-to-high transition of  $V_g$ , i.e. on how much  $V_g$  falls during the tracking

phase. In our configuration, falls of  $V_g$  as small as 350 mV can be detected, corresponding to drain currents of  $M_1$ , of the order of 5 nA and peak voltages about 1.6 mV. It follows, in this ideal case, a dynamic range of the order of 65 dB ( $\approx 1700/1$ ). If the finite accuracy of the PDH is taken into account, the dynamic range is limited to 56 dB ( $700/1$ ).

The dynamic range of the PDH in a multi-PDH environment is set by the threshold dispersion (defined by the offset of the OTA) and, without correction, is of the order of 40 dB but can be greatly improved with dedicated fine threshold adjustments.

#### 4.2. First experimental results on the PDD

A version of the PDD with  $N = 2$  was realized in the 0.35  $\mu\text{m}$  CMOS technology from TSMC. In Fig. 11, the measured analog and digital signals for a sequence of two semi-Gaussian input pulses  $V_i$  with peak amplitude  $\approx 360$  mV and  $\approx 2.55$  V, respectively, peaking time 1.2  $\mu\text{s}$ , and delay  $\approx 5$   $\mu\text{s}$  are shown.

In the figure the two *peak-found* pulses generated by the PDD logic in correspondence to each peak, the *read* request and PDH *reset* signals are shown.

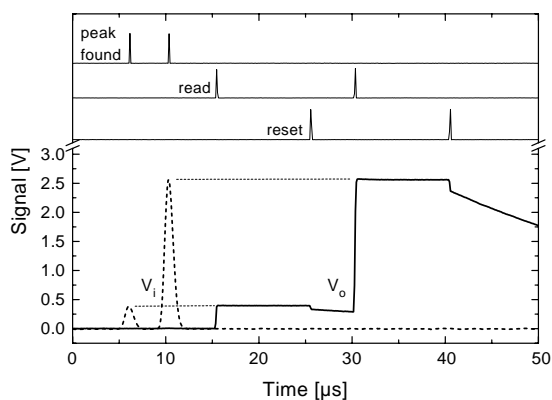


Fig. 11. Measured response of the PDD ( $V_o$ , solid trace) to an input sequence of two semi-Gaussian pulses of different amplitude ( $V_i$ , dashed trace). Digital input and output of the PDD are also shown. After each read request, the PDD presents the next analog sample at the output. Two samples can be stored in the PDD before readout.

generated by the external logic are also shown. For every *read* pulse, the PDD makes available at the output a peak height, following the same order of the input; in correspondence to each *reset* pulse, the PDD resets the last PDH read. The discharge of the output node when all output switches  $S_0$  are open can be observed. The two readings are separated by 15  $\mu\text{s}$ . The dual PDD was tested by using a sequence of two input pulses of different amplitudes separated by 4  $\mu\text{s}$ . In Fig. 11, for example, the pulses are 360 mV and 2.55 V. The logic was designed so that the next PDH available for processing was the last one read. In this way, each amplitude was alternatively stored in each PDH in a *ping-pong* fashion.

We measured the amplitudes of the input peaks and of the outputs for several pairs of amplitudes ranging from  $\approx 380$  mV up to  $\approx 2.9$  V. The measurements were made by using a differential amplifier to subtract the nominal peak amplitude from the signals, followed by an oscilloscope in histogram mode and 2 mV/div vertical resolution. The amplitude histograms are shown in Fig. 12.

From the histograms of amplitudes, we extracted the first- and second-order statistic values in order to evaluate if any line broadening was occurring as a consequence of the ping-pong alternation of the two different PDHs for each amplitude. The results, reported in Fig. 13, show the negligible impact of the use of multiple PDHs on the accuracy of the peak height.

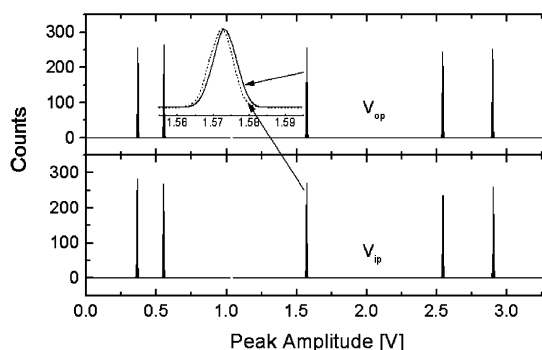


Fig. 12. Measured input and output peak histograms (1k counts) for  $V_{in} = 0.38, 0.57, 1.59, 2.56, \text{ and } 2.92$  V. The insets show a detail for the  $\approx 1.5$  V spectral line.

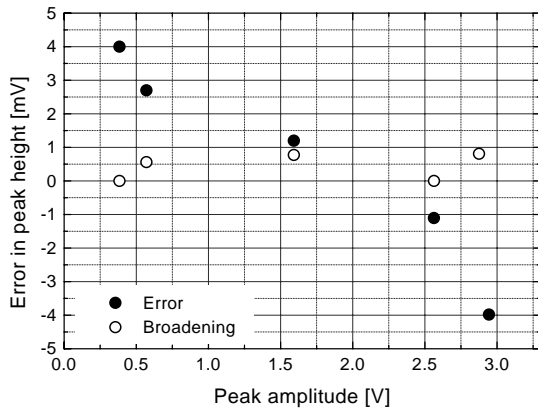


Fig. 13. Difference in mean (absolute error) and standard deviation (broadening, quadratic subtraction) of the peak-amplitude histograms at the input and output of the PDD. The corresponding spectra are shown in Fig. 12.

Table 2  
Performance of the peak detector and derandomizer

Parameter	Value
Technology	0.35 $\mu\text{m}$ DP4m CMOS
Supply voltage	3.3 V
Input voltage range	0.3–3 V
Absolute accuracy	0.2% at 500 ns 0.7% at 200 ns
Droop rate	0.25 V/s
Derandomizing	2 events
Power dissipation	3.3 mW $\times$ 2

## 5. Conclusions

The present work demonstrates that the two-phase peak detect and hold circuit overcomes the major limitations of the classical single-phase approach. By re-using the tracking amplifier as an output follower, offset and CMRR errors are eliminated and the circuit can maintain 0.2% *absolute* accuracy within 300 mV from the rails. Taking advantage of the offset-free operation, we have also developed an analog derandomizer using two peak detectors parallel to a data-driven controller. The first experimental results show that the derandomizer functions properly and introduces negligible error. The performance of the PDD circuit is summarized in Table 2.

The circuit can also provide timing measurements relatively free of amplitude-dependent time walk, since it effectively measures the zero-crossing of the derivative of the input pulse.

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