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Merle Haldeman

This file is located on the Lab PC, at D:\users\haldeman\cdms\Stanford DriverV3.doc

General Operation

The Driver is a module which has 6 independent analog amplifiers, each of which have selectable Gain and Polarity, as well as controllable DC input offset voltage. The Gain choices are 1, 1.43, 2, 5, 10, 14.3, 20 and 50, and the polarity can be inverting or non-inverting for any gain setting. The bandwidth of each channel is approximately 1 MHz wide. Offset is done at the input, and as a result, is unaffected by gain and visa-versa. The input offset is adjustable over a range of -5 to +5 volts, in approximately 2.44 millivolt steps. Each channel is designed to drive a 50 ohm impedance with shunt capacitance of up to 1000 pF.

The output is capable of driving a 50 ohm load with approximately plus or minus 5 volts.

On the Gain = 10 setting, input referred noise is approximately 2nV/$\sqrt{Hz}$, at 1kHz.

Power Control Circuitry

This module utilizes the following voltages available at the backplane:

FE+15, FE-15, +15, -15 and +5D.

When the Driver Module is plugged in with power on, or the power supplies are turned on after the module is plugged in, the on-board circuitry voltages remain off for a period of approximately 1.3 seconds, after which U30, pin 5 goes high, turning MOSFET's U31,U35, U32 and U34 ON, which connects the + & - 15 volt supplies to the rest of the module circuitry. At the same time U30, pin 6 goes low, turning MOSFET U33 on which connects the +5 volt supply to the rest of the module circuitry

Digital Interface

In order to appear as a single gate load to the crate backplane, all of the lines are buffered. The data lines are buffered by U53, whereas the address, read and write lines are buffered by U52. U52 is operated in a unidirectional mode; always passing the backplane signals to this module. The data lines buffer, U53, on the other hand, have the direction controlled by the write line, but only if this particular module is being addressed

The address this module responds to is determined by the address set up by switch S1, and U122. U122 compares the bit pattern of address lines A08, A09, A10 and A12 with that of S1; if they match, the outputs of U53 are enabled(active).

Digital to Analog Converters (DAC's).

These two, 12 bit, quad output devices, allow the user to set the output voltage anywhere in the range of plus or minus five volts, in increments of approximately 2.44 millivolts. Only 6 of the available 8 outputs are used; one for each of the 6 channels on the board. The DAC's provide a DC offset voltage, referenced to "Front End Ground", to the input signal of each of the 6 driver channels. Writing all zeros to any DAC, sets it's respective output to negative five volts. A system reset, (equivalent to writing 800_{HEX}), sets all 8 outputs to zero volts.

Four very precise, and stable, voltages are generated for operating the two, four channel DAC's. These voltages consist of the +10 and -10 volts for powering the DAC's, and the +5 and -5 volts for the high and low references. The reference for generating these voltages is U128, on schematic sheet 3 of 10.

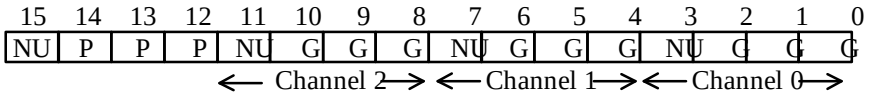
Module Addressing
This module utilizes the following address lines: A12, A10, A09, A08, to select this module, and we call this the "**Module Address**". The Module address is set with a four position DIP switch. Setting a switch to ON, causes the module to respond to a high level, or a logical "1", on that address line at the backplane.

Lines A2, A1, A0 are used to select an item on this module to read from or write to.

Module Address + 0; DAC0;	Reads or writes the DRIVER, Channel **00** OFFSET.
Module Address + 1; DAC1;	Reads or writes the DRIVER, Channel **01** OFFSET
Module Address + 2; **DAC2;**	Reads or writes the DRIVER, Channel **02** OFFSET
Module Address + 3; **CSR0;**	Reads or writes, CSR0
Module Address + 4; **DAC4;**	Reads or writes the DRIVER, Channel **03** OFFSET
Module Address + 5; **DAC5;**	Reads or writes the DRIVER, Channel **04** OFFSET
Module Address + 6; **DAC6;**	Reads or writes the DRIVER, Channel **05** OFFSET
Module Address + 7; **CSR1;**	Reads or writes, CSR1

Control and Status Register (CSR0), Bit assignments

The address of CSR0 is **Module Address + 3**. **CSR0** consists of U45. It is a 16 bit register which can be both, read from and written to, and has the following control functions.



P=Polarity Bit; NU=Not Used; G=Gain Bit; R=Reset Bit

Bit 2	**Bit 1**	**Bit 0**	**Meaning**
0	0	0	Driver Channel 0 Gain = 1
0	0	1	Driver Channel 0, Gain = 1.43
0	1	0	Driver Channel 0, Gain = 2
0	1	1	Driver Channel 0, Gain = 5
1	0	0	Driver Channel 0, Gain = 10
1	0	1	Driver Channel 0, Gain = 14.3
1	1	0	Driver Channel 0, Gain = 20
1	1	1	Driver Channel 0, Gain = 50

Bit 6	**Bit 5**	**Bit 4**	**Meaning**
0	0	0	Driver Channel 1, Gain = 1
0	0	1	Driver Channel 1, Gain = 1.43
0	1	0	Driver Channel 1, Gain =2
0	1	1	Driver Channel 1, Gain = 5
1	0	0	Driver Channel 1, Gain = 10
1	0	1	Driver Channel 1, Gain = 14.3
1	1	0	Driver Channel 1, Gain = 20
1	1	1	Driver Channel 1, Gain = 50

Bit 10	**Bit 9**	**Bit 8**	**Meaning**
0	0	0	Driver Channel 2, Gain = 1
0	0	1	Driver Channel 2, Gain = 1.43
0	1	0	Driver Channel 2, Gain = 2
0	1	1	Driver Channel 2, Gain = 5
1	0	0	Driver Channel 2, Gain = 10
1	0	1	Driver Channel 2, Gain =14.3
1	1	0	Driver Channel 2, Gain = 20
1	1	1	Driver Channel 2, Gain = 50

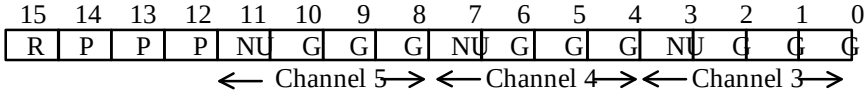
Bit 12 **Channel 0 Polarity; 0=non-invert, 1=invert**
Bit 13 **Channel 1 Polarity; 0=non-invert, 1=invert**
Bit 14 **Channel 2 Polarity; 0=non-invert, 1=invert**

Bits 3, 7, 11 and 15 **unused**

A “0” in the CSR causes the respective relay to be “set” and conversely,
a “1” in the CSR causes the respective relay to be “reset”.

Control and Status Register (CSR1), Bit assignments

The address of CSR1 is **Module Address + 7**. **CSR1** consists of U46. It is a 16 bit register which can be both, read from and written to, and have the following control functions.



P = Polarity Bit; NU = Not Used; G = Gain Bit; R = Reset Bit

Bit 2	Bit 1	Bit 0	Meaning
0	0	0	Driver Channel 3, Gain = 1
0	0	1	Driver Channel 3, Gain = 1.43
0	1	0	Driver Channel 3, Gain = 2
0	1	1	Driver Channel 3, Gain = 5
1	0	0	Driver Channel 3, Gain = 10
1	0	1	Driver Channel 3, Gain = 14.3
1	1	0	Driver Channel 3, Gain = 20
1	1	1	Driver Channel 3, Gain = 50

Bit 6	Bit 5	Bit 4	Meaning
0	0	0	Driver Channel 4, Gain = 1
0	0	1	Driver Channel 4, Gain = 1.43
0	1	0	Driver Channel 4, Gain =2
0	1	1	Driver Channel 4, Gain = 5
1	0	0	Driver Channel 4, Gain = 10
1	0	1	Driver Channel 4, Gain = 14.3
1	1	0	Driver Channel 4, Gain = 20
1	1	1	Driver Channel 4, Gain = 50

Bit 10	Bit 9	Bit 8	Meaning
0	0	0	Driver Channel 5, Gain = 1
0	0	1	Driver Channel 5, Gain = 1.43
0	1	0	Driver Channel 5, Gain = 2
0	1	1	Driver Channel 5, Gain = 5
1	0	0	Driver Channel 5, Gain = 10
1	0	1	Driver Channel 5, Gain =14.3
1	1	0	Driver Channel 5, Gain = 20
1	1	1	Driver Channel 5, Gain = 50

Bit 12 **Channel 3 Polarity; 0=non-invert, 1=invert**
Bit 13 **Channel 4 Polarity; 0=non-invert, 1=invert**
Bit 14 **Channel 5 Polarity; 0=non-invert, 1=invert**

Bits 3, 7, and 11 **unused**

Bit 15 **Module Reset**. Writing a "1" to CSR1, Bit 15, produces a module reset. Module reset, places all channels in the non-inverting gain =1