BTeV Pixel Detector: Data In and Out project

Specification of the low speed optical link receiver chip

The principal function of BteV's Pixel Detector is to acquire and deliver a very high data volume. However, some information must travel in the opposite direction. Clock, Initialization and Control signals must be delivered to the Pixel Detector planes. We can define *the pixel detector slow control and monitoring* as the group of actions which allow us to interact and supervise the pixel detector amplifier chips. These actions can be performed at a slower speed compared to the pixel data readout speed. As well as data is coming into the pixel detector plane some information should go the opposite way in order to supervise the functioning of the pixel chips. This document starts the specification of an optical link receiver chip. The problem of sending data from the Pixel Detector's plane for supervision purposes is not considered here. However, at first sight exist the idea of using the high speed data channels to send this information. The minimization of the number of fiber optic channels is very important for several reasons like space available in the pixel plane, power budget, fault tolerance, and cost. The estimated price for an optical link is $150 and there are about 1000 "optical centers" in the Pixel Detector.

The Pixel chips need a clock to operate. Most of its actions are synchronous with this clock. Even when the FPIX chips can operate at a wide range of clock frequencies, the most likely will be to use the 53 MHz clock provided by the accelerator. This clock may be internally divided by two to operate some sections of the FPIX chip where the speed is not so critical or where a better noise margin is required

Another important component in the Pixel Detector's plane is the fiber optic link Serializer/Transmiter. This chip will need a "very clean" clock, with less than 100ps of jitter. The Serializer/Transmiter is being designed to operate up to 60 MHz, so the 53 MHz clock will be appropriated as well.

The pixel chip needs a BCO clock to provide temporal information to hit occurrence. The BCO clock is 7 times slower than the 53 MHz clock and synchronous with it. Furthermore, the pixel chip needs some control and initialization signals. Most of these signals must be provided from outside the Pixel Detector plane. We can classify them as Initialization, Reset, and Control. All these signals can be run at medium to low speed.

The initialization signals, including the initialization clock, are driven during the initialization of the load and kill pattern and the mask for each pixel cell. The speed of this pattern faces a trade off between the speed of the download and the error rate probability. A clock of few MHz seems appropriate. For details see [Ref]

All control signals, like Reset, Throttle, etc can be operated with a response time of few μs.

In order to minimize power consumption, physical space, and cost, the number of optical links must be as few as possible. Since all the commands are slow they can be serialized onto a single fiber. The BCO clock (~7.5MHz) could, also, be codified in the same fiber channel. Figure 1 shows the proposed fiber optic links for both the receiver and the transmitter ends, and the connection to the Pixel chips. The receiver end considers two channels, one for the "very clean" 53 MHz and a second for the rest of the signals. That is BCO and Initialization clocks plus Initialization and Control signals. However, the pros and cons of codifying BCO/Initialization clock and data in one fiber must be better analyzed. An alternative solution would be to send it though a separate fiber, adding a 3rd link.

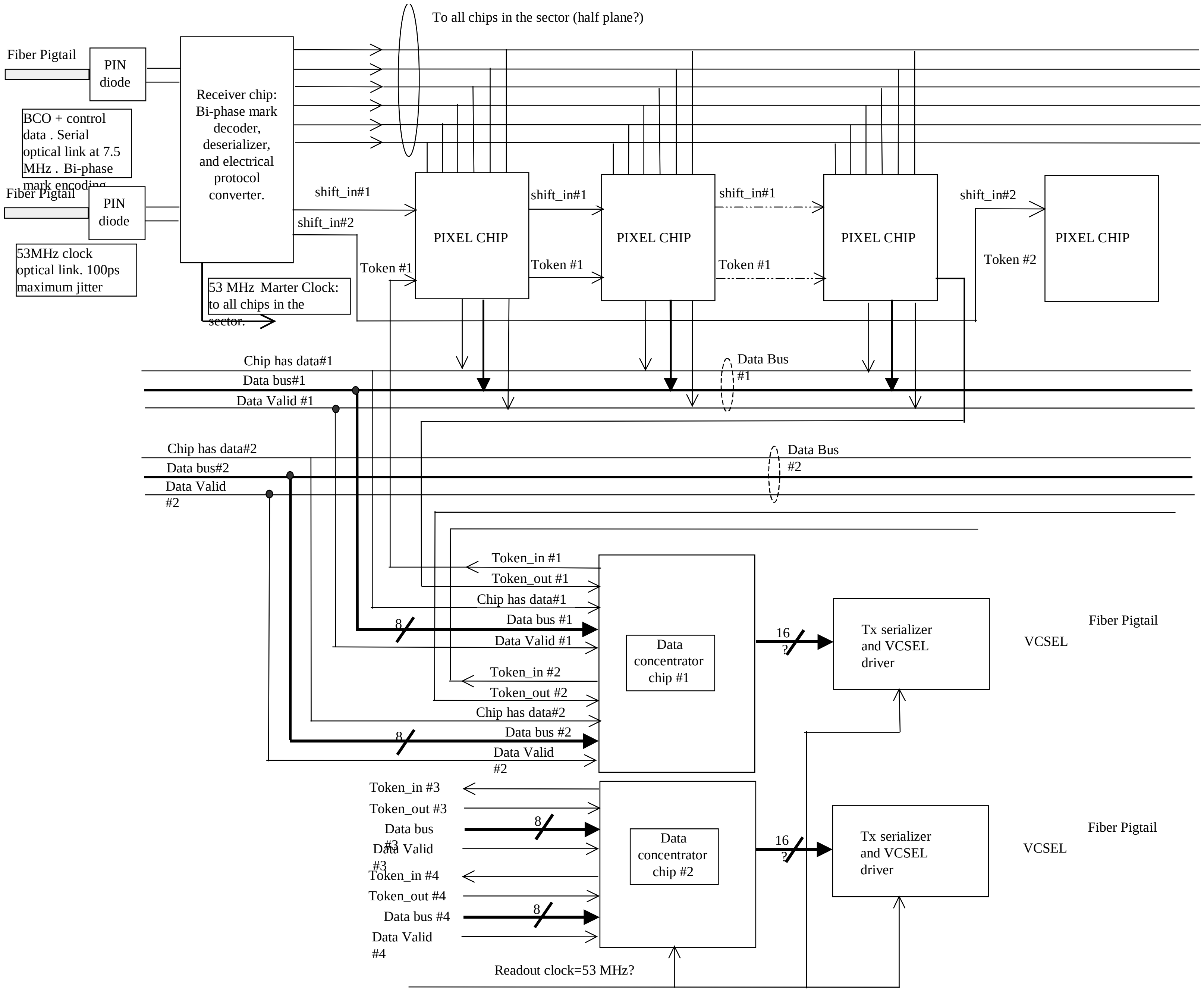
The FPIX Initialization and Control functions are not concurrent. The Initialization functions are the ones used to configure the FPIX for the Analog Input Charge Inject or Detector Charge Inject modes of operation. Several data patterns are stored into the FPIX memory. This memory is laid out as a set of shift registers into the FPIX. The initialization is performed through a serial input, shifting the data with a clock and selecting a specific shift register with some control lines.

The Control functions send a command to the chip while the chip is operating (either in the Analog Input Charge Inject or Detector Charge Inject mode). A control action can stop the acquisition of hits as with Data or Program Resets, throttle the FPIX or request status information without interfering with the FPIX normal operation. A detailed specification of each signal and timing information is provided in the following sections.

The FPIX chip needs three clocks Rdoutck (53MHz), BCOck (7.5MHz) and ShiftCk (in the few MHz range). The Rdoutck and BCOck run concurrently; the ShiftCk runs while the other two are stopped.

The cost of each optical link is estimated between $100 and $200. Each fiber added to the optical system will cost at least $100. If the addition of a fiber is one per half pixel detector plane, the total cost of an additional fiber, multiplying by ~200 half planes is $20K. If the fiber must be added in more than one place in each half plane, the costs will be higher. This is the case if a fiber to be added, such us for BCO clock, must be duplicated to meet electrical constrains (like noise, crosstalk, etc) or physical constrains in a tight layout design (flex circuit).

In order to reduce the number of fibers, several signals can be multiplexed onto the same fiber. A clear case is the one of Rdoutck and BCOck, which are not concurrent. A second case is all the Initialization and Control signals, since they are slow. A more ambitious approach is to send all Initialization, Control and clocks onto the same fiber as shown in Figure 1.



To all chips in the sector (half plane?)
Fiber Pigtail
PIN diode
Receiver chip: Bi-phase mark decoder, deserializer, and electrical protocol converter.
BCO + control data . Serial optical link at 7.5 MHz . Bi-phase mark encoding
Fiber Pigtail
PIN diode
53MHz clock optical link. 100ps maximum jitter
53 MHz Marter Clock: to all chips in the sector.
shift_in#1
shift_in#2
Token #1
PIXEL CHIP
shift_in#1
Token #1
PIXEL CHIP
shift_in#1
Token #1
PIXEL CHIP
shift_in#2
Token #2
PIXEL CHIP
Chip has data#1
Data bus#1
Data Valid #1
Data Bus #1
Chip has data#2
Data bus#2
Data Valid #2
Data Bus #2
Token_in #1
Token_out #1
Chip has data#1
Data bus #1
Data Valid #1
Token_in #2
Token_out #2
Chip has data#2
Data bus #2
Data Valid #2
8
8
Data concentrator chip #1
16 ?
Tx serializer and VCSEL driver
VCSEL
Fiber Pigtail
Token_in #3
Token_out #3
Data bus #3
Data Valid #3
Token_in #4
Token_out #4
Data bus #4
Data Valid #4
8
8
Data concentrator chip #2
16 ?
Tx serializer and VCSEL driver
VCSEL
Fiber Pigtail
Readout clock=53 MHz?

Figure 1

Data and clock onto a single fiber

There are several possible encodings like the Manchester, and the bi-phase mark encodings (Figure 2).

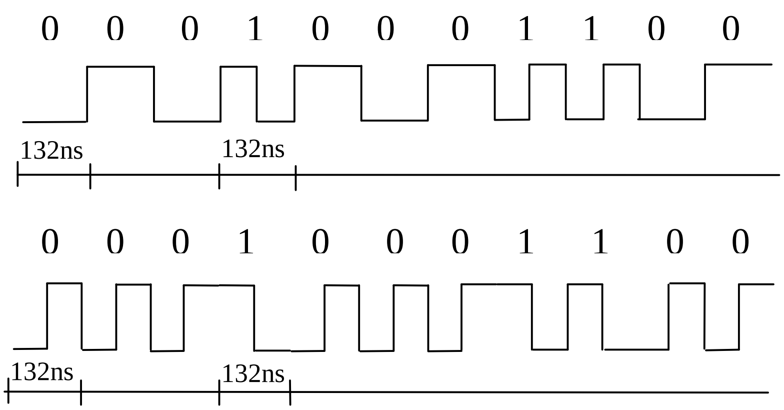


Figure 2a) (upper) Bi-Phase mark encoding 2b (lower) Manchester encoding.

Both encodings have a guarantied transition every clock cycle. The Manchester encoding guaranties a transition at the middle of every cycle but not at the end of a bit. The bi-phase mark encoding guaranties a transition at the end of every bit. The number of transitions is less that in the Manchester encoding.

One of the important requirements is to keep a balance in the DC level of the optical channel. The problem is that at the receiver end, there must be a comparator after the photodiode amplifier. A comparator has 2 inputs, at what voltage do you put the non-fiber one? Usually, the fiber is AC coupled, so the other input can be grounded, but this only works (at high speed) if the optical input is DC balanced. Different protocols all try to keep the same number on ones and zeros to keep an overall DC line balance. With Manchester encoding, you have edges twice as fast, so it is not preferred at high speed.

Another reason is to maximize the power the VCSELs can handle. The maximum DC current for the Mitel 469 is 10mA while is 20mA in pulsed mode Both the BPM and the Manchester encoding accomplish DC level balance requirement. The Receiver chip must separate the clock from the control data signal.

Both the Manchester or Bi-phase encodings are self clocking into the receiver. An alternative solution to simplify the Oprtical Receiver circuit is to use the 53MHz clock to clock the BCOck and data. In this case we will not be using the self clocking property of the Bi-phase encoding but we still use a single DC-balanced channel (Figure 3).

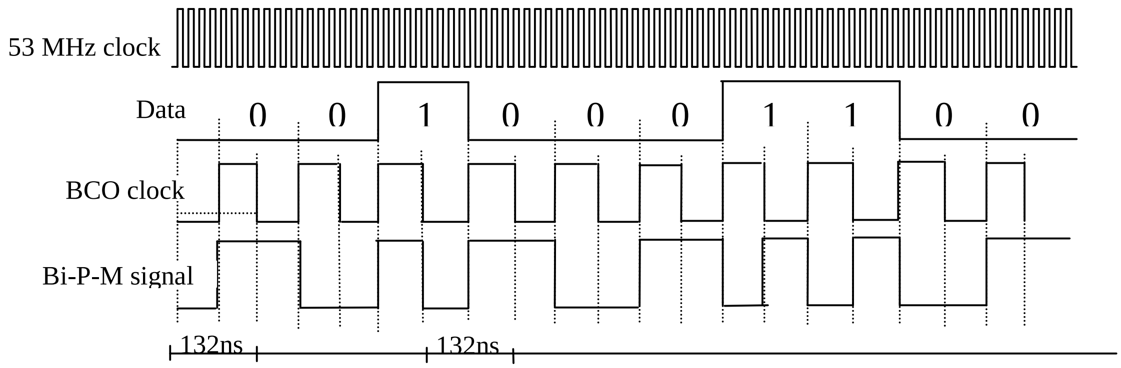


Figure 3

Data Frame:

The data can be framed as shown in Figure 4. It has 5 different fields: Synchronization Pattern, Beginning of Frame (BOF), Command, Data and End of Frame (EOF). The Sync. Pattern is used to mark the beginning of a frame after the channel has been idle for some time. Its purpose is to reset the electronics of the receiver and to disable all action until the next command is available. The BOF signals the beginning of a new control or data frame. It causes the receiver to be synchronized within a byte boundary. The Command field will perform an internal action, setting FFs or generating timing conditions needed to interface with the Pixel chips or Data Concentrator chips. The only frames, which add a Data field to the Command field, are the Initialization frames. The data is loaded into the Pixel chips in series. In case more than one chip is daisy chained together, the initialization sees the chain of chips as a single chip. Finally, The EOF field signals the end of frame, providing frame synchronization to start the next frame or to go to silent mode.

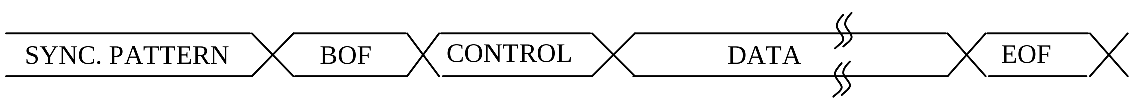


Figure 4.

The transmitter must send a synchronization pattern of at least 2 bytes of 0’s, after which the receiver must guarantee to be ready to accept a command frame. When the receiver is synchronized, it will be waiting for the first 1 to signal the beginning of a frame. This means that BOF must start with 1. It is convenient that CONTROL and the EOF fields start with 1 as well to differentiate “control” fields from the DATA field. For instance

Sync. Pattern	000 0000 0000
BOE	111 XXXX XXXX
Command	101 CCCC CCCC
Data	001 DDDD DDDD
EOE	110 XXX XXXX

Table 1

The 8 bit Command field allows 256 different commands.

Commands:

The Receiver chip will decode control information for the Pixel Detector Amplifiers and for the Data Concentrator chip. The Receiver chip is the only interface between the DAQ-Trigger control and the Pixel Detector. Most of the control lines are semi-static, that is, they can be set with one command and reset with a another command. This information will be stored into FFs into the Receiver chip. Each FF will represent a particular mode set in the Receiver. Not all the command modes will produce an output signal to the Pixel or Data Concentrator chips, some of them will be used to enable internal conditions, which will allow other signals to be delivered to the Pixel or Data Concentrator chips.

Initialization:
The Pixel chip Initialization is the most complex digital function to be implemented in the Raceiver chip because it involves the decoding of a control command, the bypass of an incoming data steam into the ShiftIn input of the Pixel chips and the generation of the proper timing signals. The function to be implemented by each signal related to the initialization of the Pixel chips is as follows:

ShiftIn: This is the data input signal. ShiftIn is the input to a long shift register which programs internal conditions of the Pixel chips, such us the charge inject enable, the kill inject enable and a mask for every single pixel cell. Every Pixel chip has, also, a ShiftOut output, which allows the chips to be daisy chained making an even longer shift register. The Receiver chip must provide a data input stream of the length of the total shift register to be programmed. The ShiftIn signal must be qualified with other complementary signals and clocked into the Pixel chips with ShiftCk. The SiftIn and ShiftOut signals are single ended CMOS.
NOTE: Ideally the ShiftIn data is a continuos stream of equally length bits, however the serial frame structure may need to break up this data stream to allow for frame boundary fields like BOR, EOR, StartBit, etc.

ShiftCk: This signal clocks ShiftIn data into the Pixel Chip's shift registers. The number of clock cycles must be exactly equal to the number of FFs to be programmed. This is usually accomplished by having a free running clock and enabling the data input with other control signals (Load/Kill and Reg<0:2>). Special care must be taken with this implementation due to the fact that the commands are sent sequentially over a serial line and with a frame format. The ShiftCk signal is a CMOS input to the Pixelchips.

Load/Kill: Enables the data path to either the Load or the Kill shift registers. The Load shift register provides a pattern, which enable (disable) each individual Pixel cell to receive an input during the Test Mode through the Analog Input. The Kill pattern disables noisy pixels.

Reg(0:2): Selects a data path (also called scan path) into the Pixel chips for the ShiftIn data. Reg(0:2)=0 disables the input (disables ShiftIn and ShiftCk?). These are CMOS inputs.

The scan paths are as follows:

	Bit Pattern	Path	Data to be loaded/chip (bits)
0	000	Idle – no path	N/A
1	001	Trigger path	6 (used during runtime in trigger mode only)
2	010	Not used	N/A
3	011	Mask registers	102
4	100	Not used	N/A
5	101	Mode, ChipID and Lag	11
6	110	Kill or Inject	5760
7	111	Kill or Inject	5760 (use either path 6 or 7)

Table 2

The number of data bits to be loaded into a FPIX varies depending on the scan path. This number is shown in Table I.

Reset:
There are two resets: Program Reset and Data Reset.

Data Reset: When high (3.3 volts), the BCO counters are reset to zero; the End-of-column registers are reset to Empty; the chip stops Talking. This is a CMOS level signal.

ProgramReset: When high (3.3 volts), the mask registers are reset to zero (no masking); the chip is reset to continuous mode (Non-triggered); the BCO lag is set to 2; the ChipID is set to zero. This is a CMOS level signal.

The 53 MHz clock

Peter Denes' CHFET serializer chip needs a very accurate, jitter-free clock. Peter suggested 100 ps of maximum jitter. However, this is not a definite number since he has not done any simulation on the ability of the CHFET chip to reject jitter in the clock. The problem of jitter is as follows. The period of a 53 MHz clock is about 19ns. The CHFET chip serializes 20 bits in this period. The time each bit is stable in the output is less than 1ns. As a consequence, is logical that a low jitter output data is needed. The CHFET chip has a DLL (Delay Lock Loop). The output of the DLL's phase detector is integrated by a charge pump amplifier, which, basically, is a first-order low pass filter.

The DLL simulations show that, effectively, most of the high frequency input jitter is also present at the output.

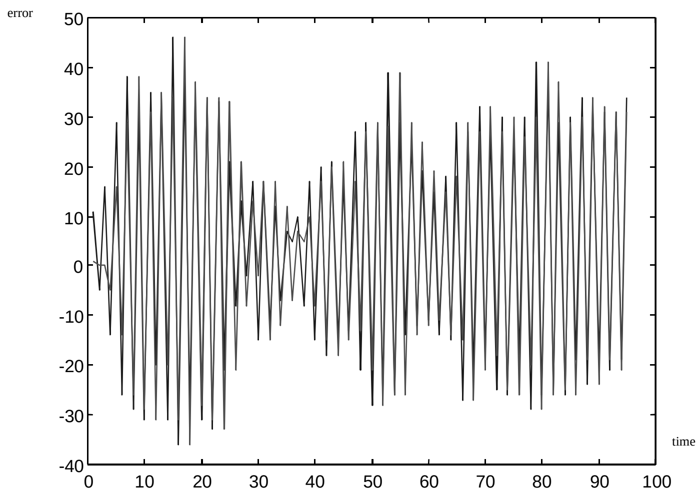


Figure 5

Optical Receiver chip block diagram

Figure 6 shows a block diagram for the deserializer and command decoder of the Optical Receiver chip. The serial data is shifted into the serial to parallel circuit. The first 3 bits indicate whether the word is a Sync, BOF, Control, Data or EOF word. If it is a Control word, the last 8 bits are decoded by the Command Decoder circuit. The commands individually set and reset a FF as shown, (figure) synchronized by the 53 MHz clock. The FFs can be, also, reset by a command reset.

The FPIX initialization requires downloading data into the FPIX chips. The data can be provided at the transmiter side as a byte oriented file. The transmiter will append the 3 bit header (001). The Optical Receiver must remove the header. This can be easily done by stretching the clock. Figure 7a shows that no Shiftck is sent while the 3 bit header is in the ShiftIn output.

The Optical Receiver chip must have as many ShiftIn outputs as initialization chains will be in the Pixel Detector area under its control Figure 6.

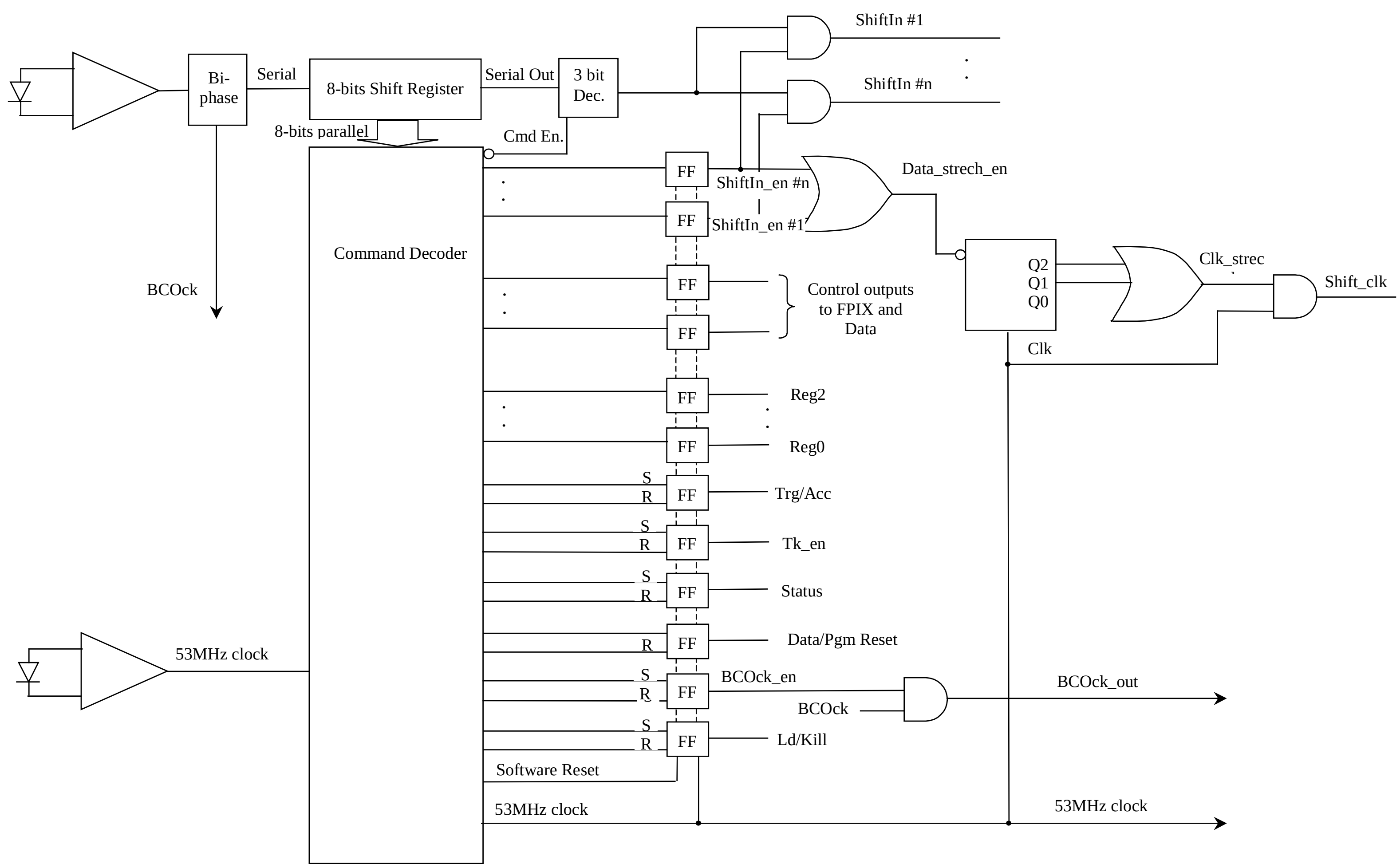

ShiftIn #1
ShiftIn #n
Bi-phase
Serial
8-bits Shift Register
Serial Out
3 bit Dec.
8-bits parallel
Cmd En.
FF
ShiftIn_en #n
ShiftIn_en #1
Data_strech_en
Command Decoder
BCOck
Control outputs to FPIX and Data
Q2
Q1
Q0
Clk_strec
Shift_clk
Clk
Reg2
Reg0
S
R
Trg/Acc
Tk_en
Status
Data/Pgm Reset
53MHz clock
BCOck_en
BCOck
BCOck_out
Ld/Kill
Software Reset
53MHz clock
53MHz clock

Figure 6

The Initialization procedure is as follows:

i) The Optical Receiver electronics is reset (or disabled) by a stream of 0’s.

ii) The Command Decoder decodes a ShiftIn_en command and sets the corresponding FFs.

iii) ShiftInx_en is enabled to output the Serial Output Data. This is the same Serial Input data delayed by the 8 steps of the Shift Register.

iv) ShiftInx_en also enables the Streach Clock counter. The Streach Clock function is to skip the first 3 bits if every data word. The first two bits do not contain data but a fixed 001 pattern as shown in Table 1.

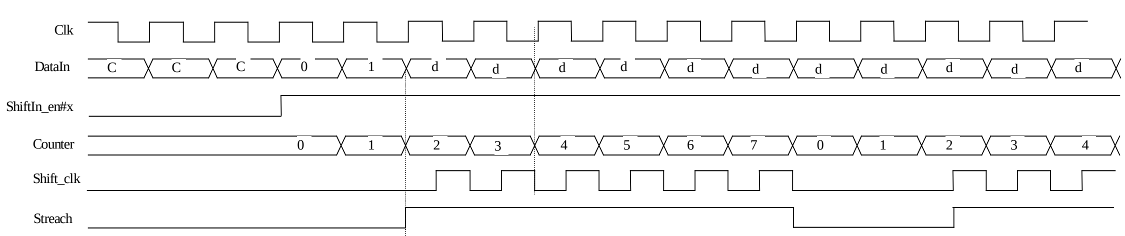
The length of the data field depends on the scan path being initialized and the number of chips daisy chained. The length of each scan path is shown in Table 2, and must be multiplied by the number of daisy chained chips. There are two ways of designing the data field (while keeping it simple), adding a counter with the byte count in the data field or adding a fixed pattern at the beginning of each data word to differentiate it from other frame fields. The first one is less redundant but complicates the electronics of the receiver. It makes the need of a counter, which for this particular case would be a 16-bit counter. Since Initialization time is not an issue here, the proposed approach is the latest.

In order to differentiate the 5 different frame fields, a fixed field pattern has been established. These patterns use the first bits of the word. As shown in Table 1, those are:
BOF: 111
Command: 101
Data: 001
EOF: 110

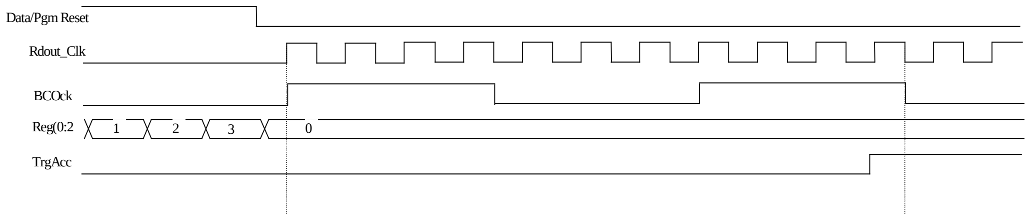
Timing:

Figure 7 a) ,b) and c) show FPIX1 timing signals. Each figure show wich lines must be active during a particular FPIX action.

Initialization



Normal Operation



Reset

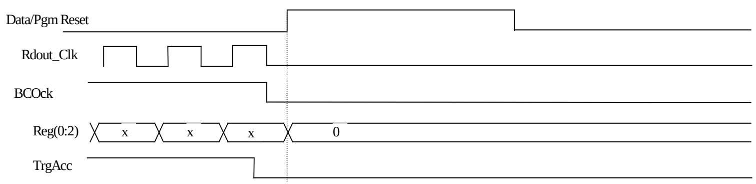


Figure 8

Command List:

	Command	Value
1	Data Reset	
2	Data Reset (reserved)	
3	Program Reset	
4	Program Reset (reserved)	
5	BCO_ck_en	
6	BCO_ck_dis	
7	ShiftIn_en#1	
8	ShiftIn_en#2	
9	ShiftIn_en#3	
10	ShiftIn_en#4	
11	ShiftIn_dis#1	
12	ShiftIn_dis#2	
13	ShiftIn_dis#3	
14	ShiftIn_dis#4	
15	Load/Kill_set	
16	Load/Kill_reset	
17	Set_ScanPath#0	
18	Set_ScanPath#1	
19	Set_ScanPath#2	
20	Set_ScanPath#3	

21	Set_ScanPath#4	
22	Set_ScanPath#5	
23	Set_ScanPath#6	
24	Set_ScanPath#7	
25	Trigg/Acc_high	
26	Trigg/Acc_low	
27	Token_eneble	
28	Report_Status	
29	Receiver reset	

Table 3

The BCO clock:

The BCO clock is provided by the accelerator along with the 53 MHz clock. The BCO clock frequency is about 7.57 MHz and is synchronized to the 53 MHz. In order to reduce the number of fibers, the BCO clock can be codified together with the serial data as shown in Figure 2. The Optical receiver BCO clock output to the FPIX chips must be enabled only during Acquire Mode operation of the Pixel Detector chips. The command BCOck_en will enable the BCOck input onto the output of the Optical Receiver and the command BCOck_dis will disable it.

Chip Requirements

Signal Level Requirements:

Input signals:

The input is connected to the PIN diode. The optical power dynamic range of the PIN diode is large (50µW to 1mW). The responsivity of the PIN is at least 0.3 A/W, providing an input current in the range of 15µA and 0.3mA. This values must be framed to what the receiver chip needs before and after radiation in order to keep a low BER.

Output signals:

The output of the receiver chip will interface directly with the FPIX chips. Even when future versions of FPIX may modify the electrical specification of some outputs, they will be as in FPIX1. The exact electrical voltage end current specifications of signals may also change for the final rad-hard version of the FPIX chip.

Noise requirements:

The total noise in the optical channel, including the transmitter end receiver chip must be low enough to guarantee a certain BER to be determined (say 10exp(-12)) at the end of its life, that is after 2 or 3 years of irradiation. Since parallel optical links will be placed in the same enclosure, a small custom package, the crosstalk will be a component of the total noise and contribute to the total BER.

Radiation hardness:

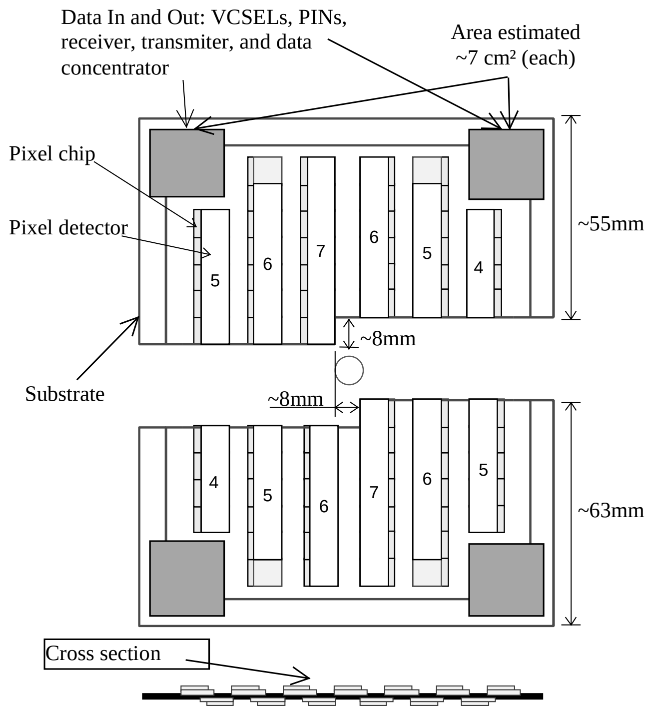
The amount of radiation expected for the area in the Pixel Detector planes where the Data In and Out components will be located has not been precisely estimated. However, 10exp(13) n/cm^2 plus 1 Mrad is a crude estimation of an upper bound. See physical requirements for more information.

Physical requirements:

The physical location of the Data In and Out circuitry has been planed following mechanical and cooling specifications as shown in Figure 4. The approximated area left for the Data In and Out circuitry is less than 7 cm^2. It will be very difficult to fit it all in this tiny space. A more realistic calculation must be made following the minimum sizes needed for this circuitry.

Some possible expansions to the drawing in Figure 4 may consider the extension of the Data In and Out area as shown in Figure 9. Of course, the mechanical and cooling designer must approve the idea (I had, already, mentioned it to Bob Downing, he didn’t say yes but he did not yield to me either). The “little ear” concept is based on the idea that the cooling pipes on the corner will not have a big impact on the Pixel chip because they too far away. Also, the power budget estimated for the Data In and Out can go down dramatically if we can use the Transmiter/Serializer being designed by P.Denes (CMS), which disipates about 100mW.

There is, also, a possibility of having cooling pipes inside the Pixel Detector plane substrate. If this becomes a reality, the space for the Data In and Out will not be a big issue.



Two halves of the pixel plane, West side

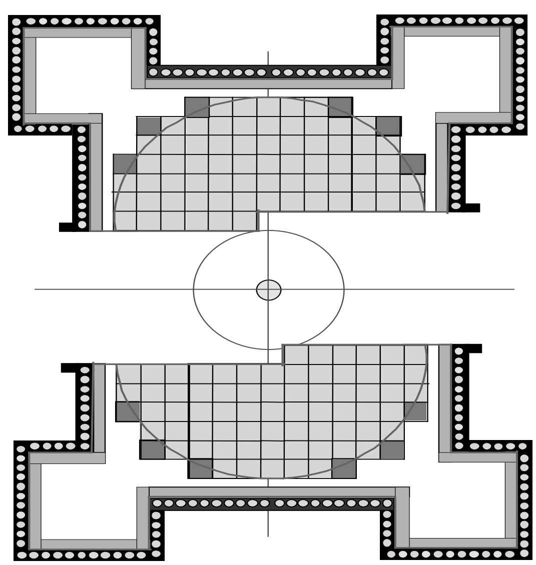


Figure 9

Temperature requirements:
???

Vacuum requirements:

As all Pixel Detector, the Data In and Out components must operate in the vacuum. They should not degrade by outgassing into the vacuum. They should not spoil the vacuum either. However, a small outgassing may be tolerated, but it will make more sophisticated and expensive the vacuum equipment needed to comply with the accelerator requirements.