3 Central Fiber Tracker Stereo Front End Electronics

The Central Fiber Tracker Stereo Front End Electronics, CFTS FE, and Trigger system includes all of the Central Fiber Tracker Stereo channels. Some of the main features of the system are as follows.

The CFTS System

1 Includes Central Fiber Tracker stereo channels.

L3 Readout

1 The analog signal from 512 channels is digitized in an SVX and readout for L3.
2 SIFT chips and MCM's are used because of the shorter integration time of the SIFT chips.
3 The discriminator outputs from the SIFT chips are put into a VSVX for inclusion in the L3 data stream.

CFTS Trigger System

1 Provides no information to the L1 or L2. But digital outputs of the SIFT chips are on the board and pipelined for the VSVX allowing for a future upgrade which sends the bits to the L2 as well.
2 Since the CFTS is not cabled into sectors, as is the CFT, tracks cannot be formed locally.
3 Sending fiber bits from the FE would require 512 bits per FE, and take 640ns per FE. For 75 FE's over 8 cables the transfer from the concentrator would take 6us.
4 The CFTSpp would have to sort and form tracks over 4.8 kbytes of data.

For the L1 CFTS Trigger

1 No L1 Trigger capabilities.

For the L2 CFT preprocessor

1 No L2 Trigger capabilities.
2 May be feasible at a later time to add links over which raw bits are sent to a preprocessor.

A block diagram of the components of the system is shown in Figure 1. There are two sets of front-end electronics boards, FE, in several crates located above the VLPX cryostat in the detector platform. These boards receive the analog signals from the VLPC's and process them for the L3 readout, shown as the Sequencer and VRB crates. In the center of figure 1 is the Concentrator system would only be present for stage 3. This receives the L1 and L2 information from each of the FE boards, concentrates it and sends it on to the L1 and the L2 triggers.

The location of the VLPC cassettes for the CFTS system is shown in Figure 2. The CFTS FE boards are located in five crates in the north cryostat on the platform.

3.1 CFTS FE Electronics

The CFTS FE electronics provides the L3 readout.

3.1.1 Functional Description

During L1 live running the operation of the system can be separated into four….

3.1.2 System Architecture

3.1.2.1 Geometry and Definitions

The mechanical properties of the CFTS system are:

1. There are 75 CFTS FE boards located in 38 cassettes and 5 crates. The 5 extra cassettes in the 5^{th} crate are spares, and the 1/2 cassette in the 38^{th} cassette is a spare.
3. The CFTS FE forms one GS which it does not share with any other system.

Electronic properties are **<u>defined</u>** as:

1. Each CFTS FE board receives 512 the signals from 512 fibers.
2. Half of these, 256, are from a single fiber ribbon at the detector, and the second half are from a second ribbon.
3. The two ribbons can be from anywhere on the detector.

3.1.2.2 Hardware Inventory

<u>The CFTS FE System has;</u>

1	GS with SCL
1	VRB Crate
1/2	Sequencer Crate
5	CFTS Front End Crates, 8-cassette crates
75	CFTS FE Boards, 38 RHB & 37 LHB

<u>Each VRB crates has;</u>

1	VRB Controller board with SCL receiver
10	VRB Boards
10	VEPA Boards
40	Optical link receivers (from Seq)

<u>Each ½ Sequencer crates has;</u>

½	Sequencer Controller Board with SCL receiver

10 Sequencer boards
40 Optical link transmitters (to VRB), 4 per board
40 50-Conductor Cables, 4 per board

Each CFTS FE crate has;
8 Right Hand CFTS FE Trigger Boards
8 Left Hand CFTS FE Trigger Boards
8 BP Connectors for 50-Conductor Sequencer Cables
1 BP Connectors for Cryo I/O

Each FE board has;
1 1553 Node to receive down load
1 SVX Strings
1/2 Interface for 50-Conductor Cable from Sequencer
1 Analog and Serial Clock generator
8 MCM, each with 1 SVX and 4 SIFT chips

3.1.2.3 Hardware description

Figure 1 shows the overall data flow of the system. It could also be considered a crate level diagram of the system since each box corresponds to one or more crates.

3.1.2.3.1 FE Boards

3.1.2.3.1.1 Analog Design

Each FE board receives the VLPC output from two full width ribbons of the CFT. Each of these ribbons has 256 fibers. Figure 9 shows the routing of the signals on the FE board. On the right hand side of the drawing are depicted the 8 MCM's that receive the analog signals.

3.1.2.3.1.2 Charge Pileup

The preamplifier in the SVX chip is not reset every crossing since it needs a

3.1.2.3.1.3 L3 Readout

The SVX2e chips in the 8 MCMs are connected together into a single string of 8. See figure 13. The two strings are read out by one channel of a sequencer board. The L3 readout for these SVX chips is identical as for those in the silicon detector. Please see reference [xxx] for more details on the Silicon L3 readout system. For the CFTS the Sequencer and VRB are in their own crates and form a single and independent geographic sector, GS.