Technote 344
External FERA Control System for the E787 DAQ system

Stephen Adler

January 27, 1998

Abstract

A description of the FERA control system for the E787 DAQ system is given herein.

Due to the complicated external control system used to operate the FERA, this technote is dedicated to its documentation.

The FERA system is made up of 7 CAMAC crates loaded with 4300 FERA modules and 4301 FERA driver modules. 6 of the crates have a single 4301 driver module while the 7th contains two 4301 driver modules. One to control the 4300 modules in its crate and the other servers as the Master control module for several purposes. Among them are to collect and re-drive the data coming off the FERA data bus, to distribute the clear signal coming from the trigger to the other 7 4301 modules and to handle the Data Ready/Data Acknowledge handshake. On the receiving end of the FERA data bus is a fastbus module called a STR370, A Struck Quad DSP96002 FB Slave Module, which has a FIFO where the data is placed after each l0 gate is sent to the FERA system. For the rest of this discussion, please refer to figure 1.

The sequence of events involved with gating and reading out the FERA data is as follows.

1. A clear signal is sent to the master FERA driver which effectively clears the whole FERA system.

2. A gate signal is sent to each 4301 in each create which activates the FERAs such that they integrate their input currents, convert the integrated charge into an equivalent number through an ADC conversion process.

3. Each FERA, when done converting issues a readout request signal which is collected by the master FERA driver. Once all FERAs are ready to be read out the readout sequence begins.

4. The readout sequence is started by the master FERA driver raising the readout enable (REO) signal. This is a differential ECL signal which goes to the REN input of the first 4300 FERA module. This module dumps is data on the FERA bus modulated by a hand shaking signal between the 4300 and the master 4301 driver. As the FERA modules puts its data on the bus, part of this handshaking mechanism is done by the FERA issuing a write strobe signal. These write strobe signals are collected by each FERA master.

5. When the first FERA 4300 module is done writing its data onto the FERA data bus, a PASS signal is raised which is tied to the next FERA modules REN input. This starts the

writing of data onto the FERA bus as done by its predecessor. This sequence is continued until all the FERAs write out there data.

6. As the data from the FERAs is being written to the FERA data bus, a signal call the RQO is De-asserted by the master FERA driver, such that when the readout is finished, it gets asserted. This signal is fed into a discriminator which fires a NIM pulse every time the RQO gets asserted. In other words, an RQO NIM pulse is generated when the last FERA finished writing its data onto the FERA bus. This RQO pulse is used to trigger the STR370. More on this later.

In short, the basic sequence of events is that a clear is sent to the FERA system. Shortly after a gate is received by each FERA driver which causes the FERA modules to start their conversion and end by dumping the data onto the FERA bus, thus for every gate, data will be dumped onto the FERA bus. A subsequent clear signal from the trigger, while the FERA data is being written onto the bus will halt the data writing and put all the FERAs back into an idle state, waiting for the next gate. On the other end of the FERA bus is the STR370 module. It is a dual DSP processor module with FIFO inputs which receive the FERA data. The write strobes which are generated as the FERA data is being written onto the bus are used to strobe the data into the FIFO. Thus, the write strobes coming from each FERA driver are ORed together using a logic NIM fan in module and the output is plugged into the WSI (write strobe input) of the STR370.

The readout of the FERA data is finalized by issuing an interrupt signal (I1) to the DSP processor. This interrupt activates the readout sequence such that the DSP reads its FIFO full of FERA data and puts it into local memory where the local SSP has access to it. This I1 signal is generated by two events. First the RQO pulse must be issued followed by an SSP start pulse. Thus if the trigger decides the data from a L0 trigger (which caused the gate to the FERA system) is not worth saving (a required L1.N trigger failed), the RQO signal will be generated without activating the DSP to readout the FIFO because of the lack of an SSP start signal. One should keep in mind that for every gate, one will necessarily get an RQO pulse since it is generated every time the data stops being written to the FERA bus. So the rule is, the DSP is interrupted only after the RQO pulse is generated and an SSP start signal is issued by the trigger.

Special attention needs to be payed to the clear sequence of the FERA system such that one does not corrupt the L1.2 trigger or the state of the STR370 module. During the 1997 AGS run, the DAQ system would hang due to subtle problems with clears to the FERA systems. The general rules for clearing the FERA system are as follows.

1. A clear must be sent to the FERA system before it receives a gate. If the FERA system is not cleared, then the subsequent gate from the trigger system will be ignored and no data will be written onto the FERA bus.

2. The FERAs must be cleared before the level 1.2 trigger system. The level 1.2 trigger uses the data from the FERA bus to make its trigger decision, thus the FERA bus must be quiescent, in its reset state, before the L1.2 is cleared. Otherwise, the L1.2 gets reset, and then starts processing the junk data on the FERA bus as its being cleared and thus setting the L1.2 into an unknown state.

3. The latch which generates the I1 pulse needs to be cleared after the FERA bus is cleared. Otherwise it can be reset before an RQO from a cleared event comes along and sets the latch into a wrong state and eventually causes the DAQ system to crash.

The basic setup of the FERA/STR370 control system is drawn in figure 1. In order to keep the

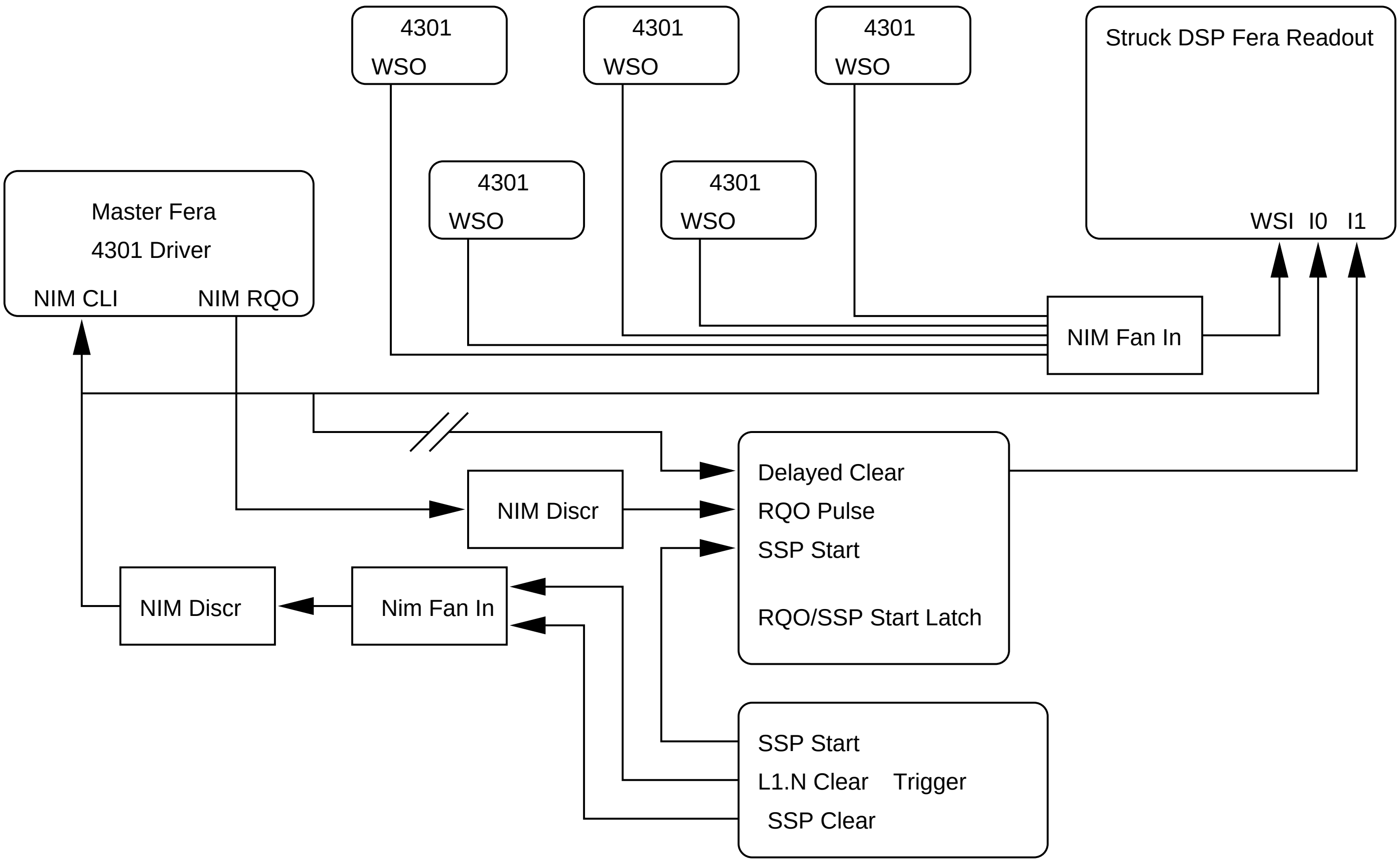

Figure 1: This is a caption

drawing simple, all fanout modules and level converters have been omitted. The obvious NIM and ECL signal conversion will not be discussed. One bit of information about level conversion which does need mentioning is that the I0 and I1 signals into the STR370 are TTL levels so a NIM to TTL level converter is employed in the FERA control system.