VIII. Basic Process Description

S. Kayali

A. Typical Ion-Implanted MESFET Process Flow

The starting wafers must be selected based on the specific process requirements. Low-noise processes require a different set of starting material characteristics than power processes, and each manufacturer has a defined set of wafer characteristics based on the selected process. A typical MESFET process flow is shown in Figures 3-29 and 3-30 with some optional steps shown for clarity and completeness of flow.

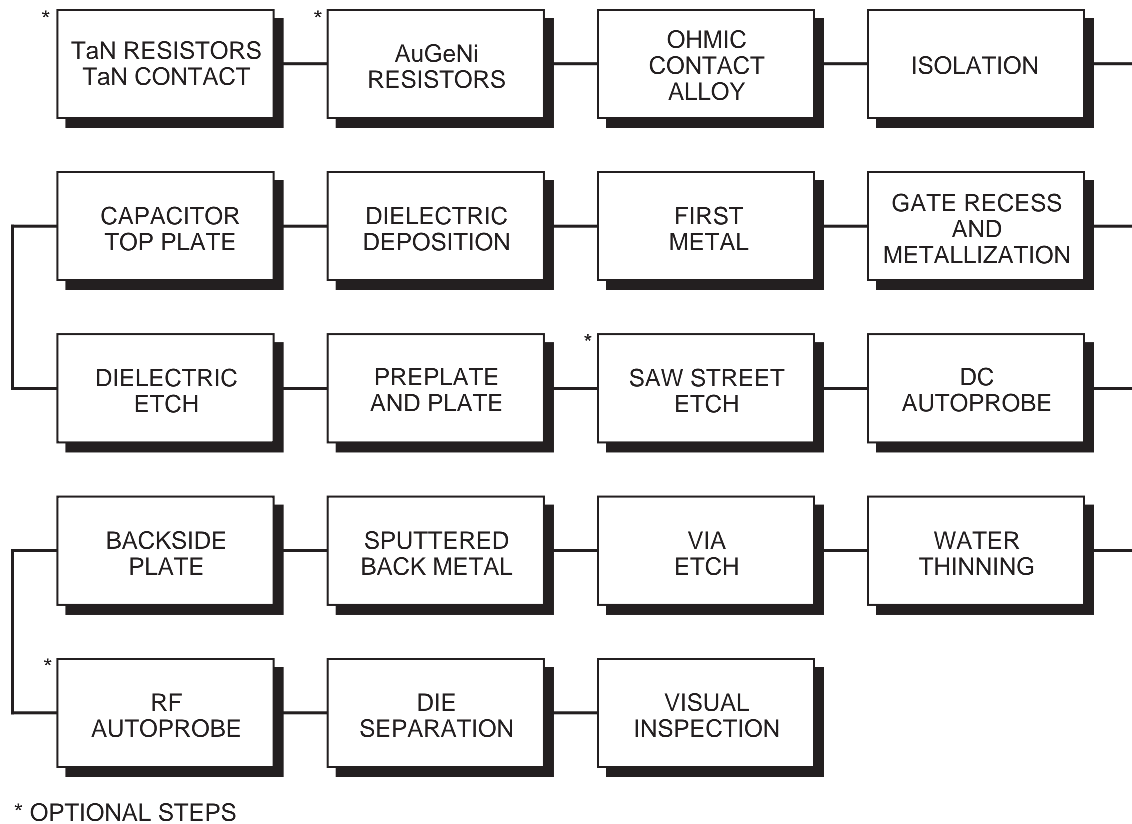

Figure 3-29. Basic sequence of process steps.

1. Resistor Deposition and Ohmic Formation

The first step normally involves the fabrication of the thin-film resistors. The AuGeNi resistor metal is evaporated, and the TaN resistor metal is sputtered and followed by a TaN contact-metal evaporation step. AuGeNi is normally used for designing low-value resistors, while TaN is used for medium-value resistors. An ohmic-contact deposition step normally follows with an alloy step, which results in a low-resistance ohmic contact to the active GaAs and also serves to stabilize the metal-film resistors.

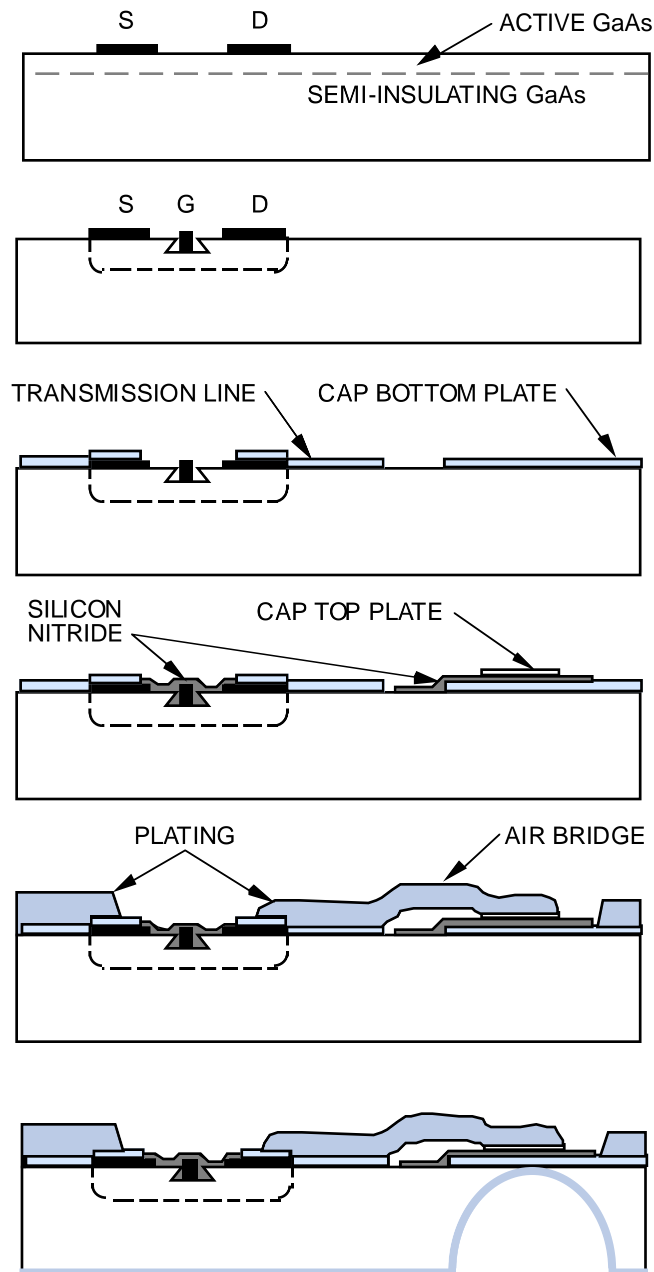

Figure 3-30. Basic process steps for MESFETs.

2. Isolation and Gate Formation

An ion implant such as boron is used to deactivate the conducting GaAs layer and form isolation patterns where desired. A direct-write e-beam can then be used to pattern the gate and gate recess in the active areas.

3. Metal and Dielectric Deposition

The first metal layer is normally an evaporated metal layer, which contacts the semi-insulating GaAs and forms the first-level interconnect. Dielectric deposition of

silicon nitride is used to protect circuit elements and provide a dielectric for capacitors. Capacitor top-plate metal is then deposited on top of the silicon-nitride dielectric. A pattern step is implemented to open the contact and define the bottom plate of the capacitor. Figure 3-31 shows a cross section of thin-film resistors and ohmic contacts on GaAs.

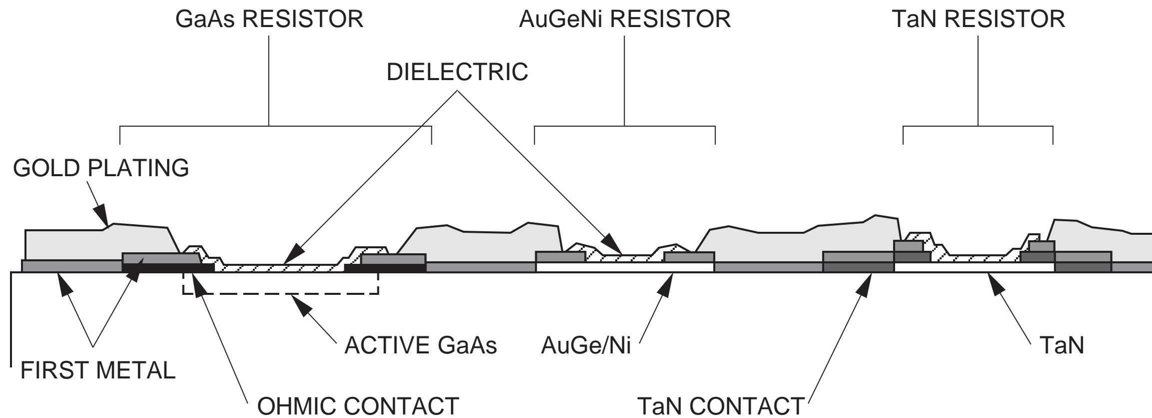

Figure 3-31. Basic process steps for GaAs, AuGeNi, and TaN resistor.

4. Plated Metal and Air Bridges

Plating is used to deposit thick layers of gold to construct air bridges, low-loss transmission lines, high-current-carrying lines, bond pads, resistor contacts, and evaporated metal step coverage. Two resist patterns are required to define the plated gold layer; the preplate and plate patterns work together to define the electroplated gold-metal level. The preplate layer defines the areas where the plating contacts underlying metal. The plate level defines the horizontal extent of the plated region. The preplate resist pattern is deposited directly on the front side of the wafer. Openings in the preplate resist are exposed and developed to define those areas where the plated metal will contact the underlying metal layer. The underlying metal is usually first metal, but plated metal can also contact capacitor top plates and other conducting layers.

After the preplate pattern is formed, a thin layer-to-metal contact is sputtered onto the entire wafer. This is the "preplate metal," which serves to carry the electroplating current. On top of the preplate metal , a second resist pattern is formed to define the horizontal extent of any plated geometry, whether it is part of an air bridge or in contact with underlying metal. The preplate metal is removed, along with the photoresist, in all unplated areas. The preplate metal remains underneath all plated areas. Figures 3-32(a) and (b) show the air-bridge process.

5. Via Holes and Backside Processing

To allow for electrical connections between the frontside metal and the backside ground plane, via holes are formed and plated with gold. The size of the via hole depends on the substrate thickness; a circular pattern having a 50- to 60-µm diameter is normally used on 100-µm thick substrates. The plated gold layer also serves as the contact layer for die attach and a thermal path to a substrate. In processing, the via diameter at the frontside contact may vary from 12 to 160 µm on 100-µm-thick substrates. At backside, the via may be 2 to 3 times larger than the frontside pattern. Figure 3-33 shows the via hole and the process-dependent parameters.

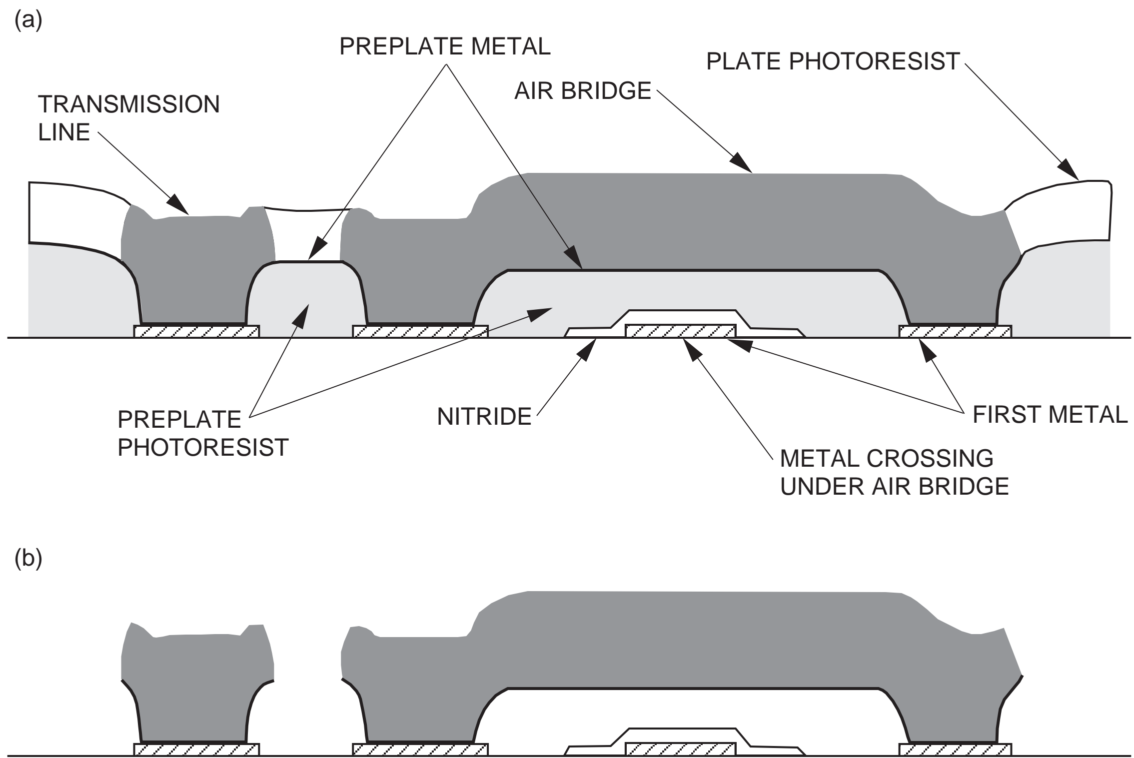

Figure 3-32. The air-bridge process: (a) with plate and preplate photoresist patterns and (b) after resist is removed.

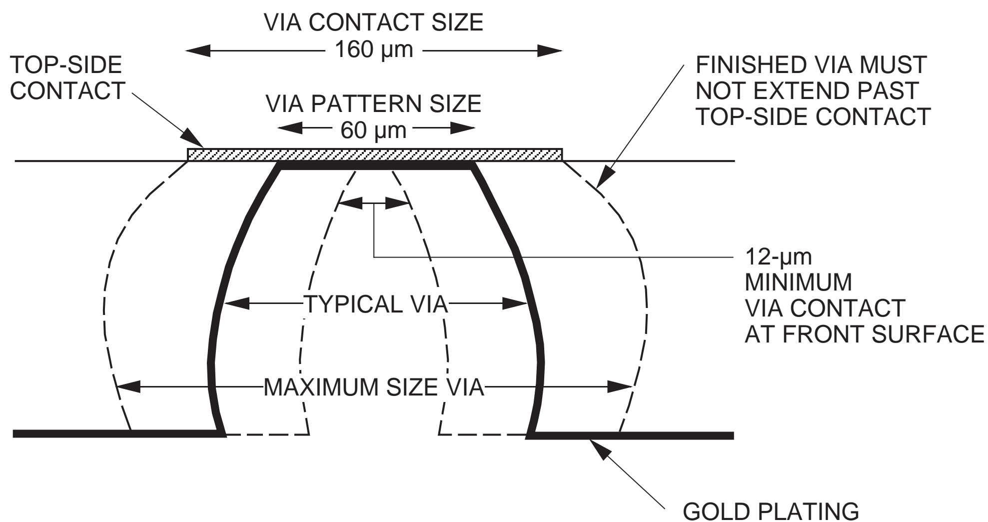

Figure 3-33. Via hole with process-variable parameters.

Reactive Ion Etch (RIE) is normally used to open the backside via holes. A layer of sputtered metal is then deposited over the entire backside of the wafer. Gold plating, approximately 6 µm thick, is then added to the sputtered metal for the die-attach capability.

The last step in the process is to physically separate the devices on the wafer. This is done by either scribing and breaking apart the devices or by using areas called saw streets, which are strips void of plated metal and are the outer boundaries of the individual MMICs. Final visual inspection is normally used in conjunction with dc probe data to select acceptable devices.

B. Typical HEMT/PHEMT Process Flow

The starting materials for HEMT-based devices require specific and stringent parameter control. Device manufacturers normally specify the applicable parameters that affect their process and are suitable to the processing flow. After the usual wafer cleaning and inspection, an epitaxial layer must be grown to provide the required material characteristics necessary for HEMT and PHEMT devices. The process starts with a GaAs buffer layer epitaxially grown to isolate defects from the substrate and provide a smooth foundation for further growth of the active layer of the transistor. A superlattice structure of undoped alternating layers of Al_xGa_{1-x} As and GaAs is them grown to further inhibit substrate conduction. The active channel is then grown using undoped GaAs in HEMT and undoped InGaAs in PHEMT. A spacer layer of undoped AlGaAs is then grown to separate the 2DEG from any ionized donors generated by the active layer. An n^+ AlGaAs donor layer is then grown to provide a source of electrons and to complete the growth of the HEMT/PHEMT epitaxial layer. Further processing steps complete the device structure and define the contact areas of the MMIC.

Differences exist in the fabrication of HEMT and PHEMT devices, but the general approach and processing flow remain essentially the same. Further details of the device structure and operation are found in Section 3-IV. The following brief description of the general processing flow is depicted in Figure 3-34.

1. Active Channel Definition and Isolation Implant

Using wafers with the epitaxial layers described above, a photoresist masking step is used to define the desired active channel area of the device. An isolation implant is then used to eliminate lateral conduction between devices. The resist layer can then be removed to expose the GaAs surface for the next process step.

2. Ohmic-Metal Formation

A photoresist masking step is used to define the desired ohmic-metal contacts. This metal is normally evaporated and then alloyed to provide the desired ohmic characteristics. Source and drain contacts along with capacitor bottom plates, resistor contacts, and, if applicable, inductors can be applied in the same process step.

3. Gate-Recess Formation

Photoresist masking and etching steps are then used to define the gate-recess areas. The etch depth and profile play major roles in the final characteristics of the device and should be carefully studied and characterized.

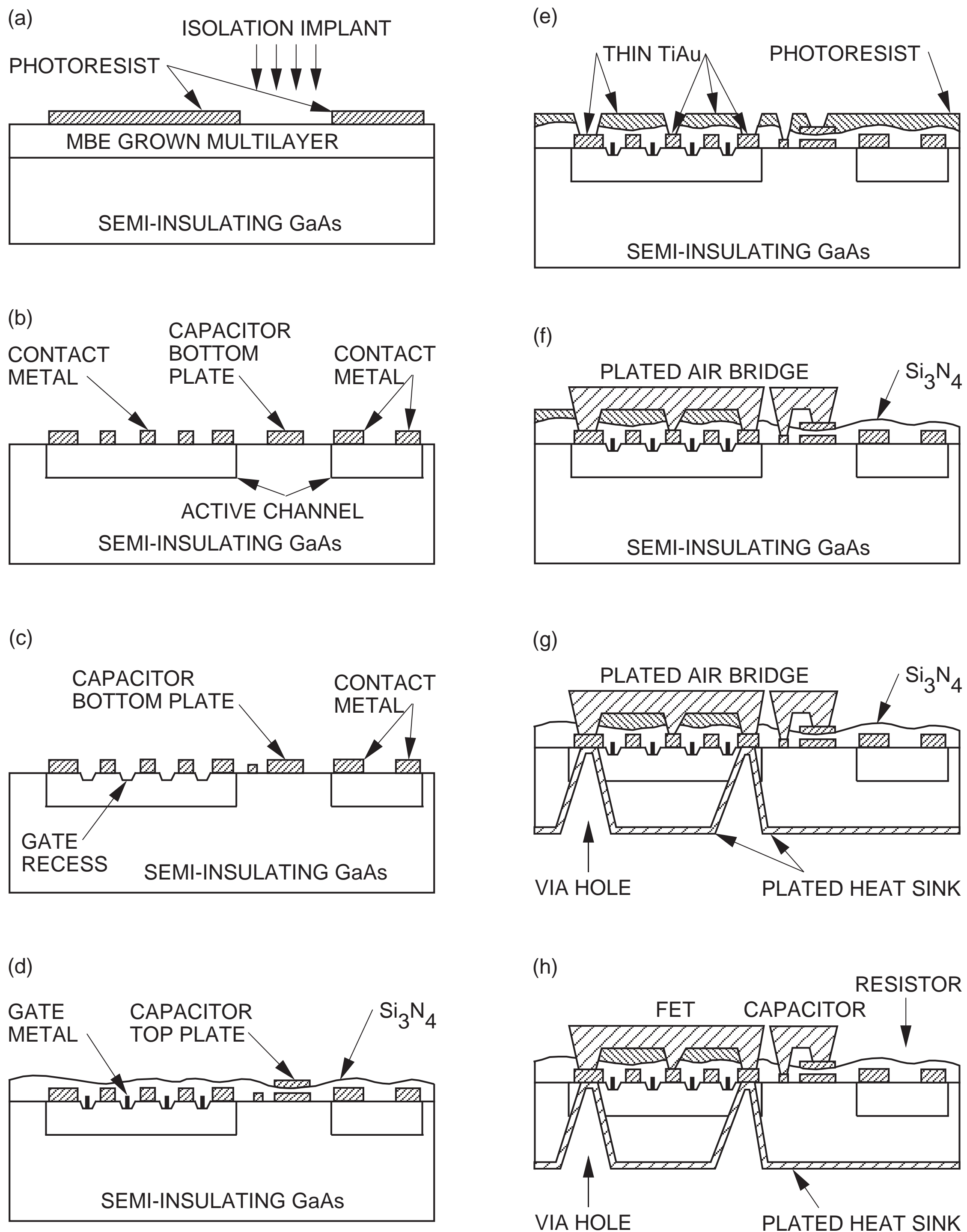

Figure 3-34. Typical HEMT/PHEMT process flow: (a) active channel definition and isolation implant, (b) ohmic-metal formation, (c) gate-recess formation, (d) gate-metal formation and nitride deposition, (e) source and contact etch, (f) air-bridge formation, (g) via-hole formation and backside processing, (h) completed typical MMIC structure.

4. Gate-Metal Formation and Nitride Deposition

Gate metal is normally sputtered or evaporated to form the desired Schottky contact. A nitride layer covering the active areas and forming the dielectric layer for capacitors is then applied. The actual method and conditions for gate-metal and nitride application are critical to the performance, characteristics, and stability of the devices being manufactured.

5. Source and Contact Etch

A photoresist masking step is normally used to pattern the source and other contact openings. A thin layer of TiAu is also applied to help in the next step of air-bridge plating. At this step, wafers can be mounted face down to perform the thinning operation. The wafers are normally thinned down to a thickness of about 25 mils.

6. Air-Bridge Formation

After cleaning the front side of the wafers, a thick layer of Au in normally plated to form the air-bridge structures. An etch to remove photoresist for the undesired locations is also performed.

7. Via-Hole Formation and Backside Processing

A photoresist masking step is used to identify the desired via-hole location. An etch after exposure of the photoresist can provide the backside contact. An Au layer is normally plated to serve as an electrical and thermal path.

8. Complete Typical MMIC Structure

The completed MMIC structure is now ready for probe test, dicing, and further packaging.

C. Typical HBT Process Flow

This section describes a typical mesa process flow used for fabrication of devices based on a non-self-aligned HBT process. Other possible processes and fabrication flows are practiced by various device manufacturers to provide higher yield and device performance.

The device fabrication sequence basically consists of etching steps to reveal the various layers in the structure and fabricating electrical contacts to each layer. Finally, devices are isolated and interconnections are made within each device as well as between devices. The following general steps as shown in Figure 3-35 are applicable to this flow:

1. Emitter Contact

The lift-off technique is generally used to achieve an ohmic (nonrectifying) contact on GaAs. Typically, AuGe/Ni/Au layers are evaporated in sequence and then alloyed to form the ohmic contact. The choices of alloying temperature and time play an

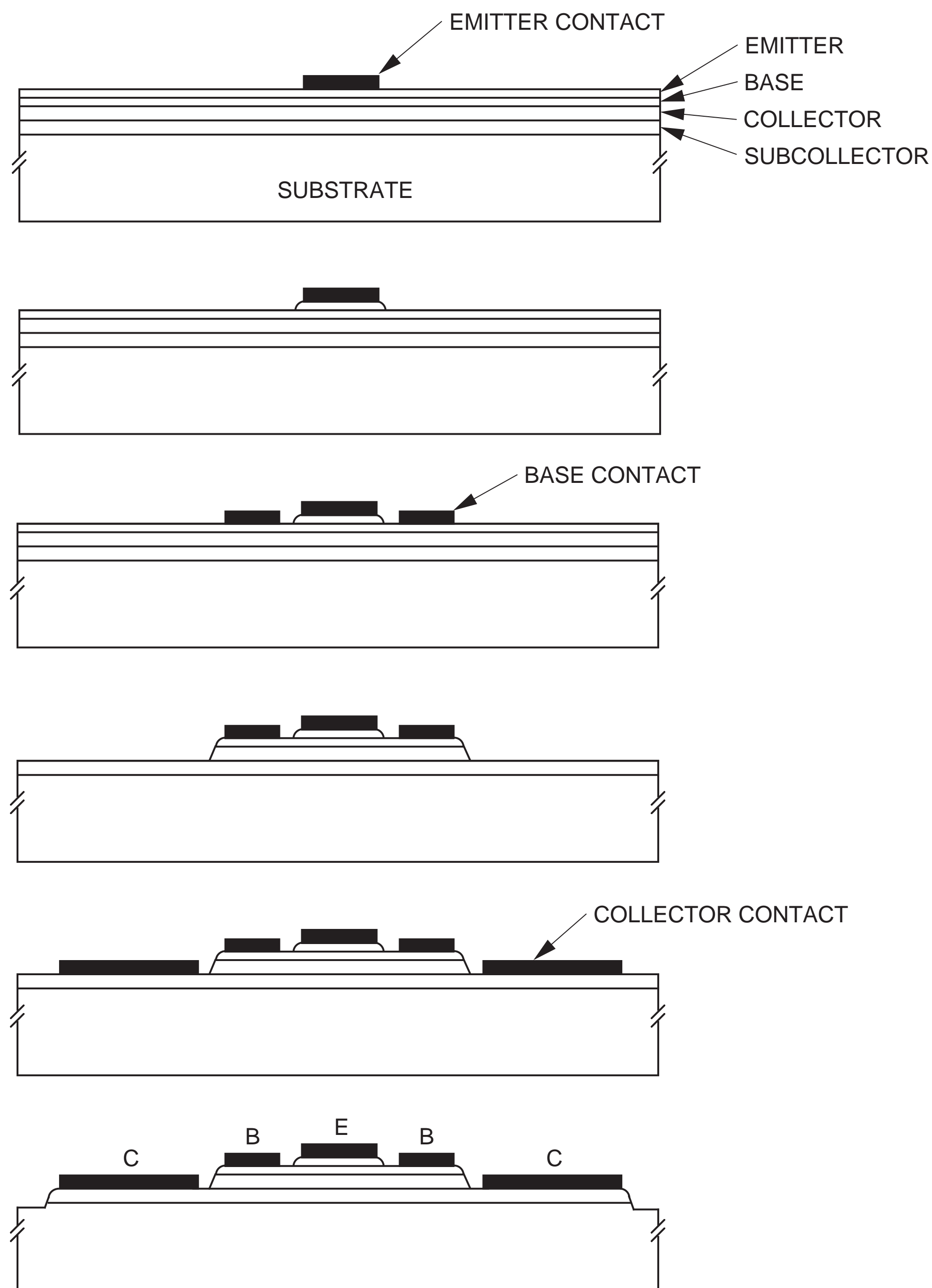

Figure 3-35. A typical HBT device processing sequence. (Courtesy of Artech House.)

important role in the quality and long-term stability of the contact. Other materials such as AuGe/Ni/Ti/Au, PdGe and Ti/W/Au can also be used for achieving this application.

2. Base Contact

A photoresist layer is generally used to mask the defined base contact area, a wet-etching or dry-etching step is then used to remove the emitter layer at the defined location, and the lift-off technique is again used to form the base contact. Alloyed contacts using materials such as AuBe, AuZn, or AuMg are common for ohmic contact formation. However, nonalloyed contacts using materials such as Ti/Pt/Au are also common.

3. Collector Contact

A process similar to that used for the emitter contact is used to achieve the collector contact. A photoresist layer masks the desired area, and the defined area is then etched using either a dry or a wet etching step. Finally, the lift-off technique forms the collector contact using the same metallization scheme as that used for the emitter contact.

4. Isolation and Interconnection

Device-to-device isolation is generally achieved by the use of wet or dry etch to remove the subcollector layer, as shown in Figure 3-35. Ion implantation can also be used to achieve the same result. Interconnection, on the other hand, can be achieved by the use of air bridges.

Other processing techniques employing self-aligned contacts (Figure 3-36) and planar structures (Figure 3-37) can provide improved device performance and higher levels of integration. Ion implantation is generally used to form conductive channels and semi-insulating layers. Planar structures can provide the added advantage of access to the various device terminals without the need of air bridges. This can provide a substantial improvement in device yield.

Additional Reading

Ghandi, S. K., *VLSI Fabrication Principles,* John Wiley & Sons, New York, 1982.

Texas Instruments GaAs Foundry Services Design Guide, Texas Instruments, 1993.

Williams, R., *Modern GaAs Processing Methods,* Artech House Inc., Boston, 1990.

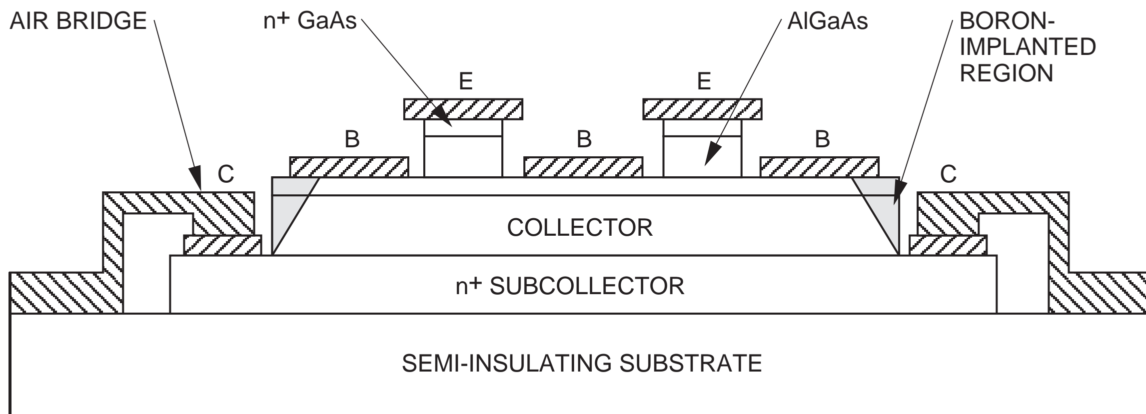

Figure 3-36. Self-aligned HBT cross-sectional view. (Courtesy of Artech House.)

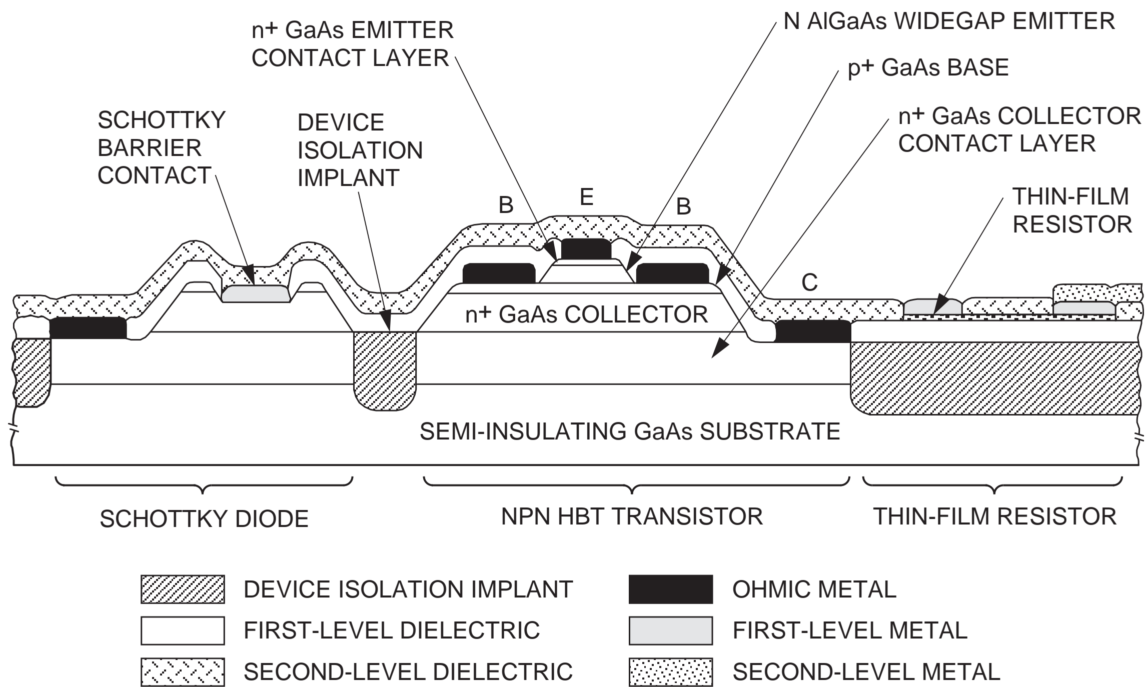

Figure 3-37. Schematic cross section of the self-aligned HBT IC structure with integrated NPN transistor, Schottky diode, thin-film resistor, and metal–insulator (SiN)–metal capacitor (not shown). (Courtesy of Artech House.)