CFT/CPS Axial Daughterboard
Printed Circuit Board
Fabrication Specifications

11 May 2000

General Information

The CFT/CPS Axial Daughterboard (CFT_DB) is a 7.800” x 4.125” printed circuit board with ten layers. There are 2788 holes ranging in size from 0.012” to 0.090” – all holes are plated-through. The CFT_DB is an impedance controlled board; use the layer stackup listed in this document. Additionally, there is selective gold plating on the “solder” side.

BOARD SPECIFICATIONS

size:	7.800" x 4.125"
board thickness:	0.0906”
board material:	FR4
layers:	10
solder mask:	BOTH sides LPI, color = BLACK
silk screen:	BOTH sides, color = WHITE
special plating:	selective 1.25 µm “hard” gold plating on bottom layer (see below)
finish:	ENTEK (organic)

FILENAMES:

** NOTE **

Gerber files are in extended gerber format.
All gerbers are POSITIVE IMAGE.

TOP routing layer	top.gbr
GROUND plane	ground.gbr
inner routing layer	inner1.gbr
inner routing layer	inner2.gbr
inner routing layer	inner3.gbr
inner routing layer	inner4.gbr
inner routing layer	inner5.gbr
+3.3V power plane	vcc3.gbr
+2.5V power plane	vcc2.gbr
BOTTOM routing layer	bot.gbr
soldermask top	smt.gbr
soldermask bottom	smb.gbr
silkscreen top	sst.gbr
silkscreen bottom	ssb.gbr
solder paste top	spt.gbr
solder paste bottom	spb.gbr
cnc drill tape	thruhole.tap
drill drawing	drd.gbr
assembly drawing top	ast.gbr
assembly drawing bottom	asb.gbr

LAYER STACKUP

Use the following layer stackup to achieve a total pressed board thickness of 0.0906". Top and bottom layers are ½ oz foil; all other layers are 1oz copper.

1. top routing	TOP.GBR	"COMPONENT SIDE"
0.075" prepreg		
2. ground plane	GROUND.GBR	
0.010" core		
3. inner routing	INNER1.GBR	
0.075" prepreg		
4. VCC2 plane	VCC2.GBR	
0.010" core		
5. inner routing	INNER2.GBR	
0.005" prepreg		
6. inner routing	INNER3.GBR	
0.010" core		
7. inner routing	INNER4.GBR	
0.075" prepreg		
8. inner routing	INNER5.GBR	
0.010" core		
9. VCC3 plane	VCC3.GBR	
0.075" prepreg		
10. bottom routing	BOT.GBR	"SOLDER SIDE"

COLORS

silkscreen = White, both sides

soldermask = Black, LPI, both sides

THRUHOLES

4 different hole sizes
12 mil hole is smallest
90 mil hole is largest.
no blind or buried vias
refer to dp_drd.gbr for fabrication data and hole legend
2788 holes total

BOARD TESTING

Each board must be electrically tested with a flying head probe or bed of nails fixture. Boards which pass a netlist connectivity test must be clearly stamped with a quality mark. Defective boards which must be "kludged" or repaired with conductive ink or paint in order to get them to pass this electrical test *are not acceptable.*

MISC.

- Selective 1.25 µm "hard" Gold plate pads on the "solder side" of the board. Refer to the bottom assembly drawing (ASB.GBR) for more information.

- Please supply to-scale photoplots for the ten layers listed in the LAYER STACKUP section listed above.

Contact Information

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