Chemical-mechanical polishing: enhancing the manufacturability of MEMS

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ABSTRACT

The planarization technology of Chemical-Mechanical-Polishing (CMP), used for the manufacturing of multi-level metal interconnects for high-density Integrated Circuits (IC), is also readily adaptable as an enabling technology in MicroElectroMechanical Systems (MEMS) fabrication, particularly polysilicon surface micromachining. CMP not only eases the design and manufacturability of MEMS devices by eliminating several photolithographic and film issues generated by severe topography, but also enables far greater flexibility with process complexity and associated designs. Thus, the CMP planarization technique alleviates processing problems associated with fabrication of multi-level polysilicon structures, eliminates design constraints linked with non-planar topography, and provides an avenue for integrating different process technologies. Examples of these enhancements include: an simpler extension of surface micromachining fabrication to multiple mechanical layers, a novel method of monolithic integration of electronics and MEMS, and a novel combination of bulk and surface micromachining.

Keywords: surface micromachining, polysilicon, microelectromechanical systems, chemical mechanical polishing, planarization

1. INTRODUCTION

The intent of this paper is to overview the benefits of wafer planarization by chemical-mechanical-polishing (CMP) for MicroElectroMechanical Systems MEMS fabrication. CMP is readily adapted to the MEMS fabrication technology known as polysilicon surface micromachining. A brief description of CMP process technology followed by a cursory description of polysilicon surface micromachining clearly illustrate why CMP is compatible and how surface micromachining benefits from this technology. We then provide several examples of how CMP enhances the manufacturability of a standard, non-planarized surface micromachining process. The final sections discuss new design and process directions enabled through the use of CMP planarization.

2. CHEMICAL-MECHANICAL POLISHING

CMP processes produce both global and local planarization through relatively simple and quick processing. Figure 1 illustrates the CMP process in which an oxide surface is planarized by rotating a wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry. The theory of oxide polishing is not well understood, however, it is generally accepted that the alkaline chemistry hydrolyzes the oxide surface and sub-surface thus weakening the SiO_2 bond structure[1]. The mechanical energy imparted to the abrasive slurry particle through pressure and rotation causes high features to erode at a faster rate than low features, thereby planarizing the surface over time.

For the particular results shown here, a colloidal-fumed silica slurry (Cabot SS-12) and a polyurethane pad (Rodel IC1000/Suba IV) are used.

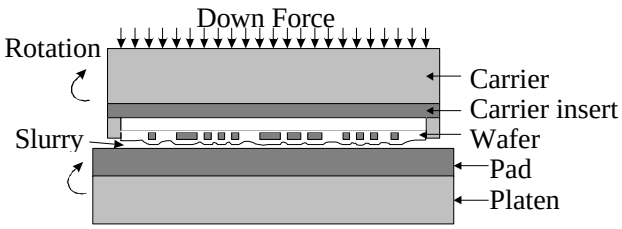


Fig. 1 Schematic representation of CMP process in which an oxide surface is planarized by rotating the wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry.

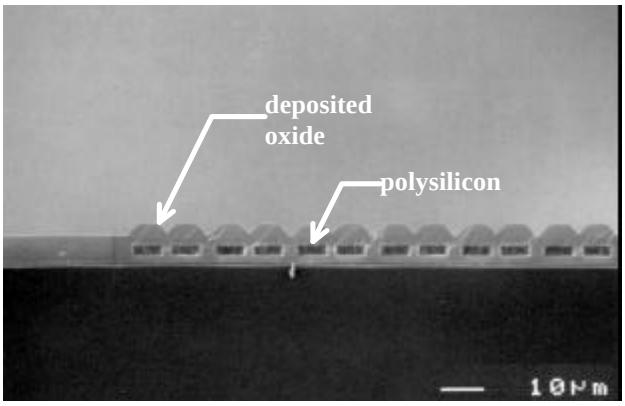


Fig. 2 SEM cross-section of a partially-fabricated micromachine illustrating the uneven, severe topography before CMP planarization.

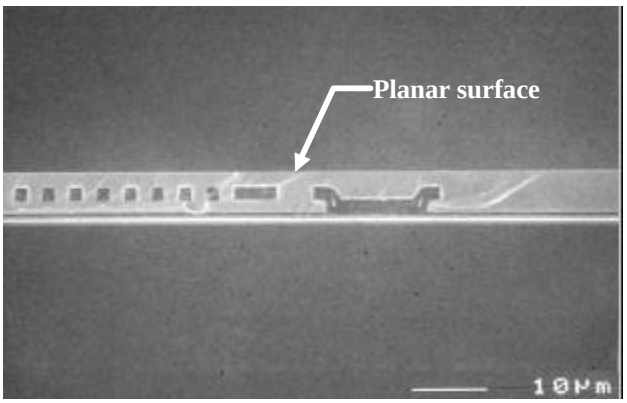


Fig. 3 SEM cross-section of a partially-fabricated micromachine after CMP planarization. Note the planarity of the upper oxide surface.

One of the main differences between planarizing inter-level dielectric materials used in ULSI interconnect technology and planarizing sacrificial oxide material used in MEMS technology is the large step heights (2-4 μm vs. 0.8 μm) associated with polysilicon surface micromachined MEMS. These large step heights present a challenge to any planarization strategy. Figures 2 and 3 show the surface topography of single level polysilicon structure prior to CMP (2) and after the CMP process (3). As can be seen from the figures, CMP does an excellent job of removing the ~ 2 μm step height and planarizing the oxide surface.

2. ENHANCED MANUFACTURABLILITY OF SURFACE MICROMACHINED MEMS

MEMS process technologies, and in particular polysilicon surface micromachining[2,3], have been plagued by process issues generated by severe vertical topography which is introduced by the repetitive deposition and etching of multiple films. Polysilicon surface micromachining readily adapts to the inclusion of CMP and clearly illustrates the benefits of CMP for several reasons. Surface micromachining uses the planar fabrication techniques and films common to the microelectronic circuit fabrication industry to manufacture micromechanical devices. The standard building-block process consists of depositing and photolithographically patterning alternate layers of low-stress polycrystalline silicon and sacrificial silicon dioxide. The result is a construction system consisting of one layer of polysilicon which provides electrical interconnection and one or more independent layers of mechanical polysilicon which can be used to form mechanical elements ranging from simple cantilevered beams to complex systems of springs, linkages, mass elements and joints. At the completion of the process, the sacrificial layers, as their name suggests, are selectively etched away in hydrofluoric acid (HF), which leaves the free-standing polysilicon layers. Figure 4 illustrates both the essence of polysilicon surface micromachining and clearly displays the vertical topography which arises during the non-planarized process. This topography can produce mechanical interference between moving parts, and complicates subsequent process steps.

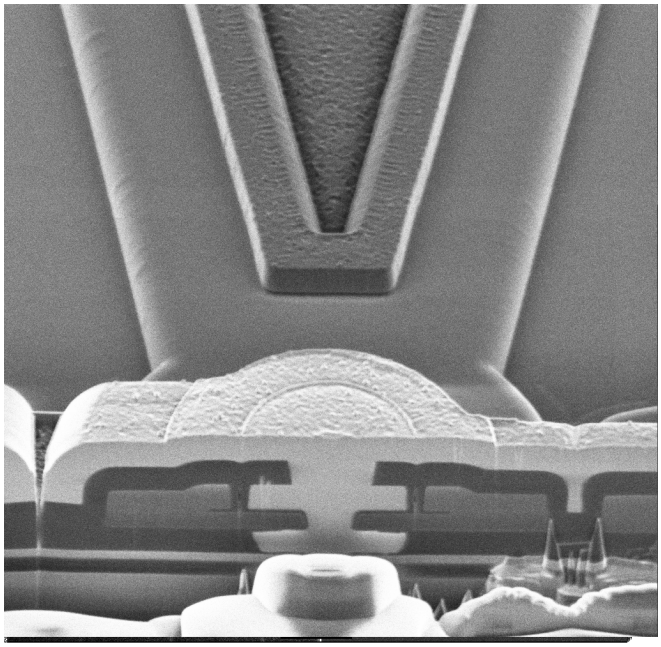
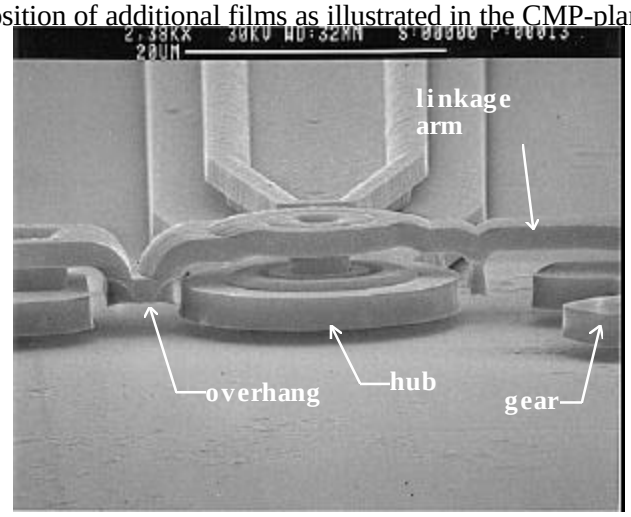


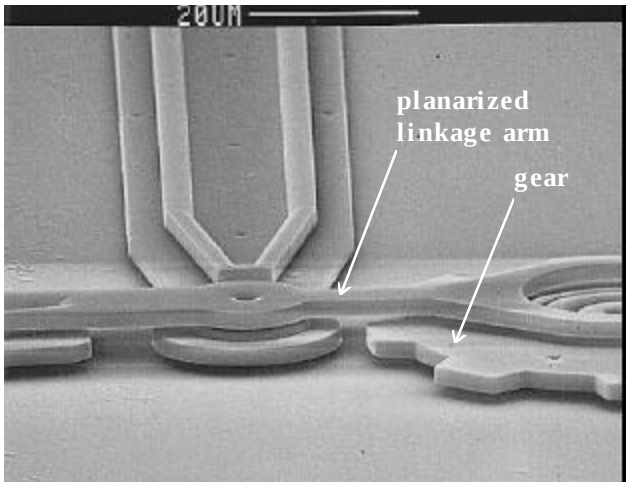
Fig. 4 Focused Ion Beam (FIB) milled cross-section of a mechanical joint formed in a three-layer polysilicon surface micromachining technology[2]. The final mechanical polysilicon film is the upper light-colored film which illustrates the topography and the interference artifacts generated (arrows) by the previous film steps. The film thicknesses are on the order of 2μm for both the mechanical polysilicon films and the sacrificial silicon dioxide films.

The mechanical interference arises when an upper layer of polysilicon must pass over the edge of a previously etched lower layer. An example of this interference, taken from the microengine[3], can be seen in Fig. 5a where the

upper link runs over the edge of the gear causing an overhang feature. This feature is due to the conformal deposition of the polysilicon film. Link/gear interference can be alleviated by the microengine design, or by planarization of the surfaces before subsequent deposition of additional films as illustrated in the CMP-planarized joint in Fig. 5b.



(a)



(b)

Fig. 5 The SEM Fig. 5a illustrates the artifacts generated by the conformal nature of the polysilicon depositions over prior topology (indicated by arrows), while Fig. 5b illustrates the same microengine joint feature fabricated with planarization by CMP before the final polysilicon deposition. The overhang artifacts are no longer present.

In addition to the above design constraint, two significant process difficulties arise from severe topography. The first results from the use of highly anisotropic plasma etch processes for the definition of the polysilicon layers. The anisotropy is necessary to obtain the desired vertical sidewalls of the polysilicon structures. However, the very anisotropy of the etch also prevents the etch from removing the polysilicon layer from along the edge of a step. This produces long slivers of polysilicon, often referred to as stringers, along these edges as illustrated in Fig. 6. The stringers can also produce mechanical interference or even an electrical short. Secondly, photolithographic definition of subsequent layers becomes problematic over severe topography. Photoresist, the photosensitive polymeric coating used

to transfer the design into the physical films, becomes difficult to apply, expose, and develop, leading to loss of resolution and definition. Removal of these difficulties through the use of CMP aids manufacturability by reducing or eliminating photolithography reworks.

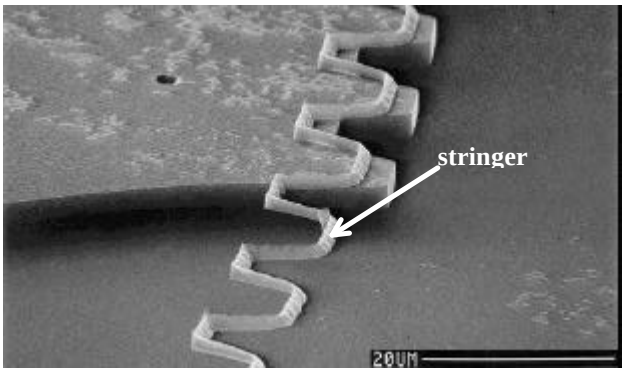


Fig. 6. Polysilicon stringer next to a gear edge. The stringer was formed during a later polysilicon deposition and patterning.

Thus, the addition of chemical-mechanical polishing (CMP) planarization to polysilicon surface micromachining technology is a major process enhancement from both the process and design perspectives[4]. Techniques other than CMP for overcoming topography problems have also been used by researchers in the MEMS community. For example, researchers at University of Wisconsin have demonstrated locally-planarized surface-micromachined pressure sensors produced in a double LOCOS process[5]; while the use of plasma planarization has recently been demonstrated on MEMS devices by researchers at Delft[6]. Although these planarization techniques have yielded improvement in the manufacturability of MEMS devices through local planarization, CMP provides a higher quality of both local and global planarization in a manufacturing environment. CMP, best known for its global planarization use in sub-micron circuit technology[7], was first used in the MEMS field to improve the optical quality of polysilicon surface-micromachined mirror devices by smoothing the polysilicon[8]. However, the first use of CMP planarization in MEMS was reported by Sniegowski[4,9] in the application of a three-level polysilicon process for the microengine.

The benefits of CMP for surface-micromachining are four-fold. It eliminates the potential mechanical interference problem. It eliminates the artifact of anisotropic etching of conformal polysilicon films over edges, i.e. stringers, since there are no edges on a planar surface. Thirdly, the extension to four or more levels of polysilicon becomes practical since the topography and associated photolithographic problems are eliminated. Finally, CMP planarization provides an avenue to integrate separate process technologies such as microelectronics and micromechanics or surface micromachining and high-aspect-ratio micromachining. The first three benefits combine to produce higher device yield and reliability, while the latter two combine to produce exciting new processes and designs as described in section 3.

3. ADVANCED MEMS APPLICATIONS OF CMP

The previous section dealt primarily with improved manufacturability of MEMS with large topography. This section continues to illustrate enhancements to manufacturing, but principally describes new capabilities made possible by CMP-planarization.

3.1 Multi-Level Structures

Multiple levels of structural polysilicon enable fabrication of increasingly complex MEMS devices such as microengines[10] capable of driving sets of gears. Simple flexure structures such as comb drives[11] can be built in a single level of structural polysilicon while a second level enables the production of gears with pin joints. A third level enables linkages between spinning gears, but introduces severe topography problems that must be solved with a combination of careful process and device design or solved by planarization with CMP as previously described in section 2, Fig. 5. Figure 7 shows a geared transmission unit with multi-level, compound gears. Although designed to accommodate non-planar processing (as made apparent by the etch artifacts seen on the surface of the top large gear), the design was actually fabricated with CMP to produce fully functional units. A new design, not compromised with the non-planar design, will lend itself to more reliable operation.

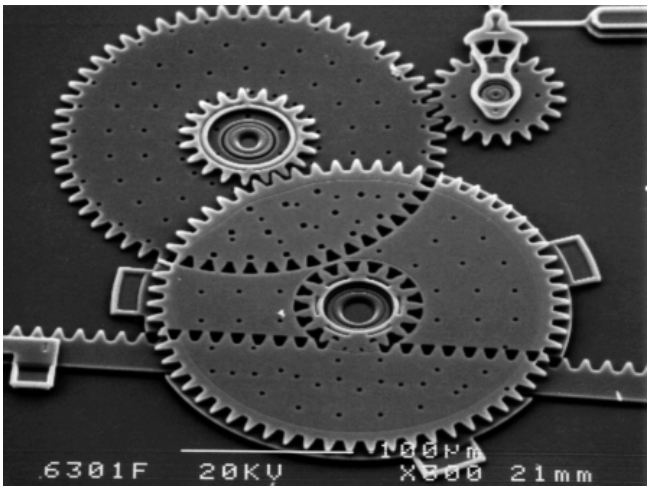


Fig. 7 is an SEM of the completed gear-speed-reduction unit and linear rack. The linear speed of the rack is approximately one tenth that of the linear tooth velocity of the drive gear. The rack has been successfully used to drive a folding mirror, for example.

Additional levels of polysilicon promise even more complex structures, but the extreme topography of these multi-level structures (four or more active layers) has prohibited their fabrication. A micromachining technology that includes planarization steps such as CMP will enable device fabrication with these additional levels.

3.2 Pressure Sensors

A planar pressure sensor technology[12] has been developed based upon a silicon nitride layer as the diaphragm material. A trench is etched ~2 μm deep in the surface of a silicon wafer. This trench is refilled with a sacrificial oxide and planarized with CMP. A silicon nitride diaphragm layer is then deposited. The sacrificial oxide underneath this

diaphragm layer is removed using HF leaving a cavity beneath the diaphragm. An additional silicon nitride layer is used to seal the cavity in near-vacuum conditions (approx. 200 mTorr). Polysilicon piezoresistors are deposited on the diaphragm to sense the diaphragm strain that results from changes in ambient pressure. A completed, 100-µm-diameter planar pressure sensor is shown in Fig. 8. This sensor shows marked improvement in planarity when contrasted against a similar, non-planar sensor shown in Fig. 9.

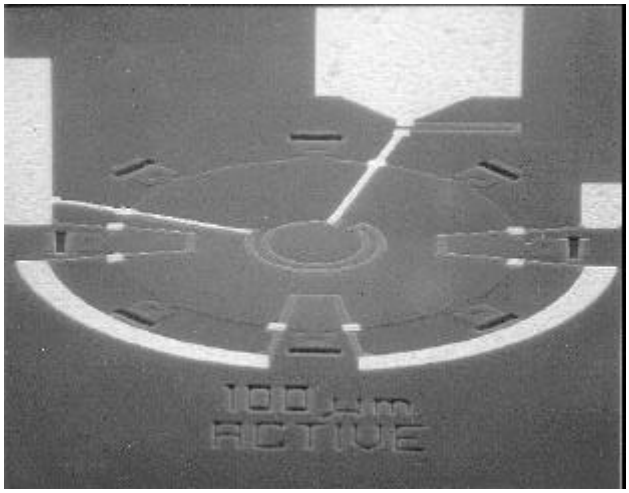


Fig. 8. Top view of a planar pressure sensor fabricated in a process that includes CMP. The reference cavity is embedded below the substrate surface, eliminating step coverage problems.

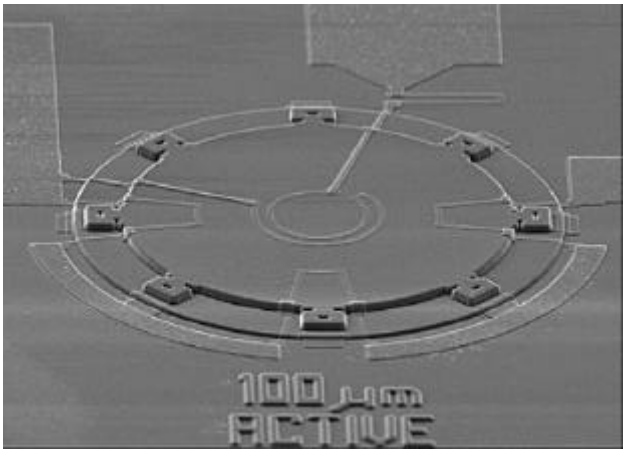


Fig. 9. Top view of a non-planar pressure sensor. The circular diaphragm covers a 2µm-high reference vacuum cavity, and is the source of step coverage problems.

In the non-planar sensor manufactured without CMP the reference pressure cavity is formed above the silicon surface producing large step heights. These steps cause processing difficulties with photoresist coverage and removal, dry etch selectivity to photoresist where the photoresist thins over steps, and metal step coverage. These challenges to manufacturing were eliminated in the CMP-planarized sensor. In the future, the use of an embedded cavity will enable the monolithic integration of this sensor technology with CMOS in a modified version of the integration process

described later in this paper, and will also enable the use of deeper vacuum cavities to extend the sensing range of the devices.

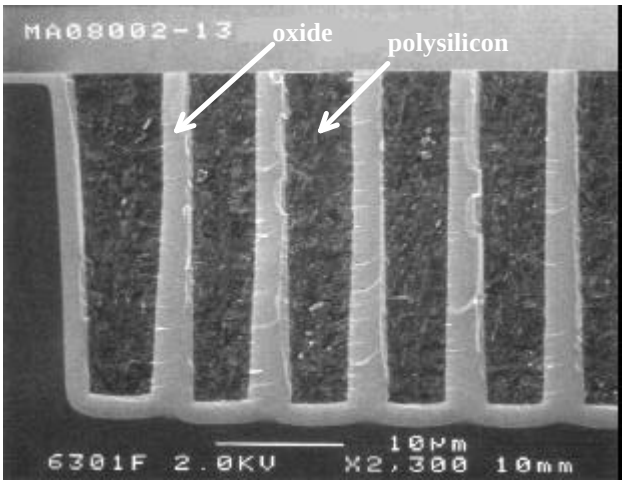


Fig. 10. Cross-section of a high-aspect-ratio polysilicon accelerometer proof mass with CMP-planarized top surface.

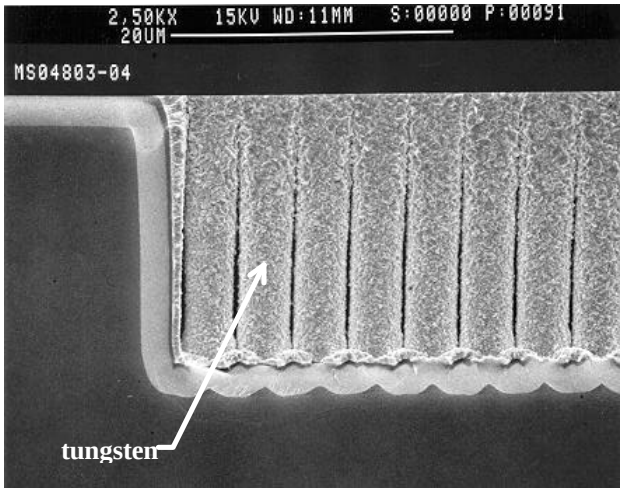


Fig. 11. Cross-section of a high-aspect-ratio tungsten accelerometer proof mass with CMP-planarized top surface.

3.3 High-Aspect Ratio Micromachining

In addition to its uses for planarization of surface-micromachined devices, CMP plays a key role in the fabrication of high-aspect ratio micromolded polysilicon and tungsten devices. In the technology presented here[13], deep, narrow trenches lined with oxide are filled with thin films (~2-5 µm) of either polysilicon as shown in Fig. 10 or tungsten as shown in Fig. 11 and planarized with CMP. These structures can then be integrated with surface micromachined polysilicon structures to form large high-aspect-ratio proof masses with compliant surface-micromachined springs as shown in Fig. 12.

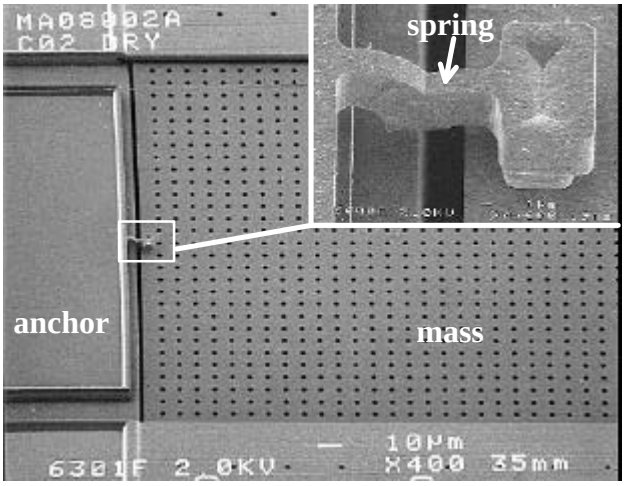


Fig. 12. High-aspect-ratio polysilicon accelerometer mass integrated with a surface-micromachined spring.

3.4 Integration of MEMS with Microelectronics

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MEMS with driving, controlling, and signal processing electronics[14]. The monolithic integration of micromachines and microelectronics enables the development of wide new classes of small, smart, products with maximum levels of system performance. A new integration scheme[15] overcomes the limitations of traditional integration schemes and enables, for the first time, the integration of micromachines of arbitrary complexity with high performance, state-of-the-art CMOS. Functionality yields in excess of 98% have been achieved with this technology[16]. An example of devices built in this technology are shown in Fig. 13.

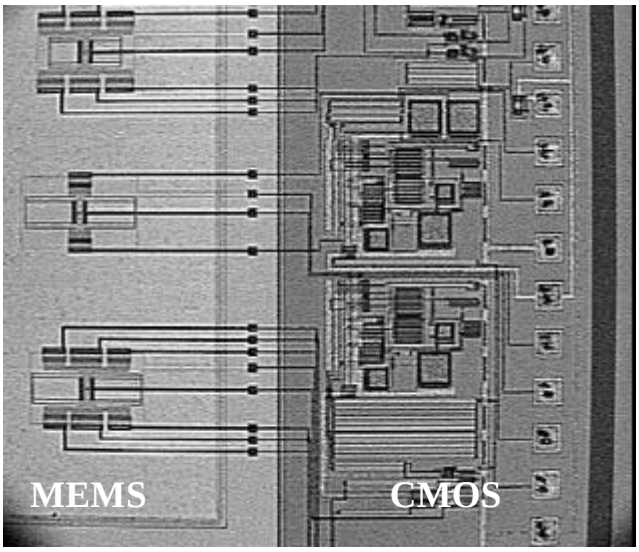


Fig. 13. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics.

We have developed this embedded MEMS approach to enhance the manufacturability, design flexibility, and performance of microelectronic/micromechanical devices. This process places the micromechanical devices in a

shallow (~6-12 μm) trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topography of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures.

Fig. 14 is a schematic cross-section of the integrated technology. Alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench is etched in (100) silicon wafers using an anisotropic etchant that preferentially etches the (100) crystal plane and produces a trench with sidewalls having a slope of 54.7° relative to the surface. This slope aids in the subsequent photo patterning within the wells.

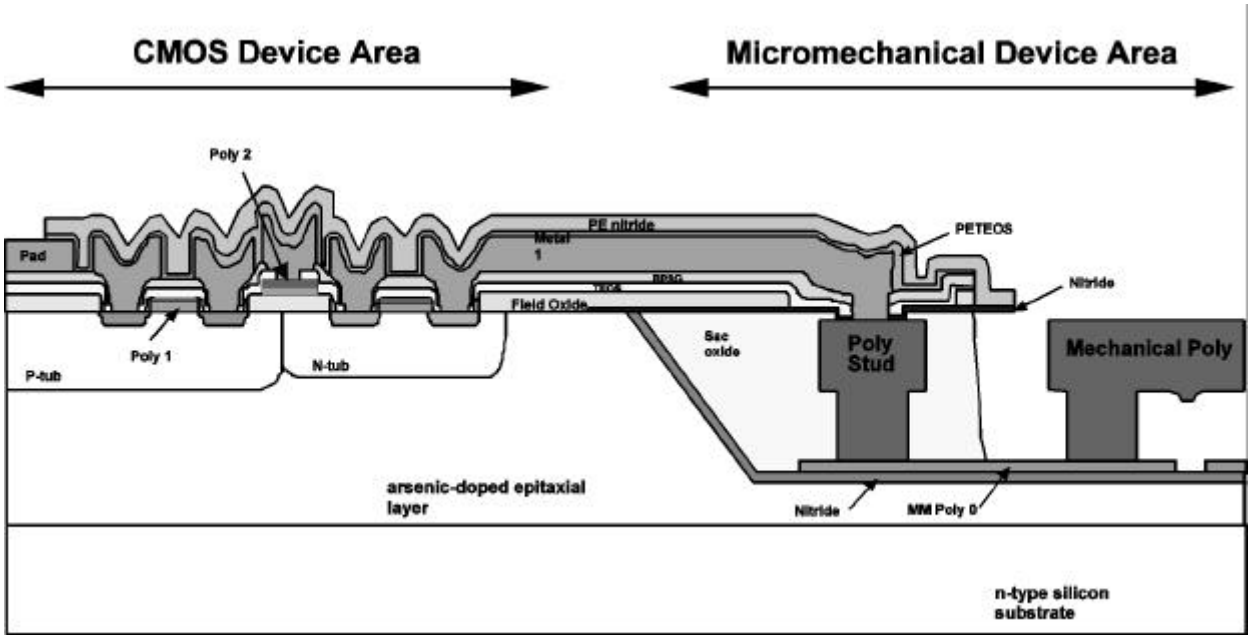


Figure 15. Cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench. This approach is used to optimize level-to-level registration and resolution of features within the trench. Feature sizes with critical dimensions as small as 0.8 μm, the limit of g-line lithography, were successfully defined within the trench.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS devices; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the planarized trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires an additional step to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures. Photoresist is used as a protection layer over the exposed bond pads during the release process.

This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. A planarized wafer with the embedded MEMS can serve as starting material for a conventional microelectronics foundry service since the technology does not require significant modifications of standard microelectronic fabrication processes.

4. CONCLUSION

Once the basic chemical-mechanical polishing planarization technique for silicon dioxide over polysilicon is set-up and developed in a fabrication line, the process is readily adaptable for use in polysilicon surface micromachining. Although the planarization is a conceptually "simple" step, the impact of its inclusion in the overall fabrication process is immense. Manufacturing impediments are removed while novel, expanded processes and designs become possible. CMP increases yield and functionality of many of device design which had previously been processed with a non-planarized technique. Expanded processes can entail the inclusion of four or more layers of mechanical polysilicon films for more complex out-of-plane structures. Novel processes such as combining trenched structures with surface-micromachined structures or monolithic integration of MEMS with circuitry by embedding the MEMS in a planarized well can be realized. Further, a change in design perspective occurs since the need to circumvent mechanical interference in a non-planarized process is alleviated. Thus, more complex designs with greater functionality yet created from simpler stepwise designs are feasible.

We anticipate that CMP planarization, in the next few years, will be used extensively within the MEMS community for polysilicon surface micromachining. In addition, other MEMS fabrication technologies such as bulk micromachining and LIGA can potentially benefit from CMP, however CMP may not be as suitable for adaptation to these technologies as it is to surface micromachining.

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