Intrinsically Radiation-Hard Fully-Depleted CCDs with High Signal-to-Noise

Outline:

- Overview of Technology
- Application in Astronomy
- Performance
- Beam Test Result - Radiation Hardness
- Current Plans
- Conclusion

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Participants in High-Resistivity CCD Development

LBNL:

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History of Development

High Resistivity Silicon Techniques developed for SSC pixelated detectors

Development of Technique (“Holland Gettering Process”) for reducing impurities from the sensitive region resulting in low reverse diode leakage currents in high-resistivity silicon.

Development of integrated detectors and electronics on n-type high-resistivity silicon

P-channel MOSFET’s and silicon P-I-N diodes simultaneously fabricated on high-resistivity silicon using conventional CMOS processing.

Manufacture of high performance stripdetector with integrated amplifiers.

Development of P-I-N photodiode on high-resistivity n-type silicon for use with CsI crystal in P.E.T. medical device research.

Key innovation in developing fully-depleted P-I-N photodiode with backside transparent contact for application of depletion voltage and integral AR coating. Devices have exceptional IR sensitivity.

First development of fully-depleted MOS CCDs on high-resistivity n-type silicon.

LBL CCDs

Made on 300 μm thick float-zone high-purity n-type high-resistivity (~ 10 kΩ-cm) silicon.

Operated overdepleted with a >25 V bias. Depletion voltage applied through backside contact. Entire volume is sensitive.

Made with conventional MOS processing.

Three phase, buried p-channel, full frame transfer, inverted mode operation.

Backside polysilicon gettering layer is used to maintain low dark currents which was a significant problem with initial attempts to develop CCDs on high-resistivity substrates.

Of great interest to astronomy community due to excellent IR response and better response than costly thinned backside illuminated devices.

Work has focussed so far on 200 x 200 pixel (15x15 μm^2 pixels) test device, 2Kx2K devices nearing completion in manufacture.

LBL MicroSystems Laboratory

The LBNL MicroSystems Laboratory is a Class 10 cleanroom specializing in the fabrication of radiation detectors on high-resistivity silicon wafers (4").

Using standard industrial fabrication equipment and processes, the lab provides tight process control as well as cleanliness levels required to achieve high yields while working with ultra-pure material.

Complete lithography line including photoresist, exposure (1:1 projection), develop.

High temperature processing including wet and dry oxidation, diffusion, chemical vapor deposition -- silicon dioxide, silicon nitride, and polysilicon.

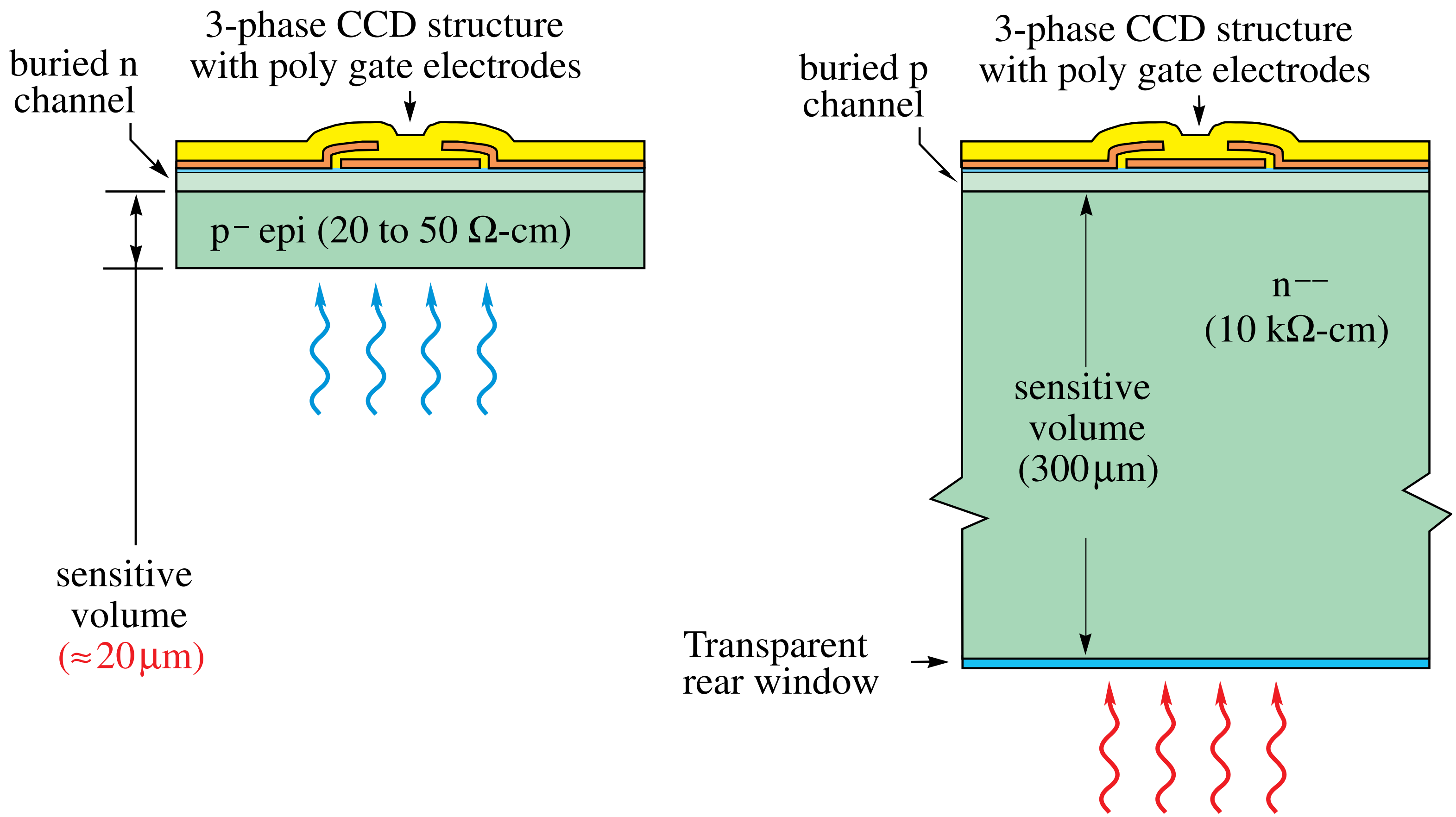
Thin film deposition of aluminum, indium-tin oxide, SiO_2, and titanium-tungsten alloy.

Wet etching of thin films in dedicated, temperature-controlled, filtered etch baths.

Dry etching of silicon dioxide.

i.e. Full MOS processing capabilities with ultra-cleanliness and purity.

Comparison of CCDs



Comparison of CCDs

Low resistivity CCDs:

Thin sensitive volume yields low S/N (20:1) limiting readout and radiation hardness.
Undepleted volume diminishes spatial accuracy and large charge diffusion.
Thinned CCDs on low resistivity silicon:
Requires complex and expensive thinning process.
Steward Observatory Process --

1) Mechanically lap wafers to >100 μm (difficult to handle)
2) Dice wafers
3) Flip chip bump bond to silicon substrate
4) Underflow epoxy between CCD and substrate
5) 1rst Acid etch
6) 2nd Acid etch
7) High pressure backside oxidation step (dark current)

Yields arbitrarily thin devices.
Commercial cost (SITe, EEV) for similar process $50-$100K per 2Kx2K device for astronomy.

Fully-Depleted High Resistivity CCDs:

Entire volume is sensitive. Requires depletion voltage.

For astronomy community has excellent IR sensitivity to 1000 nm.

Large sensitive volume yields high S/N (6000:1 for normal incidence) for tracks.

High-purity silicon likely better radiation hardness for both CTE and dark current.

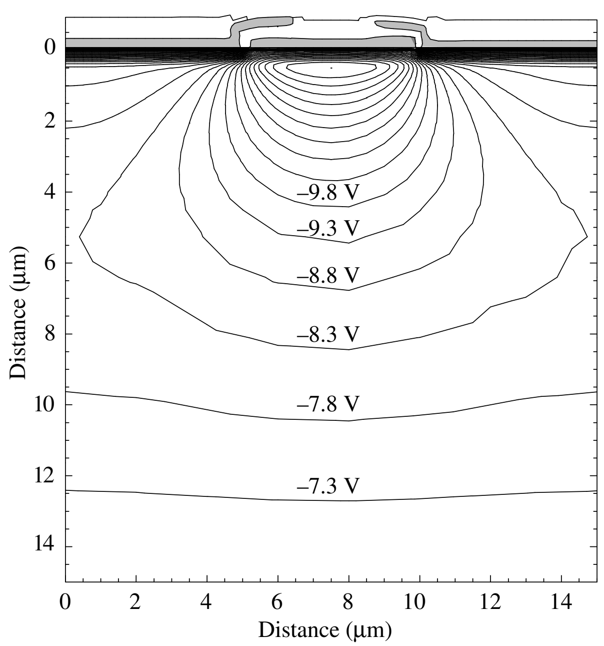
Large S/N leaves margin for radiation hardness, readout speed, high T operation.

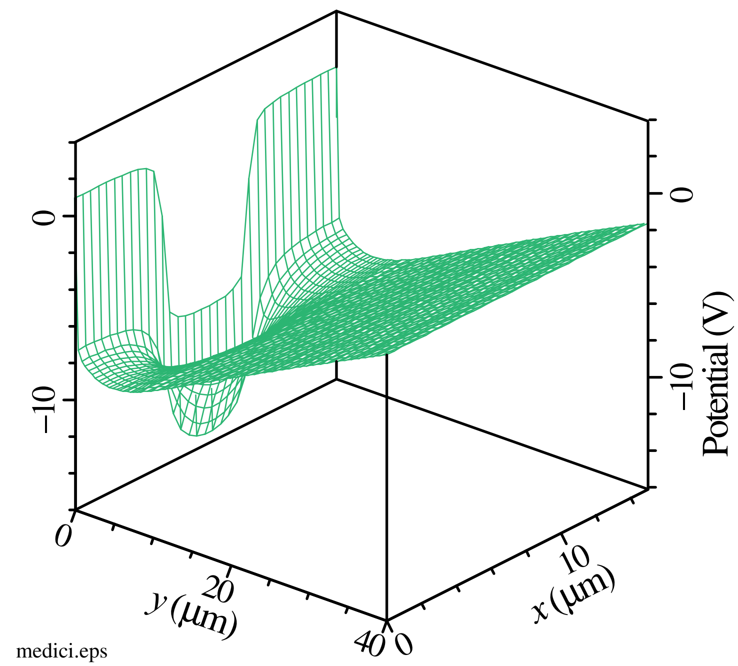
Multiple pixels hit for inclined tracks (in z only at NLC).

Can be thinned, but application of backside contact would limit to >100 μm (0.09 X).

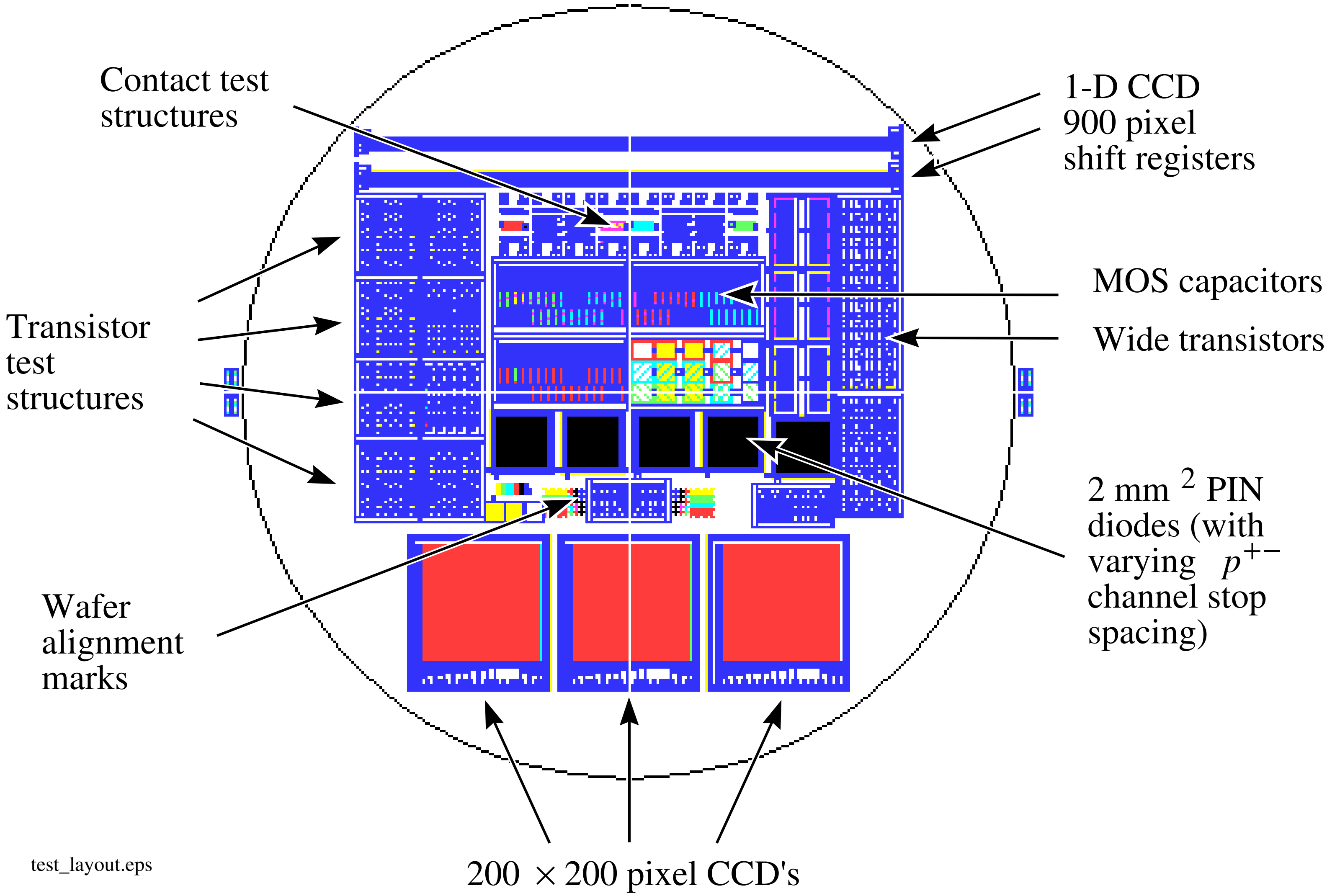
Cosmic Ray Image

Simulation of Buried-Channel on High Resistivity Substrate



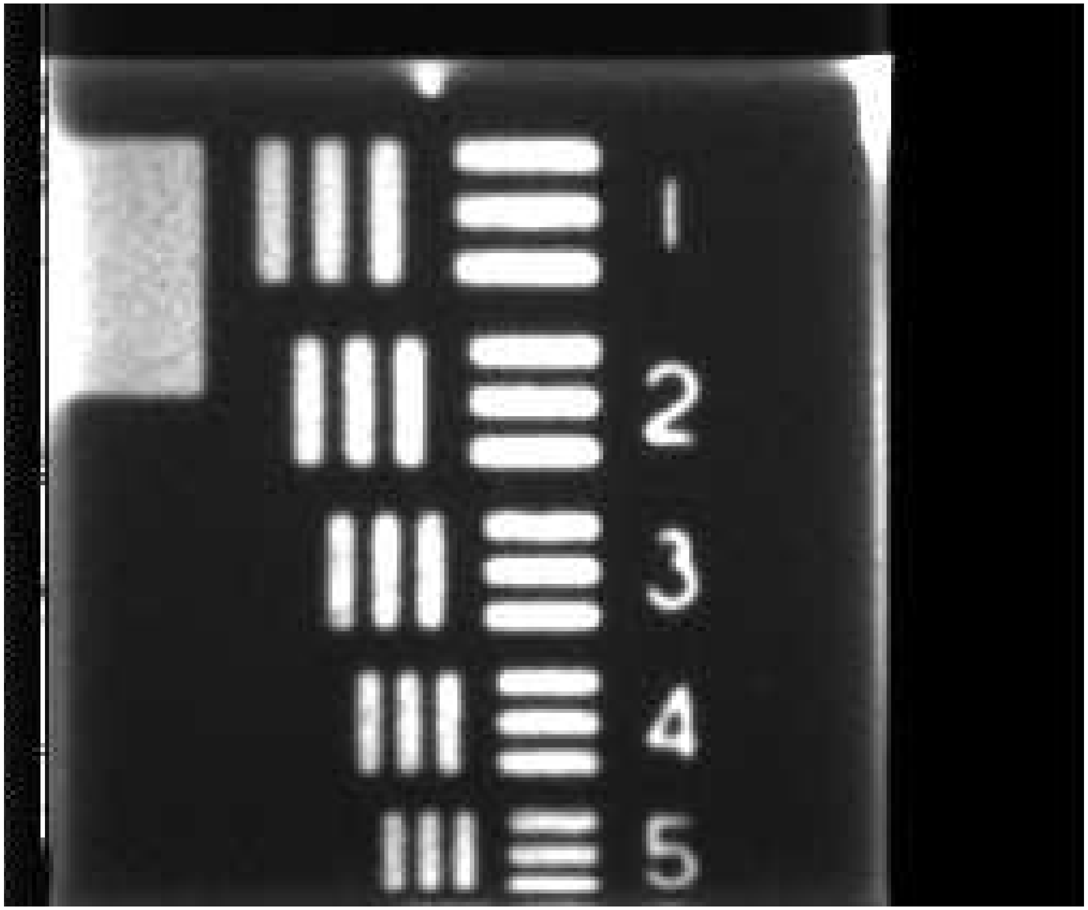


Prototype Test Chip



test_layout.eps

First Image with a back-illuminated n-type MOS CCD



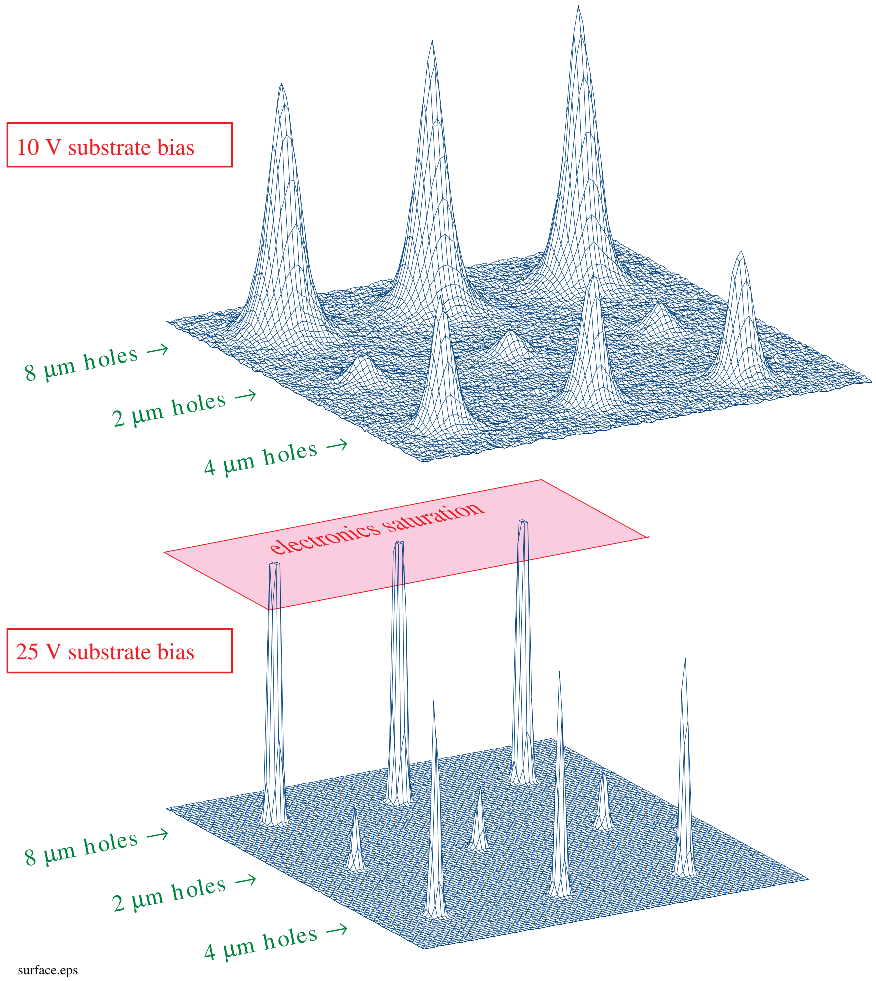
firstback_talk.ps

Back illumination (CCD at -120 C)

Photogenerated carriers must drift 300 μm to CCD potential wells

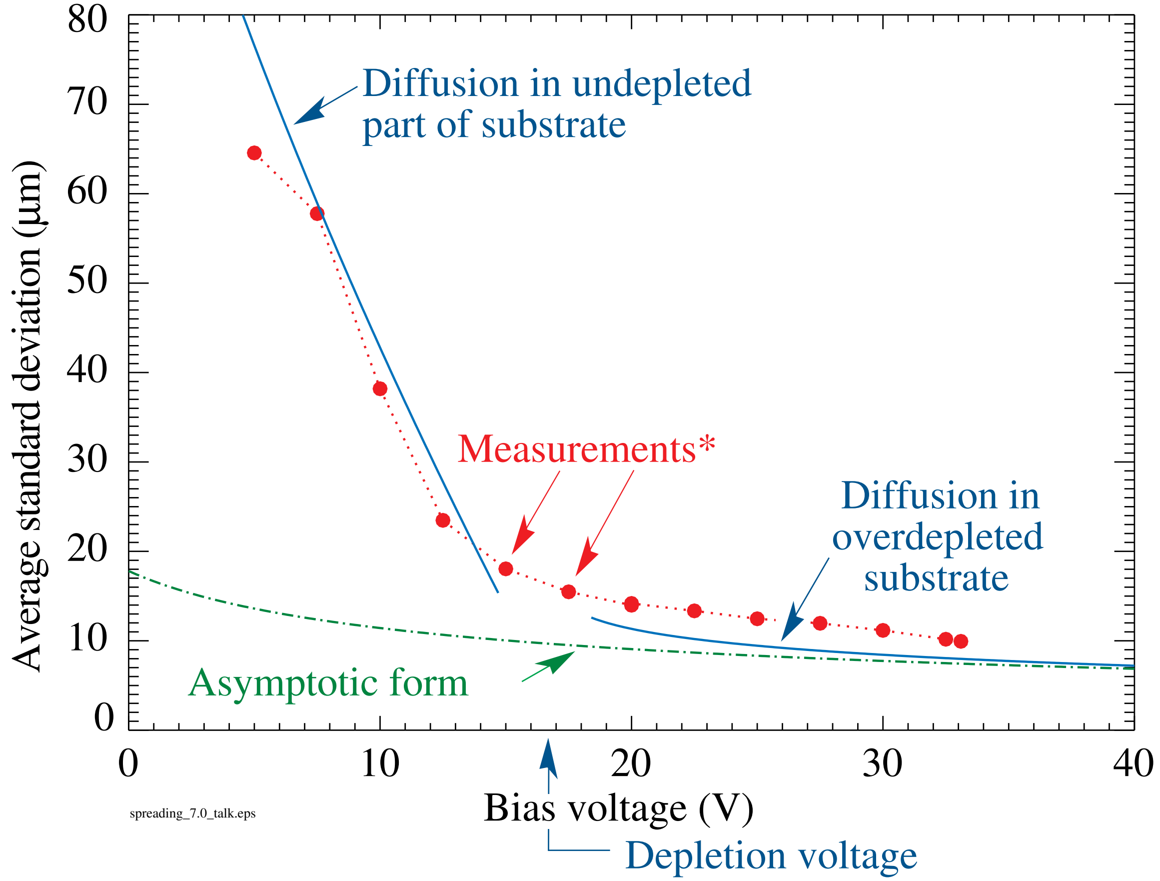
Study of Diffusion - Measurement

Charge spreading during transit of photogenerated holes from back of CCD to potential wells located 300 µm away.



Study of Diffusion - Prediction

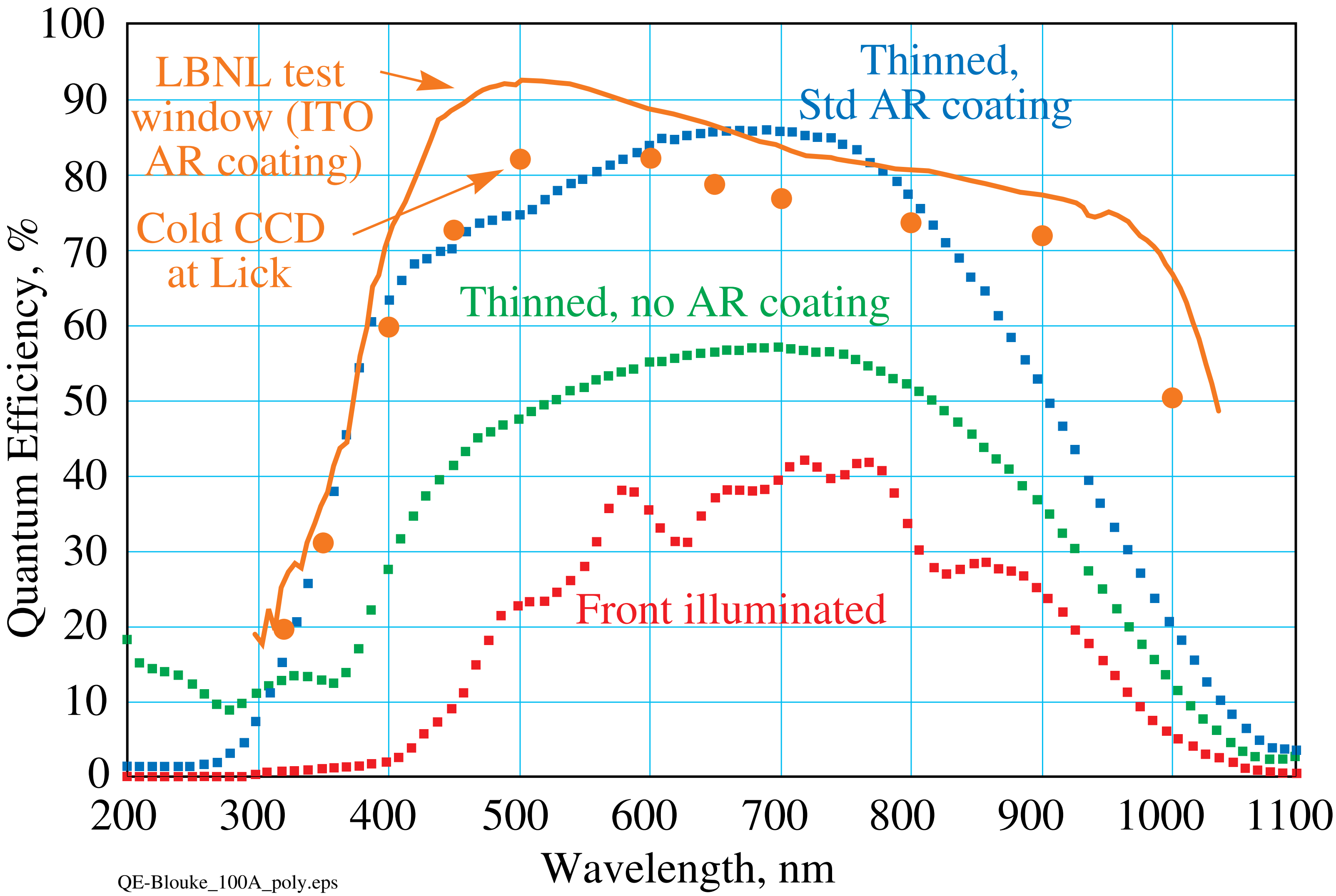
Model of charge spreading



*Results for $\sigma < 15$ µm are overestimated (at present) because of undersampling

Comparison of IR Response to Commercial CCDs

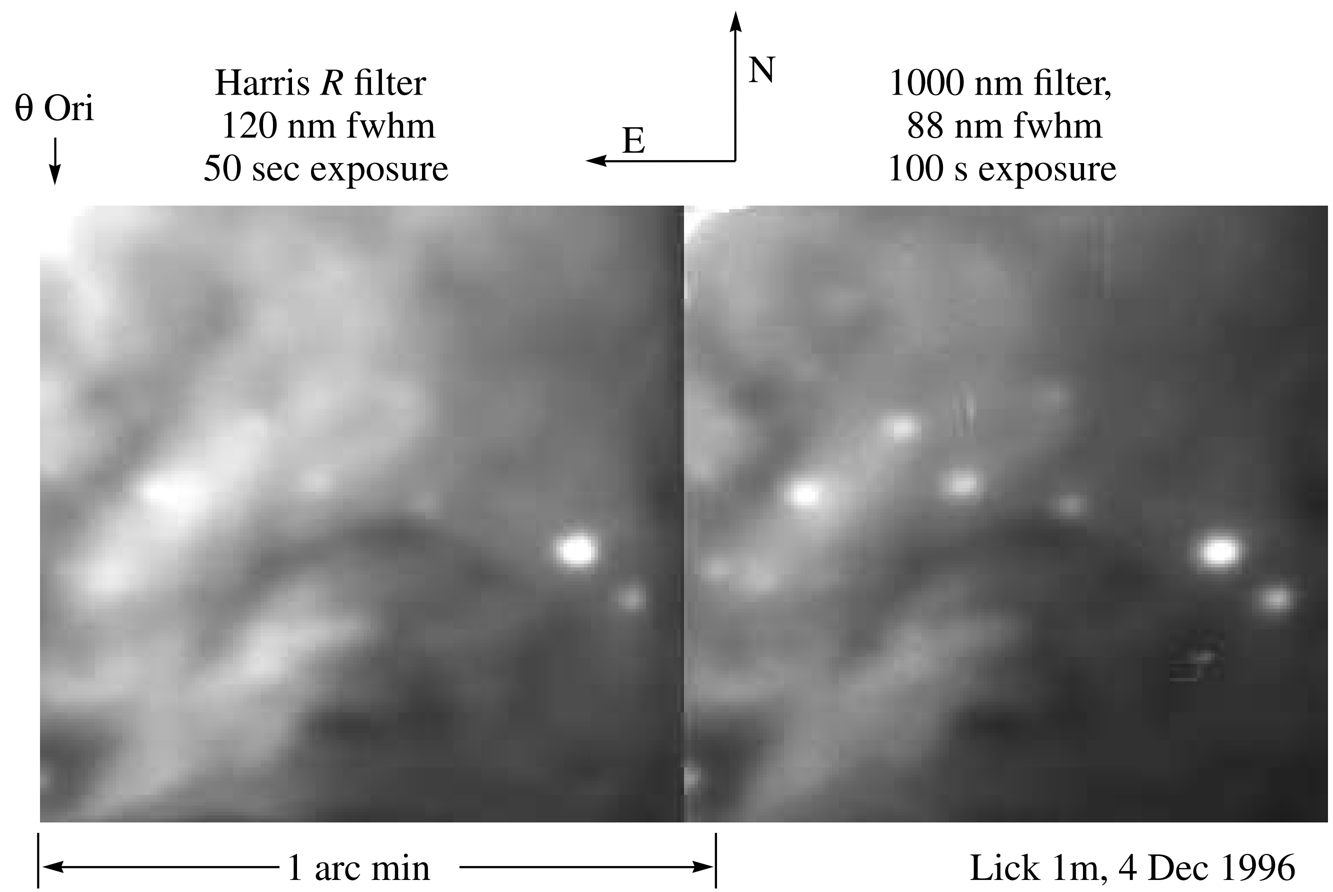
(All measurements warm unless noted otherwise.)



QE-Blouke_100A_poly.eps

First Astronomical Observation

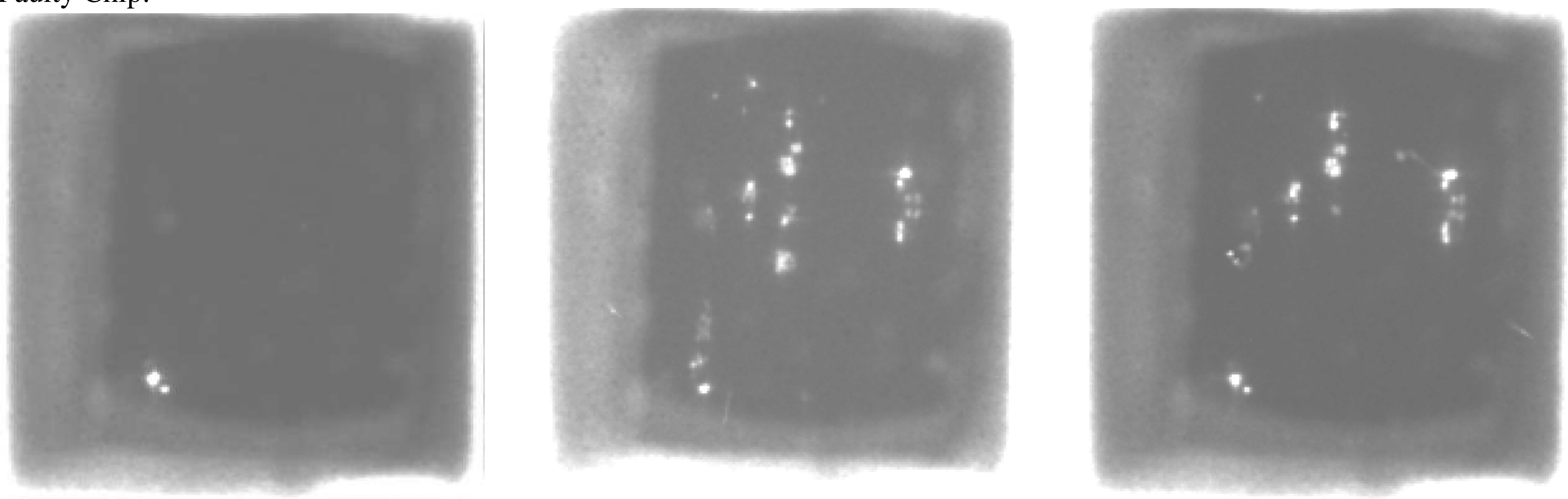
Test CCD image of obscured region in Orion Nebula under poor observing conditions at Lick Observatory. Left image 50 s exposure with filter peak transmission at 600 nm and FWHM of 120 nm. Right image 100 s exposure with filter peak transmission at 1000 nm and FWHM 88 nm.



OrionBarr_bw_cap.ps

Infrared Light from backside of 500 micron thick Faulty and Good chip compared using LBL CCD

Faulty Chip:



Good Chip:

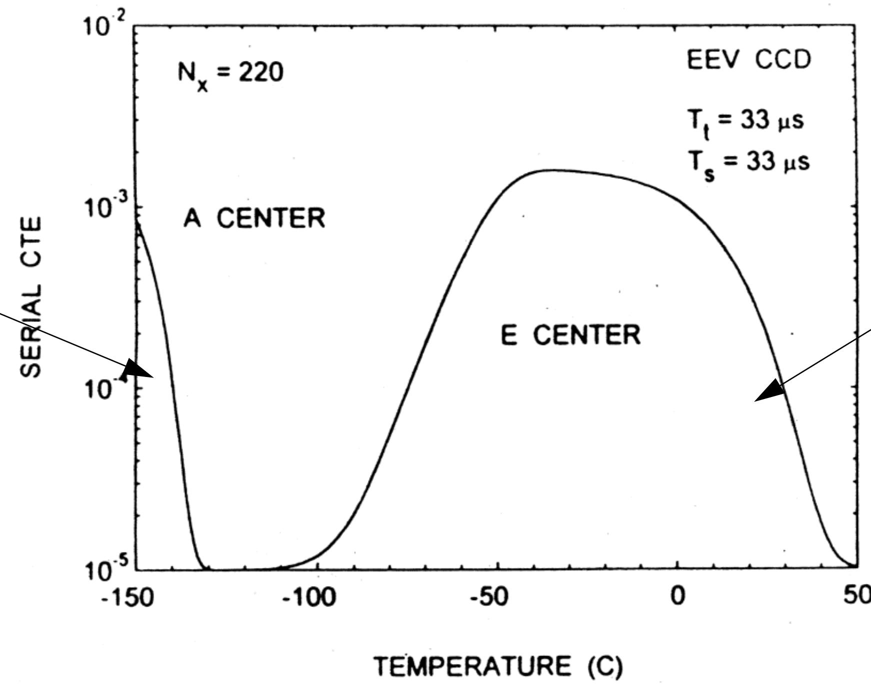
Fully-Depleted High-R CCD Performance

type	3 phase, FFT, buried channel, dual readout
# pixels	200 x 200 => (2K x 2K in fab.)
pixel size	15 μm x 15 μm
Serial CTE	0.999995 (pre-irradiation)
Width Parallel Channel	6 μm
Width Serial Channel	24 μm
Read Noise	4 - 6 e^-
Readout Rate	20 kHz
Temperature	150 K
Dark Current	0.005 e^-/s/pixel
Full Well	3 x 10^5
Output Amp	LDD PMOS Follower (1.3 μV/e^-)
Channel Doping	Boron Implant
Channel Phosphorus	10^{11} cm^{-3} => (vs. 10^{16} in typical CCD)*
Channel Oxygen	10^{15} cm^{-3} => (vs. 10^{17} in typical CCD)

*pn-CCD 10^{14} cm^{-3} [Strueder]

Radiation Hardness Study

Oxygen Centers (reduced 2 orders magnitude in our CCDs)



Phosphorus-Vacancy Centers (reduced 5 orders magnitude in our CCDs)

Figure 9 SRH simulation of the serial CTE loss in an EEV CCD assuming a 5×10^{10} cm^{-3} trap density for both the E and A centers. Each of these defects are commonly seen in irradiated Si.

C. Dale, *etal*, "Displacement Damage Effects...", IEEE Trans. Nucl. Sci., 40, no. 6, Dec. 1993, p 1628.

Radiation Hardness

Loss of Charge Transfer Efficiency (CTE) due to charge trapping centers created when non-ionizing collisions displace lattice atoms.

Relative Displacement damage for various particles and energies*

Particle	proton	proton	neutron	electron	electron
Energy	1 GeV	50 MeV	1 MeV	1 MeV	1 GeV
Relative Damage	1	2	2	0.01	0.1

* H. Spieler, "Introduction to Radiation-Resistant Semiconductor Devices and Circuits", May 1996, pp. 31. http://www-atlas.lbl.gov/strips/doc/tutorials.html.

Occupancy in innermost layer of Vertex Detector could be:
~5/mm^2/bunch train => 9x10^{11}/cm^2/yr => 5x10^{10}n/cm^2/yr equivalent.
[http://www-sldnt.slac.stanford.edu/nlc/Meetings/beamdelivery/1998-06-15-Maruyama/index.html slide 26]

Typical commercial CCDs are radiation-soft above fluences of ~1x10^9 n/cm^2.

"One possible "quantum leap" in this field may have occurred with the fabrication of the p-channel CCD where the absence of phosphorus in the buried channel will result in no P-V centres." [A. Holland, "CCDs for Future X-Ray Astronomy Missons", SPIE Vol. 3114.]

Radiation Hardness Study

Inefficiency from defects and charge trapping sites in buried channel is proportional to volume seen by transported charge. Some CCD designs the channel contains a “notch”, a narrow small diffusion implant that reduces the volume seen by the charge, but not implemented in the 200 x 200 test chip.

CTI is very difficult to measure in a small 200 x 200 pixel device (too few transfers for an accurate measurement).

Serial CTI (Charge Transfer Inefficiency 1-CTE) measured at UCO/Lick using white field illumination. One row is transferred into the CCD serial register and then the serial clocks are run to discard all of the image pixels except the last. This single pixel is then shifted back toward a region of interest. Next the serial clocks are run to shift the single pixel of charge back and forth over twenty pixels in the serial register many times, then readout. The next row is readout in normal serial-clocking fashion for calibration. The sequence is repeated 100 times until the entire CCD is read out.

Radiation Hardness Study

Pre-irradiation Serial CTI of 5x 10^{-6}.

The 200 x 200 test CCD was then taken to the LBNL 88" 55 MeV Proton Cyclotron and irradiated with 5×10^{8} p/cm^{2}.

Post-irradiation Serial CTI of 7×10^{-6}.

Change in Serial CTI was 2×10^{-6}.

Charge intensity levels for the CTI measurements were 1800 e^{-}'s.

The Parallel CTI is expected to track the Serial CTI by the ratio of register volumes,
6 µm wide parallel registers, 24 µm wide serial register, i.e. 1/4.

CCDs unpowered during irradiation.

Pixel readout rate was 20 kHz during all measurements.

Serial CTI needs to be < 1 x 10^{-4} (see table). Expect radiation tolerance up to equivalent fluence of 2.5 x 10^{10} n/cm^2 given measured post-irradiation CTI.

Expect Parallel CTI to reach 1 x 10^{-4} at fluences of 1 x 10^{11} n/cm^2.

Using a “notch” in the buried channel to reduce volume, both Parallel and Serial CTI could reach 1 x 10^{-4} at fluences of 3×10^{11} n/cm^2.

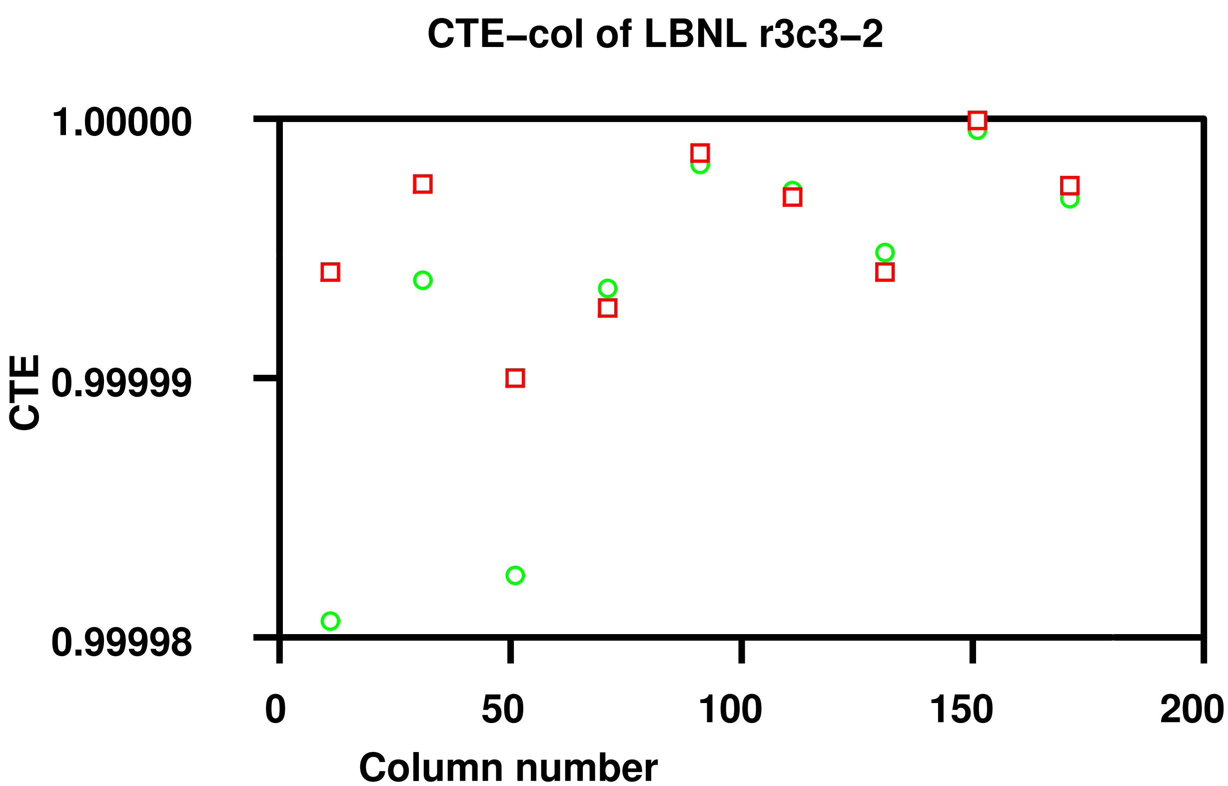
CTI depends on creation of charge trap sites during irradiation. These sites fill as charge passes over, thus CTI is intensity dependent.

24,000 electrons deposited in 300 μm silicon so CTI at high signal values is proportionately smaller than measured, thus, fluences above 10^{12} n/cm^2 may be possible.

Charge Collected vs. CTI

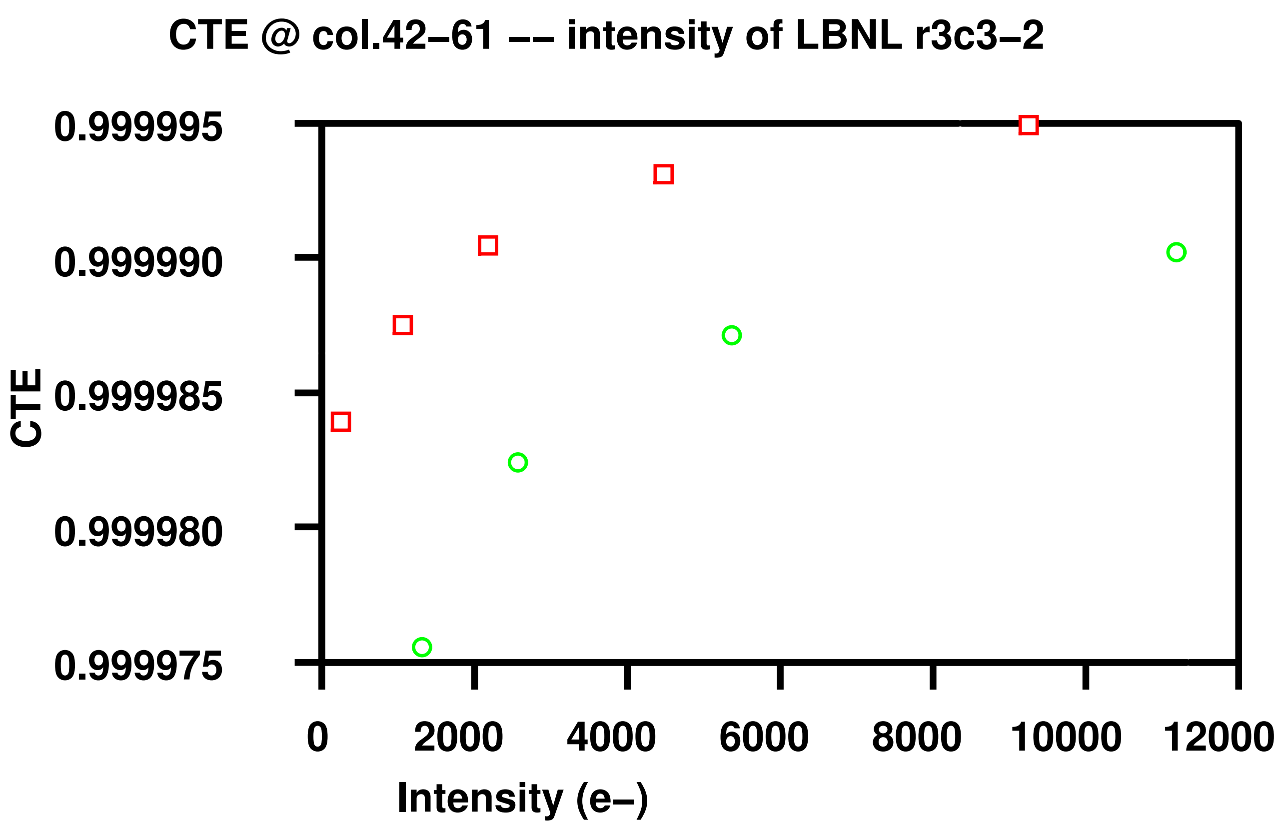
CTI	Charge Collected after 1K Transfers	Charge Collected after 2K Transfers
1 x 10^{-6}	0.999	0.998
1 x 10^{-5}	0.99	0.98
1 x 10^{-4}	0.90	0.82
1 x 10^{-3}	0.36	0.14

Serial CTE



squares: before radiation test
circles: after radiation test

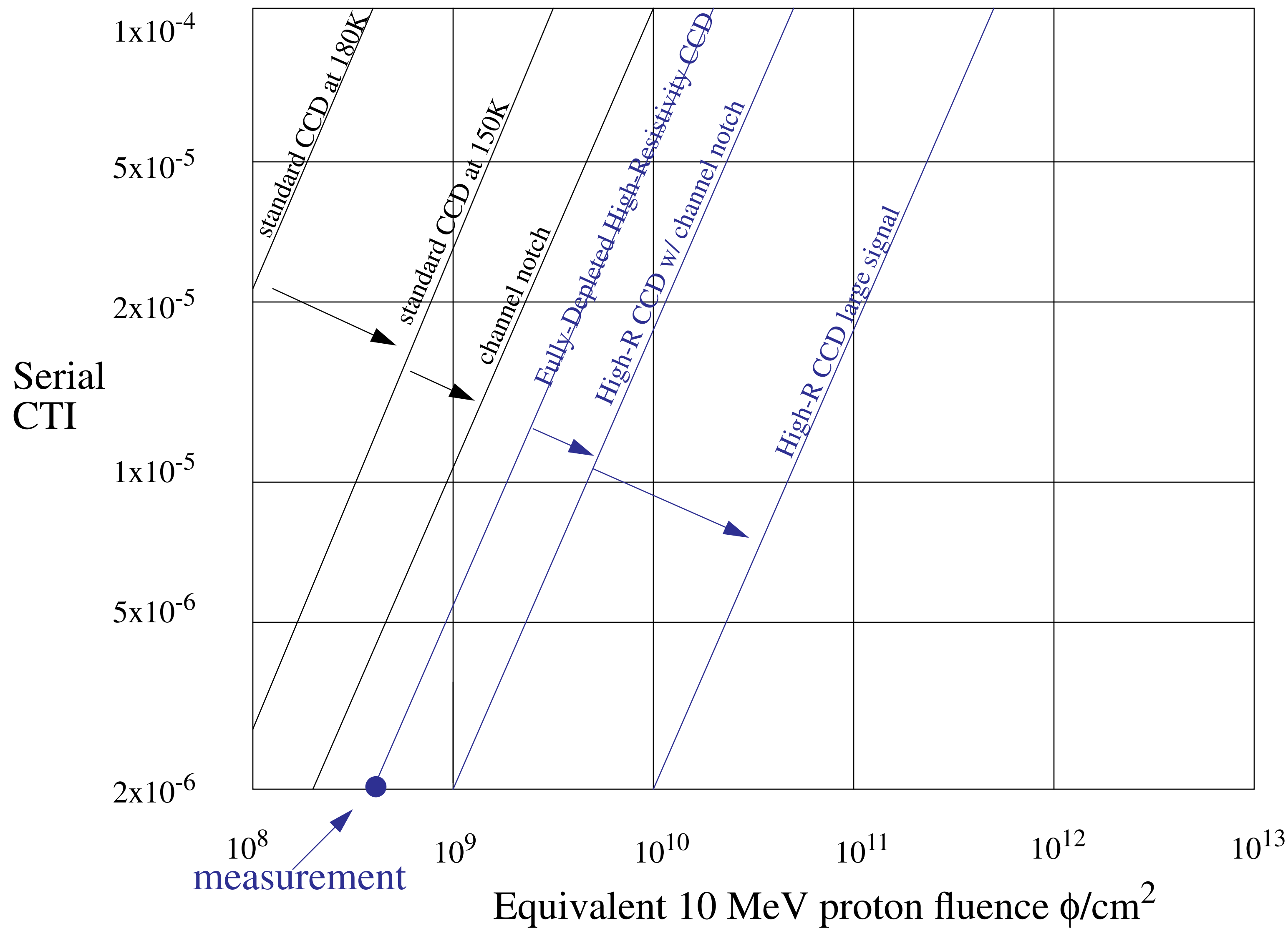
CTE vs. Intensity



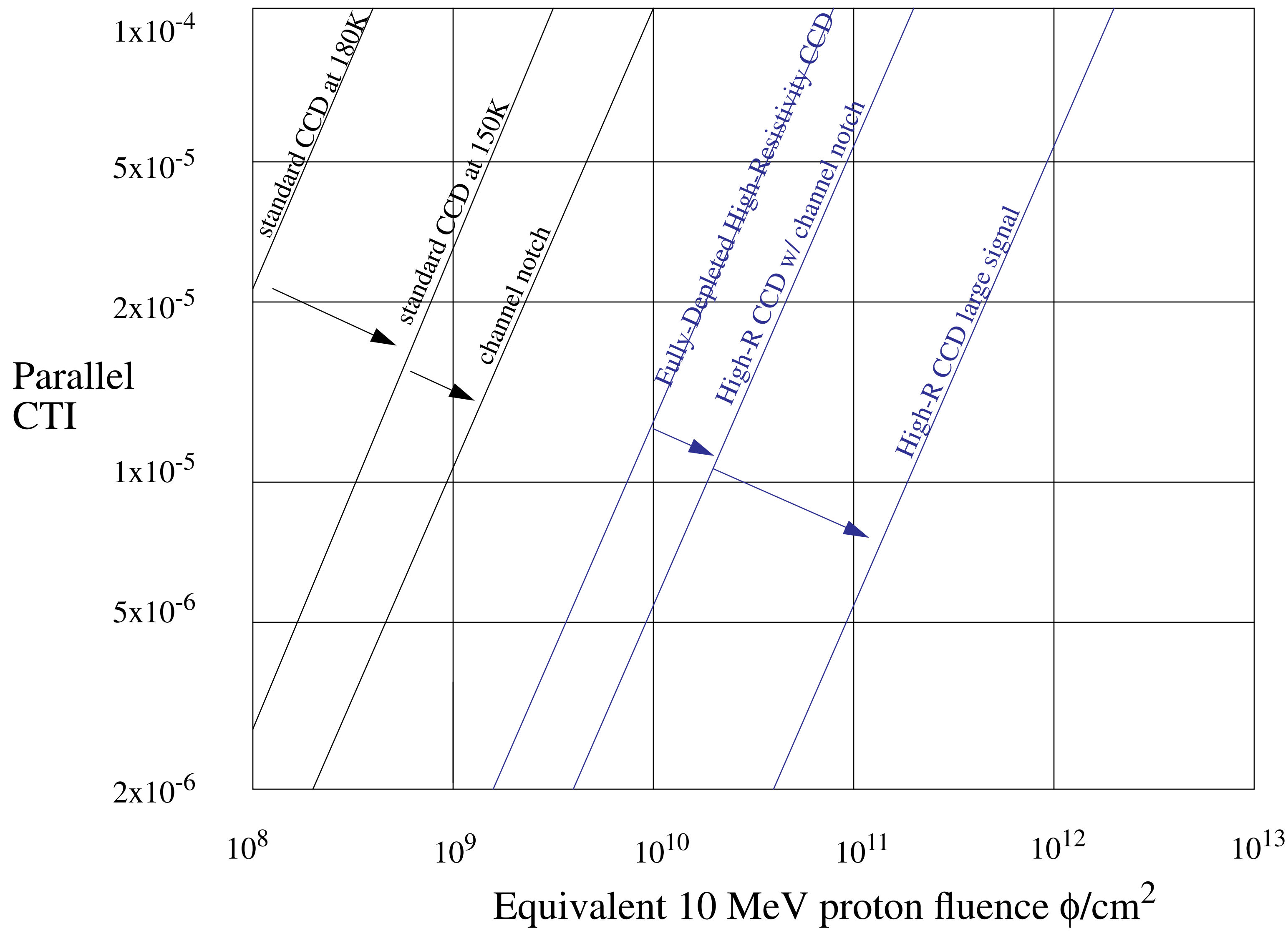
squares: before radiation test

circle: after radiation test

Equivalent 10 -MeV proton damage ϕ/cm^2 [A. Holland, etal, “Techniques for Minimizing Space Proton Damage in Scientific Charged Coupled Devices”, IEEE Trans. Nucl. Sci. Vol 38, No. 6, Dec. 1991, p. 1663]



Assume that Serial CTI and Parallel CTI are related by ratio of of volumes (4:1)



Next Step

New wafer currently in final stages of processing (7 of 10 mask steps completed).

This new wafer has devices ranging from 200x200, 512x512, 690x400, 1100x800, 1980x800, and 2048x2048.

The range of devices will allow us to study issues of dark current including inverted mode operation as the size of the device increases.

Variations in readout transistor to study noise minimization.

Pinning and guard ring strategies.

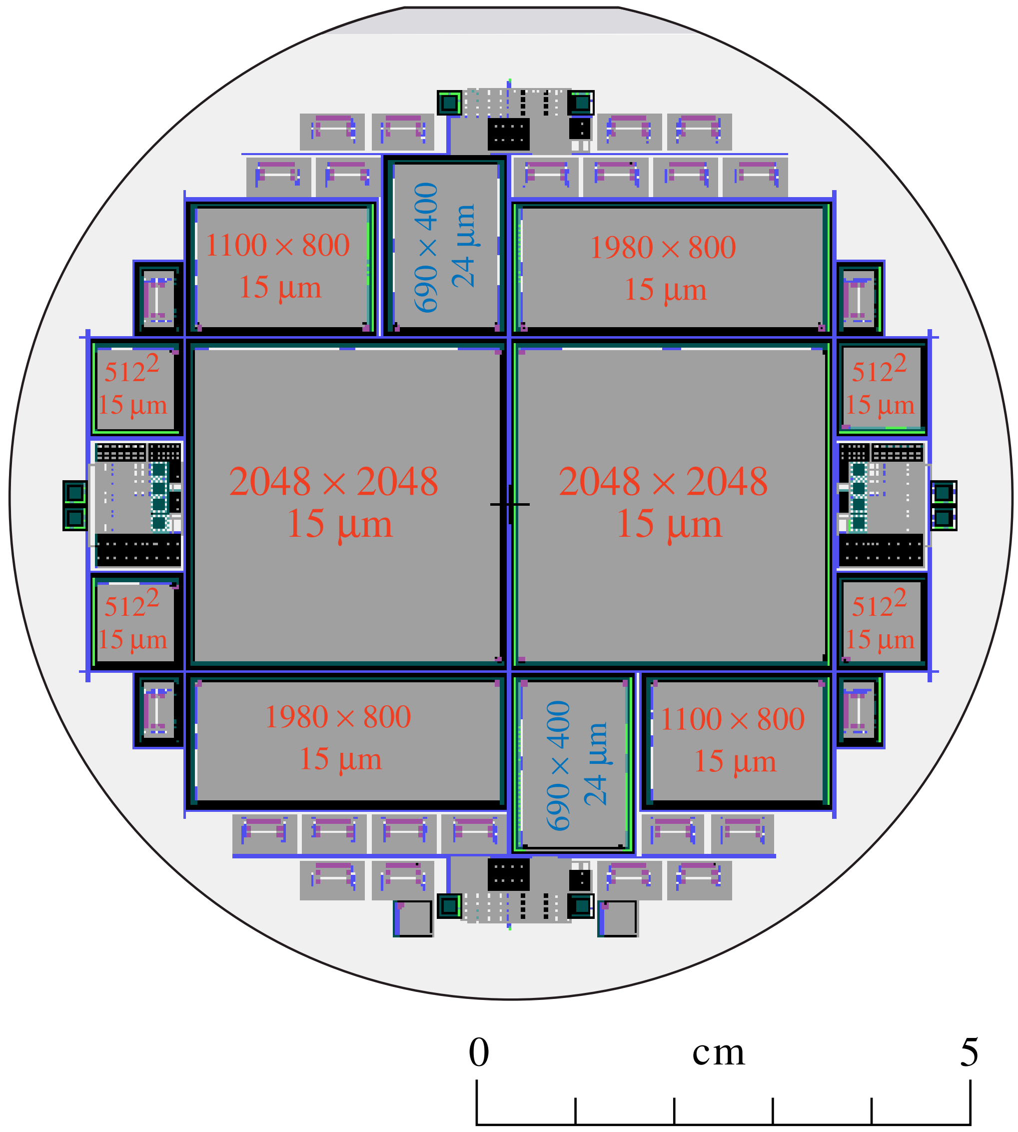
Two layer AR coatings for astronomy should achieve 90% Q.E. at 1000 nm (warm).

Channel “notch” in serial register implemented to improve serial CTE.

The larger devices will facilitate the measurement of parallel CTE and could be the subject of further radiation hardness studies.

Also have low-resisitivity wafers of same design to compare radiation tolerance, general performance.

New Wafer



1100 × 800
15 μm
690 × 400
24 μm
1980 × 800
15 μm
512²
15 μm
512²
15 μm
2048 × 2048
15 μm
2048 × 2048
15 μm
512²
15 μm
512²
15 μm
512²
15 μm
512²
15 μm
1980 × 800
15 μm
690 × 400
24 μm
1100 × 800
15 μm
0
cm
5

Next Step (cont...)

After this run:

Implementation of MPP (Multi-phase pinning)? This will permit room termperature operation of the device with low dark current.

Higher speed readout (amplifier, quad+ readout).

Commercialization of process already underway for P-I-N photodiodes on n-type high-resistivity silicon.

Intend to commercialize the manufacture of n-type fully-depleted CCDs to our specifications. Already in negotiation with two commercial foundries. Furthermore, in negotiation with OEM of fault defect microscopes for the silicon industry (photon emission microscopy). This would create a large market for the devices (larger than astronomy) improving manufacturing promise.

Evaluate manufacturing limitations for thinner devices and application of backside contact.

Conclusion

Fully depleted high-resistivity CCD on n-type silicon has been developed.

No fully-depleted MOS CCD has previously been manufactured or considered possible.

Fully active sensing volume provides excellent IR response (50% at 1000 nm achieved, 90% expected with optimized AR coating).

Large S/N and high-purity silicon provides radiation resistance for particle detectors.

Demonstrated Serial CTI degradation of only 2×10^{-6} at equivalent neutron fluences of 5×10^{8} n/cm^2. Literature indicates commercial CCDs 10-100 times worse. Fluence tolerance above 10^{12} n/cm^2 may be possible.

New wafer will push past current 200x200 pixel device to 2Kx2K.

Inexpensive MOS processing.

Commercialization of process in progress.

Strong collaboration with UCO/Lick Observatories.