# Manufacture and Metrology of 300 mm Silicon Wafers with Ultra-Low Thickness Variation

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**Abstract.** With the evolution of exposure tools for optical lithography towards larger numerical apertures, the semiconductor industry expects continued demand for improved wafer flatness at the exposure site. The allowable site flatness for 300 mm wafers is expected to be less than 45 nm by 2010 and it may be as low as 25 nm by 2015 according to the International Technology Roadmap for Semiconductors (ITRS 2006). This requires wafers with low thickness variation and presents a challenge for both wafer polishing and metrology tools, which must be capable of meeting the specifications. We report the results of fabricating 300 mm silicon wafers with very low thickness variation using magnetorheological finishing (MRF), a deterministic subaperture finishing process. The wafer thickness metrology, which guided the finishing process, was provided by an infrared interferometer developed at the National Institute of Standards and Technology (NIST). The finishing method in combination with the interferometric wafer metrology enabled the fabrication of 300 mm silicon wafers with a *total* thickness variation (TTV) of about 40 nm, and between 10 nm and 15 nm thickness variation at 25 mm  $\times$  25 mm exposure sites.

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## **1. INTRODUCTION**

The pursuit of ever decreasing feature sizes in integrated circuit (IC) manufacturing has, in recent years, required the development and deployment of exposure tools which operate at wavelengths as short as 193 nm (DUV) and use increasingly large numerical apertures. Both trends have led to a reduction of the depth of focus and require improved wafer flatness to limit the contribution of the wafer flatness error to the error budget at the exposure site. The International Technology Roadmap for Semiconductors (ITRS) [1] forecasts that the flatness at the exposure site for 300 mm diameter wafers, which is often characterized by the site total indicator range after subtraction of a best fit plane (called SFQR) over a  $26 \,\mathrm{mm} \times 8 \,\mathrm{mm}$  site, will have to decrease from 80 nm in 2005 to at least 32 nm by 2013, and to about 14 nm by 2020. In addition, the economic pressure to increase the number of dies per wafer will compel the reduction of the edge exclusion from 3 mm to 1.5 mm. These requirements are likely to exceed the capabilities of existing finishing processes, which typically consist of a combination of single and double-sided chemomechanical full aperture polishing processes [2], as well as current industry standard wafer thickness metrology approaches. If we take technology trends from the optics industry as indicators, sub-aperture polishing processes will be required to meet future specifications for wafer flatness. Along with these, metrology is needed not only for quality control purposes, but also to guide the sub-aperture polishing approaches. This paper reports on a collaboration between the National Institute of Standards and Technology (NIST) and QED Technologies, in which a wafer thickness metrology with a standard measurement uncertainty of about 5 nm, using infrared interferometry, was combined with a sub-aperture polishing process known as Magnetorheological Finishing<sup>‡</sup> (MRF). We demonstrated that 300 mm wafers could be finished to a *total* thickness variation of about 40 nm.

#### 2. WAFER THICKNESS METROLOGY

In a wafer exposure tool, the wafer is held on a wafer chuck. The wafer flatness at the exposure site is determined by the chuck flatness, the thickness variation of the wafer, and any additional flatness error introduced by the chuck-wafer interaction. It is desirable to reduce the thickness variation of the wafer to limit the flatness error at the exposure site. Sub-aperture polishing techniques require an accurate measurement of the thickness variation with high spatial resolution to guide the polishing process. When a residual flatness variation of only a few tens of nm is desired, a form of optical interferometry seems best suited to provide the necessary metrology. For the project described here, an infrared interferometer operating at 1552 nm was used for the wafer thickness variation measurements. Silicon with sufficiently low dopant concentrations is transparent to light at wavelengths larger than 1100 nm [3, 4]. At infrared wavelengths, the thickness variation of silicon wafers, or wafers made from other infrared optical materials, can be characterized using well established optical interferometry methods, which achieve low measurement uncertainties.

NIST's Improved Infrared Interferometer ( $IR^3$ ) is a phase-shifting interferometer [5] operating at the optical communication C-band wavelength of 1552 nm. Precursors to the current instrument have been described by Parks et al.[6] and Schmitz et al.[7]. IR<sup>3</sup> was initially designed and built by Optical Perspectives Group<sup>‡</sup>[8]. Subsequently, the interferometer was modified at NIST to use polarization sensitive optics. Fig. 1 shows a solid model of the interferometer. Light from a tunable external cavity diode laser, operating at 1552 nm, is delivered to the interferometer by way of a polarizationmaintaining fiber. The plane of polarization is inclined by 45° with respect to the base plate of the interferometer. After collimation by a lens (CL) a polarizing beam splitter (BS) creates two beams with orthogonal polarizations, one traveling to the diverger lens (DL), the other to the reference mirror (RM) for the Twyman-Green configuration. Both beams are circularly polarized by precision  $\lambda/4$ -plates (LP). For measurements of 300 mm wafers, the test beam, which is about 10 mm in diameter after passing through the beam splitter, must be expanded. This is accomplished with an f/3 diverger objective (DL) and the large collimator lens shown in Fig. 2. The test beam emerging from the collimator lens has a diameter of about 325 mm. The interferometer can be used either as a Twyman-Green interferometer [9] with a separate reference arm and reference mirror, or as a Fizeau interferometer. When measurements in the Fizeau mode are made, the reference mirror (RM) is blocked by a shutter. The return beams from the test and reference surfaces are reflected by the beam splitter into the imaging arm of the interferometer. A zoom lens system (ZL) images the wafer under test onto the camera (CA). Commercial phase-shifting software is used to make phase measurements either by shifting the wavelength of the laser, or by electro-mechanical movement of the reference mirror (RM). The polarization optics of the interferometer prevent unwanted coherent reflections from reaching the camera and thus suppress "ghost fringes", which increase the measurement uncertainty.

For measurements of the wafer thickness variation of double-sided polished wafers, the Fizeau configuration of IR<sup>3</sup> is suited best, because one of the wafer sides can serve as the reference surface while the other side serves as the test surface. The desired thickness variation information is thus measured directly. The test beam was



**FIGURE 1.** Solid model of NIST's improved infrared interferometer (IR<sup>3</sup>). The main components of the interferometer are indicated: collimator lens (CL), polarizing beam splitter (BS),  $\lambda/4$ -plates (LP), reference mirror for the Twyman-Green mode (RM), diverger lens (DL), polarizer (PO), zoom lens (ZL), motion controllers for the zoom lens (MC), and camera (CA). The size of the base plate is approximately 20 cm × 30 cm.

expanded to about 325 mm diameter by the collimator lens shown in Fig. 2, which enables the measurement of the thickness variation of a 300 mm wafer in one measurement with a spatial resolution of about 0.7 mm. The wafer is inserted into the test beam of the interferometer and becomes the Fizeau cavity of the interferometer. Reflected light from both wafer surfaces returns to the interferometer's camera where interferograms are measured. Phase shifting interferometry is realized by varying the laser wavelength. The resulting height maps directly represent the optical thickness variation of the test wafer. The desired physical thickness variation of the wafer is obtained, when the optical thickness variation is divided by two times the refractive index of the wafer material. We rely on tabulated data for the refractive index of silicon reported by Primak [10] and Villa [11], and assume that index variations across the wafer can be neglected. The Fizeau configuration has many advantages for thickness variation measurements. The interferometer cavity is the wafer, a solid, which is unaffected by vibration, and turbulence is absent. In addition, the coherence length of the laser source can be reduced because the distance between the wafer surfaces is small. This eliminates coherent reflections from optical surfaces in the interferometer which otherwise lead to measurement errors. In Fizeau mode, the root-mean-square (rms) of differences between several measurements has an average over all pixels of about 3 nm rms.

An important limitation of IR<sup>3</sup> for wafer thickness variation measurements must be mentioned. Wafers with higher doping levels are not transparent at 1552 nm and a different thickness variation metrology is required to prepare such wafers for sub-aperture finishing. During the



**FIGURE 2.** Test arm of the  $IR^3$  interferometer. Shown are the collimator lens of the beam expander together with a 300 mm silicon wafer. The insensitivity of the measurement to vibration permits the use of a simple wafer mount.

project described here, we examined P- and P++ wafers. P-type wafers are doped with boron, which creates positive charge carriers in the wafers. The lightly doped Pwafers could be measured with IR<sup>3</sup>. However, the heavily doped P++ wafers did not transmit enough light at 1552 nm for the interferometer to work.

# 3. MAGNETORHEOLOGICAL WAFER FINISHING

Magnetorheological Finishing<sup>‡</sup>(MRF) is a precision polishing method developed to overcome some of the fundamental limitations of traditional finishing. A summary and comparison of the relative merits of different finishing processes was recently given by Evans et al.[12]. We will give a brief summary of the magnetorheological finishing process here. MRF is a finishing process, intended for removing micrometer or sub-micrometer material thickness, which is usually employed near the end of the process chain required for the fabrication of precision surfaces. It is a *deterministic* finishing process that has been shown to produce optical surfaces with an accuracy better than 30 nm peak-to-valley (PV) and surface micro-roughness less than 1 nm rms on optical glasses, single crystals such as calcium fluoride and silicon, and glass-ceramics such as Zerodur [13, 14]. MRF is a computer-controlled sub-aperture polishing process, which is based on a magnetorheological fluid containing an abrasive whose viscosity increases in the presence of a magnetic field (see Fig. 3). The viscosity of the magnetorheological fluid can be controlled with the strength of the magnetic field. This creates a stable and conformable polishing tool. Since the tool is fluid-based,



FIGURE 3. Setup for magnetorheological finishing.

it conforms to any surface shape and eliminates the need for dedicated tooling. The stable, sub-aperture nature of the MRF process enables high-precision figure correction. The shear-mode of removal enables the MRF process to improve micro-roughness, remove sub-surface damage, and reduce residual stress [15, 16], which is typically introduced in previous manufacturing steps. The forces acting on the surface during MRF polishing are predominantly tangential. The normal forces on the individual abrasive particles are comparatively small hydrostatic forces. This is in contrast to conventional polishing techniques where a bound or loose abrasive is forced into the surface through the action of a lap [12]. Here normal forces can dominate, creating scratches, sub-surface damage, and stress.

It is common for the finished silicon wafer to exhibit "nanotopography", which originates with the initial sawing of the silicon crystal into wafers [17]. Nanotopography of a wafer surface is the flatness error of the surface with spatial wavelengths shorter than 20 mm. The removal of nanotopography poses a significant technical challenge in the chemo-mechanical polishing (CMP) processes used by wafer fabricators worldwide to finish silicon wafers [18]. The localized nature of a subaperture polishing process like MRF is well suited to reducing the nanotopography, which results in improved site flatness.

The thickness variation of a set of 300 mm silicon wafers was first measured with IR<sup>3</sup> at NIST. IR<sup>3</sup> measures the optical thickness variation of a wafer. To obtain the physical wafer thickness variation the optical thickness variation was divided by two times the refractive index of silicon at 1552 nm, which is 3.48 [10, 11]. The thickness variation of two wafers, here labeled A and B, which were finished with a conventional chemomechanical polishing process, before sub-aperture polishing is shown on the left sides of Fig. 5 and Fig. 6.



FIGURE 4. Polishing of a 300 mm silicon wafer.

The wafers were then delivered to QED Technologies for magnetorheological polishing to reduce the thickness variation measured with IR<sup>3</sup>. One of the advantages of MRF is its insensitivity to up to a few tens of micrometers of part distortion on the mount during polishing because this does not perceptibly change the forces at the polishing spot [14]. Hence, a pin-chuck was not required to hold the part. A circular base with vacuum channels cut into the flat surface held the part during polishing. The flatness error of the vacuum chuck was approximately  $5\,\mu$ m. All polishing was performed with a standard MRF polishing machine (Fig. 3), diamond-based fluid, a 150 mm diameter wheel, and vacuum fixturing (Fig. 4). The polishing spot used during the polishing cycles had lateral dimensions from 4.5 mm to 6.5 mm in the short direction and from 9 mm to 13 mm in the long direction. Volumetric removal rates between 0.2 mm<sup>3</sup>/min and 0.6 mm<sup>3</sup>/min were achieved, depending on the process conditions. It was typically necessary to remove about 300 nm of material thickness to achieve the best possible thickness variation. At the current material removal rate, this led to polishing cycle times as low as 40 min.

#### 4. RESULTS

Total thickness variation (TTV) was improved from 449 nm to 95 nm for wafer A shown in Fig. 5. This improvement in the TTV was achieved over a circular area with 297 mm diameter. The thickness variation for a second wafer before and after MRF polishing is shown in Fig. 6. In Fig. 6 the edge exclusion is 4 mm instead of 1.5 mm for Fig. 5. The thickness variations for both polished wafers can be seen side-by-side in Fig. 7, which shows that the thickness variation for both MRF finished wafers is similar and the difference in TTV after polish



**FIGURE 5.** Wafer thickness variation of wafer A before and after sub-aperture polishing. TTV was reduced from 449 nm to 95 nm over 297 mm aperture (1.5 mm edge exclusion).

ing in Fig. 5 and Fig. 6 is primarily due to the larger edge exclusion in Fig. 6.

For IC manufacturers, the TTV of a wafer is of less interest than the flatness at the exposure site. In Fig. 8, Fig. 9, and Fig. 10 we show the component of the site flatness SFQR (local peak-to-valley flatness error after subtraction of a best-fit plane) which results from the site thickness variation of wafers A and B for a tiling with 25 mm  $\times$  25 mm sites. Fig. 8 shows the site flatness of wafer A before MRF finishing resulting from the thickness variation of the wafer alone. The site flatness of the same wafer after MRF finishing is shown in Fig. 9. After finishing, the site flatness is much more uniform and, overall, is improved by about a factor of two. Fig. 10 shows the site flatness for wafer B. For both finished wafers, most sites have a site flatness between 10 nm and 20 nm, which meets the site flatness specifications until the end of the next decade. Exceptions occur at the center of the wafers where the site flatness is approximately 35 nm, and, as Fig. 9 shows, at the edge of the wafer. In the case of wafer A, the site flatness errors appear more prominent (Fig. 9), because less of the edge data were excluded than for wafer B (Fig. 10). We expect that the site flatness at the wafer center and at the edge can be improved by careful optimization of the polishing process.

## 5. CONCLUSION

We have demonstrated that sub-aperture finishing of silicon wafers with the MRF process, which was guided by thickness variation measurements prior to polishing, can address the wafer flatness requirements of many future ITRS technology nodes. It currently appears unlikely that conventional single- or double-sided polishing processes will be able to achieve comparable site flatness toler-



**FIGURE 6.** Wafer thickness variation of wafer B before and after sub-aperture polishing. TTV was reduced from 238 nm to 42 nm over 292 mm aperture (4 mm edge exclusion).



**FIGURE 7.** Residual thickness variation of wafers A and B after sub-aperture polishing. Both wafers are shown over 292 mm aperture (4 mm edge exclusion).



**FIGURE 8.** SFQR of wafer A *before* sub-aperture finishing for  $25 \text{ mm} \times 25 \text{ mm}$  sites with the same edge exclusion (1.5 mm) as in Fig. 5. 53 sites have a SFQR below 25 nm.



**FIGURE 9.** SFQR of wafer A *after* sub-aperture finishing for  $25 \text{ mm} \times 25 \text{ mm}$  sites with the same edge exclusion (1.5 mm) as in Fig. 5. 92 sites have a SFQR below 25 nm.



**FIGURE 10.** SFQR of wafer B after sub-aperture finishing for  $25 \text{ mm} \times 25 \text{ mm}$  sites with the same edge exclusion (4 mm) as in Fig. 6.

ances. Although the technologies described in this paper demonstrate a technical path to meeting the site flatness requirements of the ITRS, a significant challenge remains in creating a cost-effective, commercially viable process. This will require not only further development of the polishing process, especially to improve the polishing near the wafer edge and a reduction in cycle times, but specific integration activities with wafer manufacturers to determine where to insert sub-aperture polishing in the wafer manufacturing process chain.

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