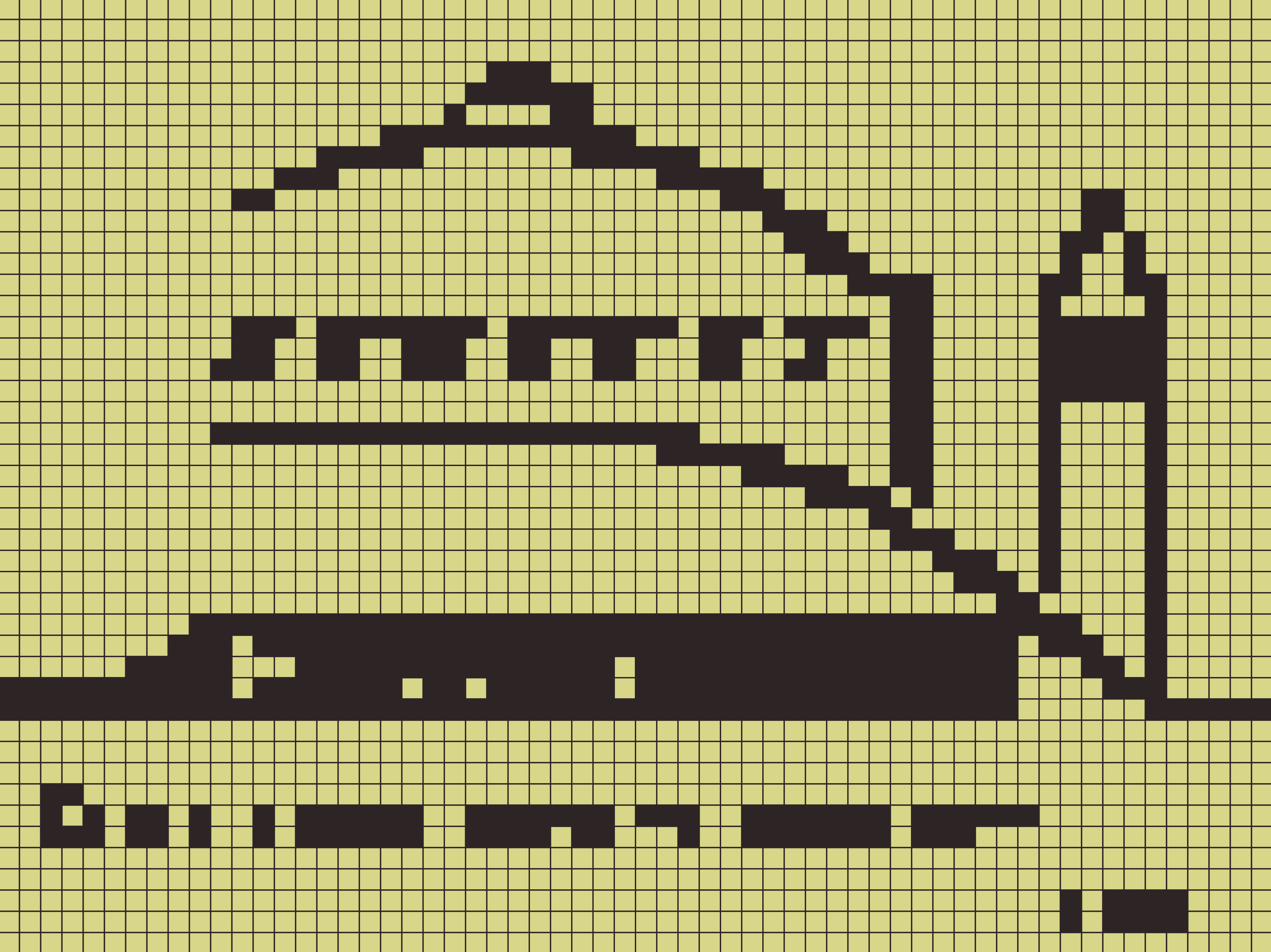


On Picture is Worth …

Much of what happens at LBNL is "taking pictures"

On Picture is Worth …

We worry a lot about getting just the right lighting …

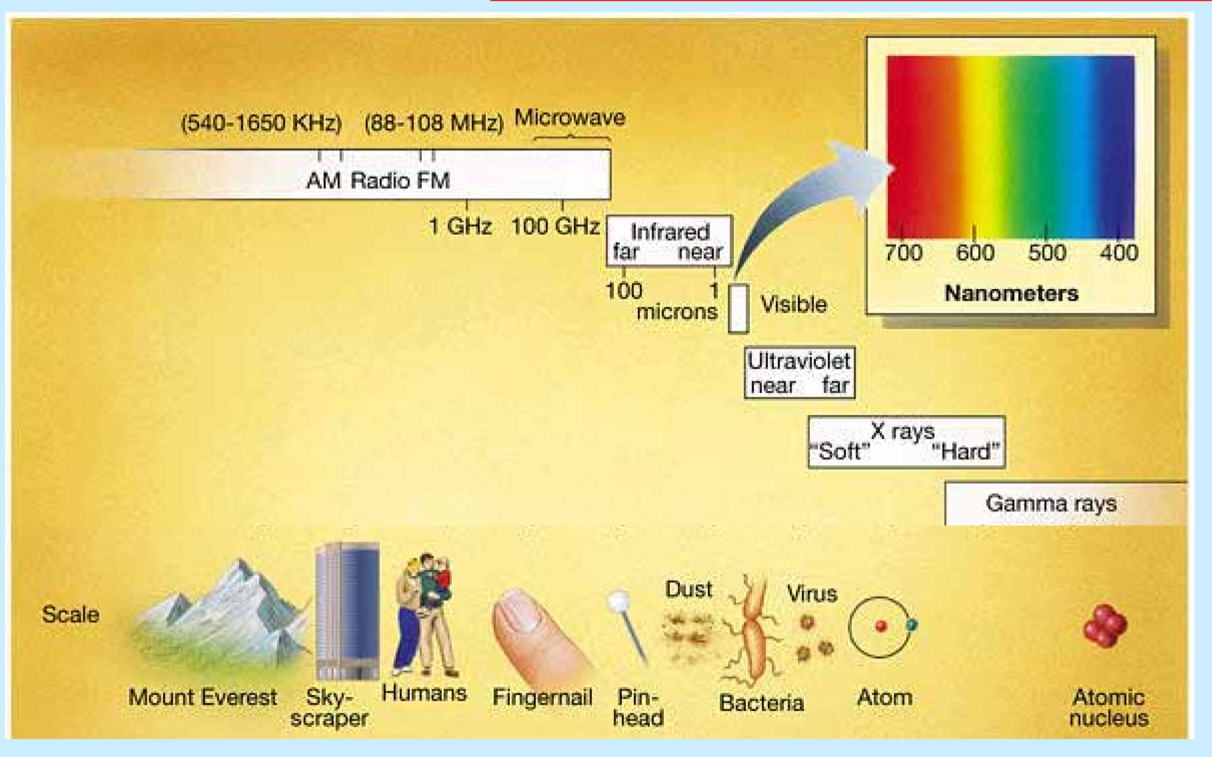
On Picture is Worth …

And of course about the subject …

On Picture is Worth …

But less often "the camera" …

One Picture is Worth …
Solid State Imaging Detectors

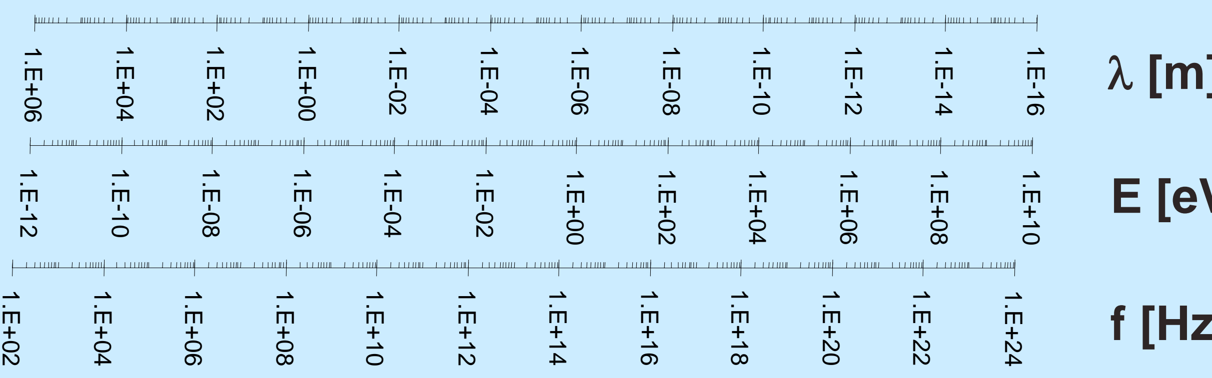


Many objects imaged with visible light

x-rays (ALS)

electrons (EM)

and other charged particles



λ [m]

E [eV]

f [Hz]

Desirable

- (x,y)
- q (or n)
- E (or λ)
- t

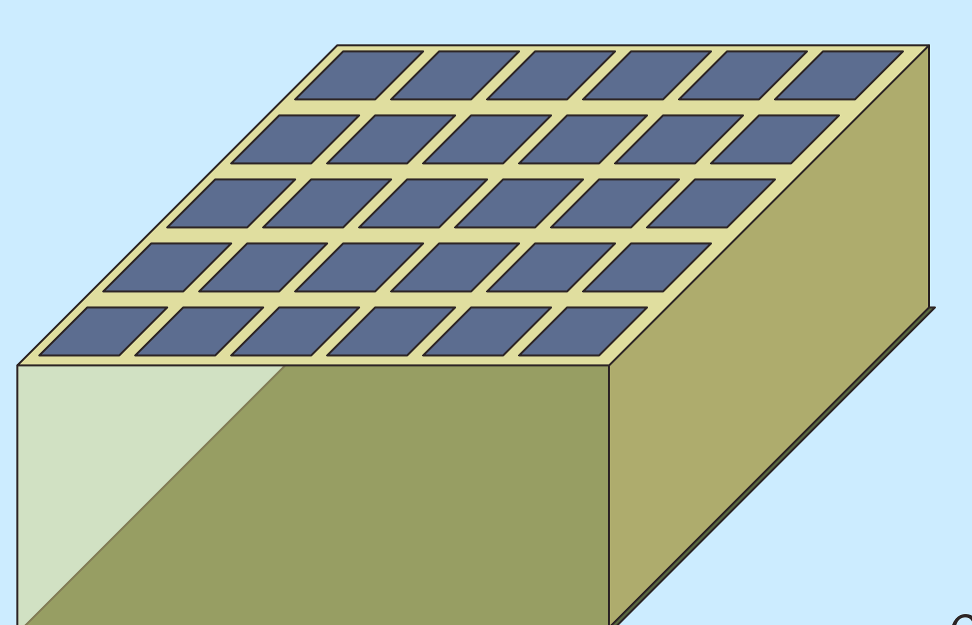
T

δ

X

- X: ∞ (or N = X/δ: ∞)
- Frame rate: ∞
- Dynamic range: ∞
- Non-linearity: 0
- Cost: 0

Solid State Imager



N+ contact

E

p Si

Depletion region

Generally some sort of diode array
(Title is general – talk is about Si)

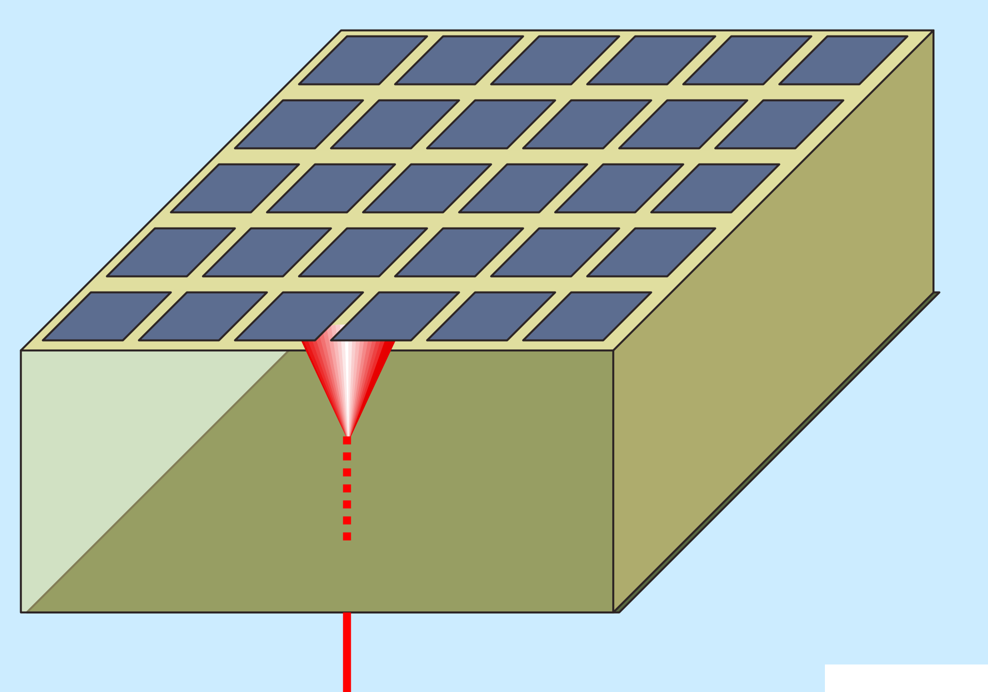
Continuity equation

$$\frac{\partial n}{\partial t} = \mu_n n \nabla E + D_n \nabla^2 n + G_n - R_n$$

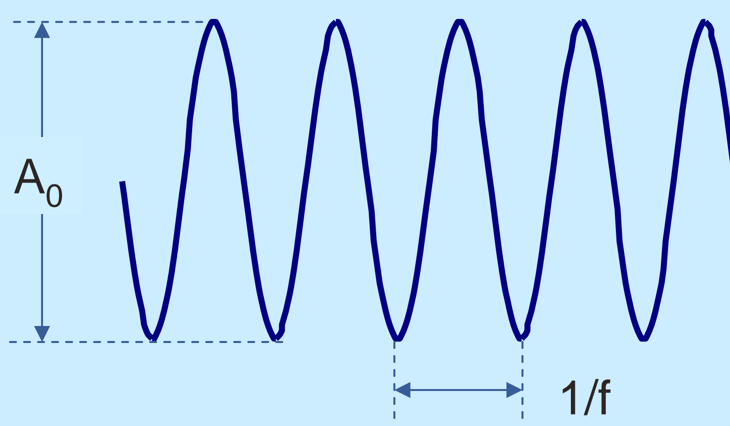
Drift: $v = \mu E$

Diffusion: $D = \frac{kT}{q}\mu$

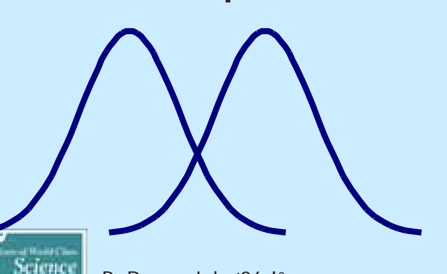
Also important

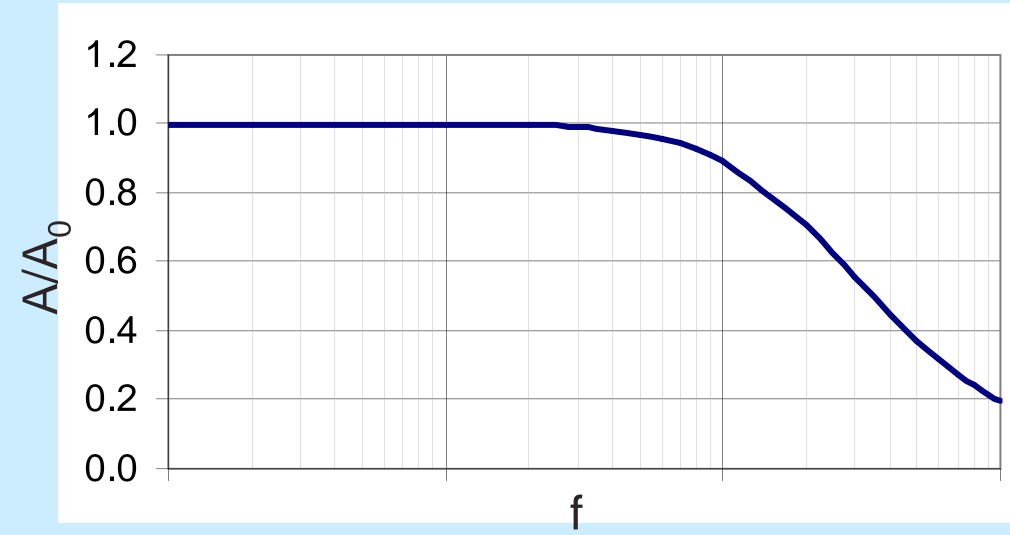


→ MTF: fft(PSF)

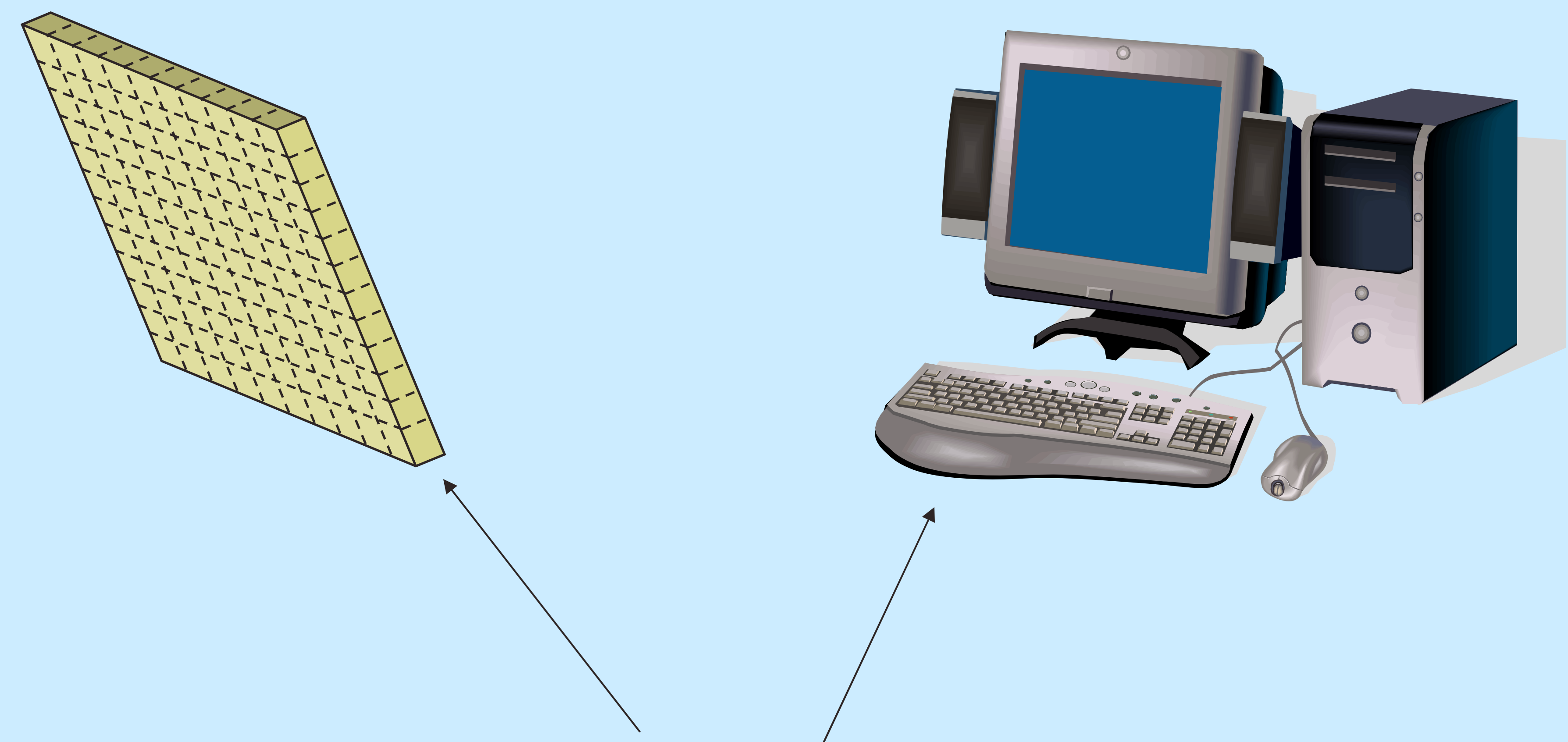


Point spread function – determines spatial resolution





Oh, this also helps



Somewhere between the "sensor" and there needs to be some electronics

Topology

Monolithic
sensor+readout
on same substrate

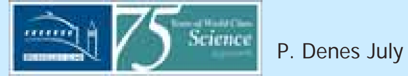
Hybrid

Sensor + Readout

2D segmented Si

2D segmented Si attached to 2D segmented Si

2D segmented Si attached to 1D segmented Si or other electronics



Start with small, but useful, part of spectrum

Consumer imaging is a many $B/year industry
(driven, of course, by such critical needs as →

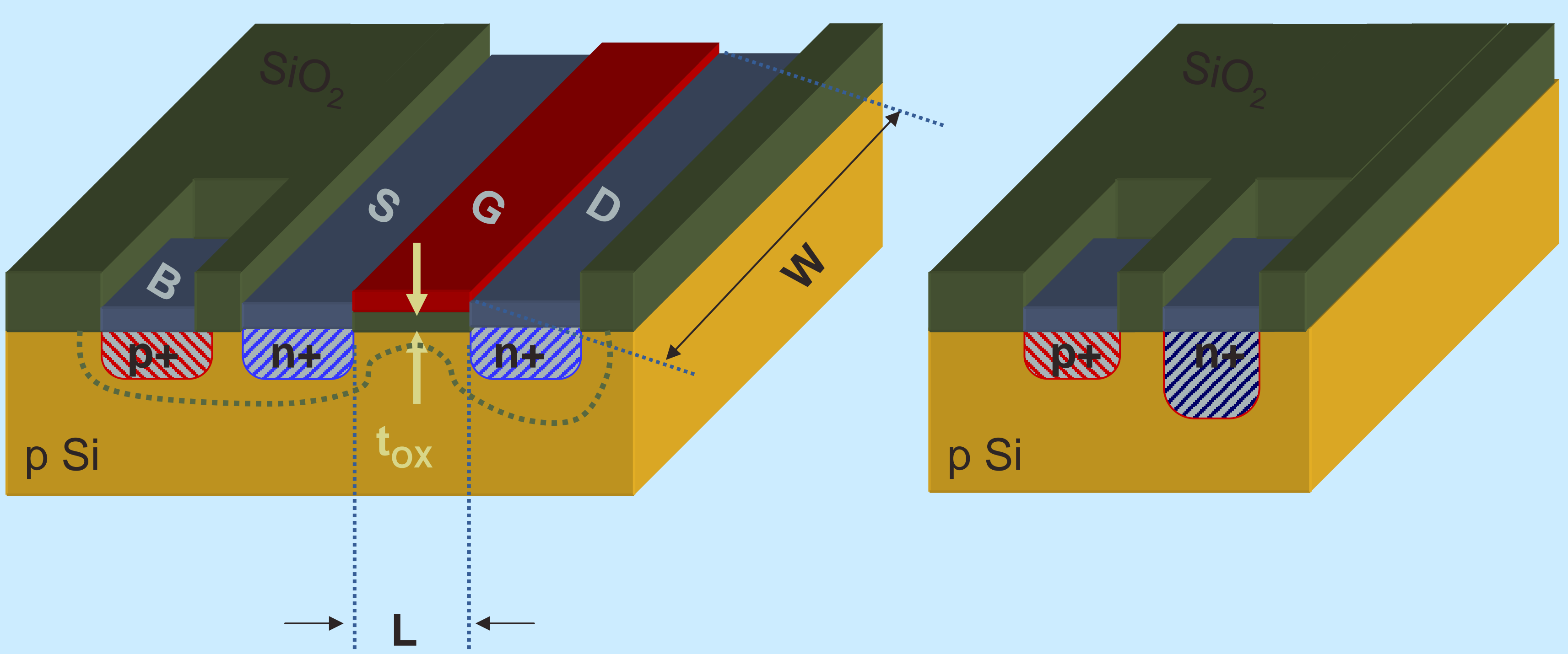
4.5
14.9
13
48.5
1.9
54.7
57.7

- Memory
- Microporcessor
- Logic
- Analog
- Discretes
- Opto
- Sensor

2005 SIA breakdown
($B)

What can we learn? What can we do better?

Integrated Circuit Elements



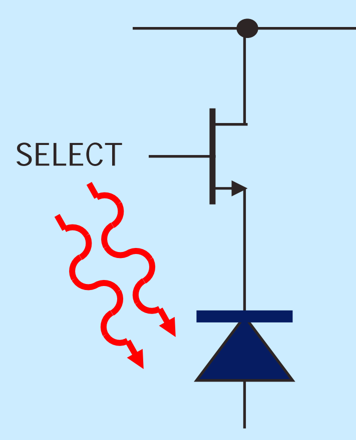
MOS Transistor

pn Diode

Conventional Semiconductor Processing

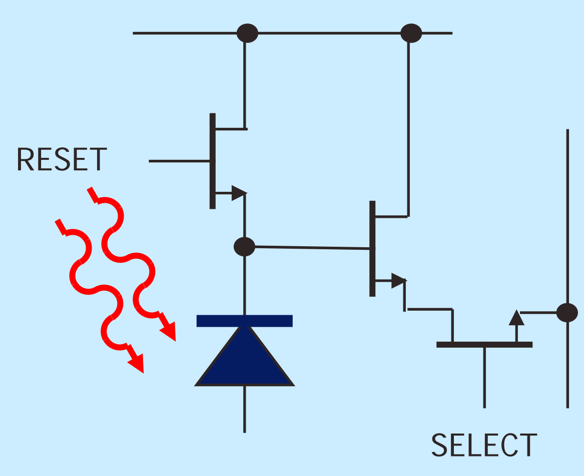
n+ n+ n+ n+ n+ n+

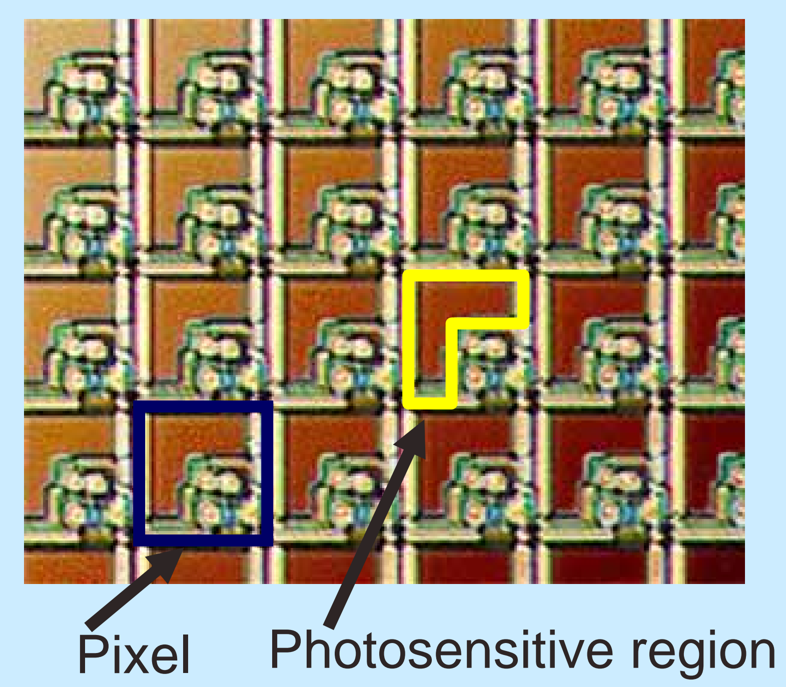
p Si



- Passive Pixel Sensor
- Proposed 1968
- No in-pixel reset
- Poor performance due to capacitive load (nothing buffers the photodiode)

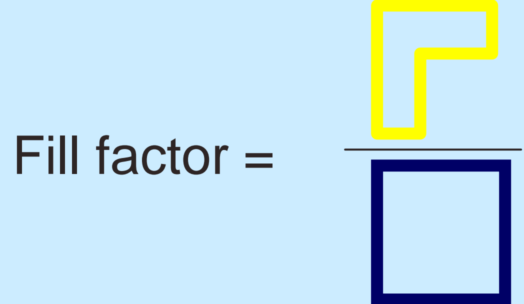
Active Pixel Sensor



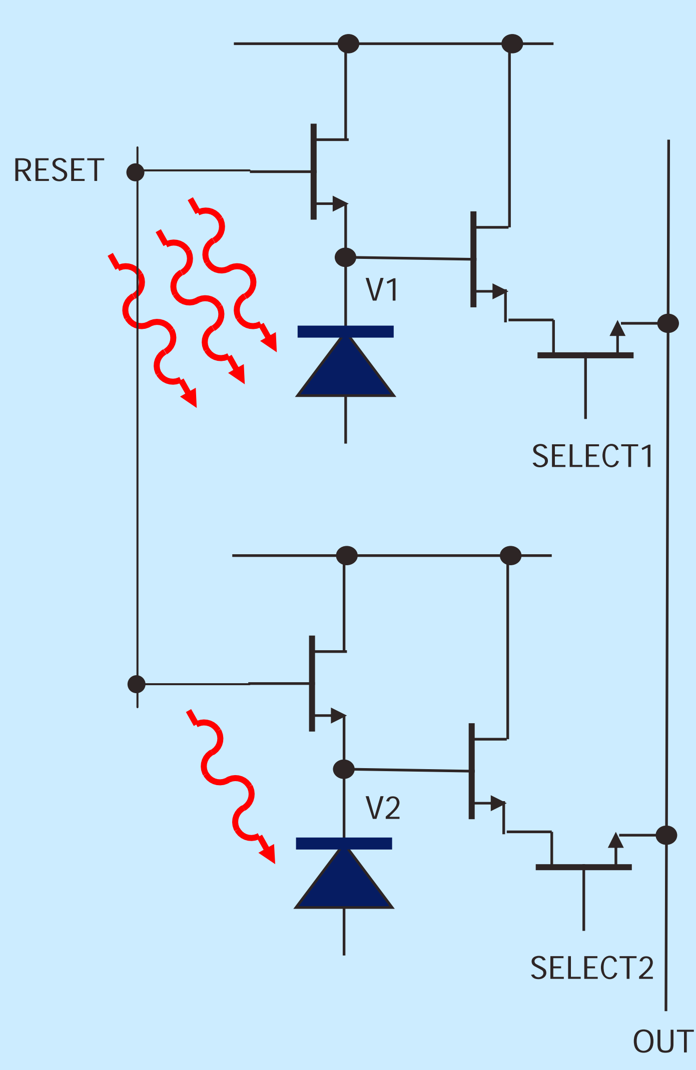


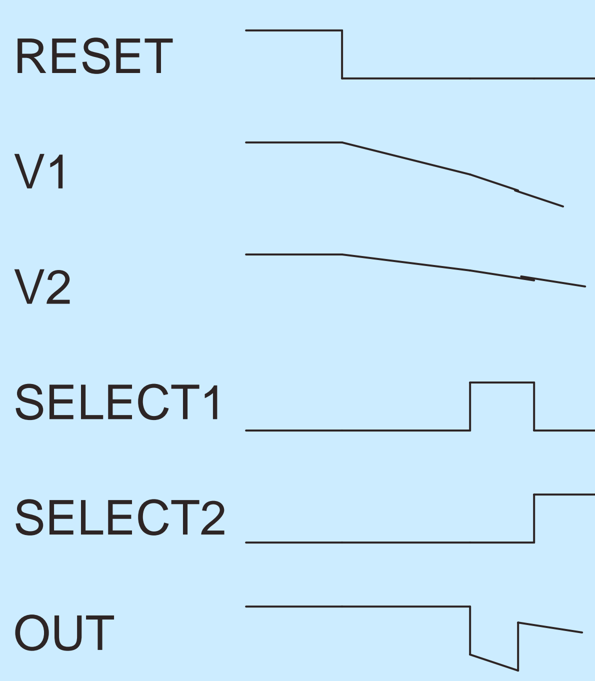
- Active Pixel Sensor
- *Also* proposed 1968
- Many ways to make the photodiode

Fill factor =

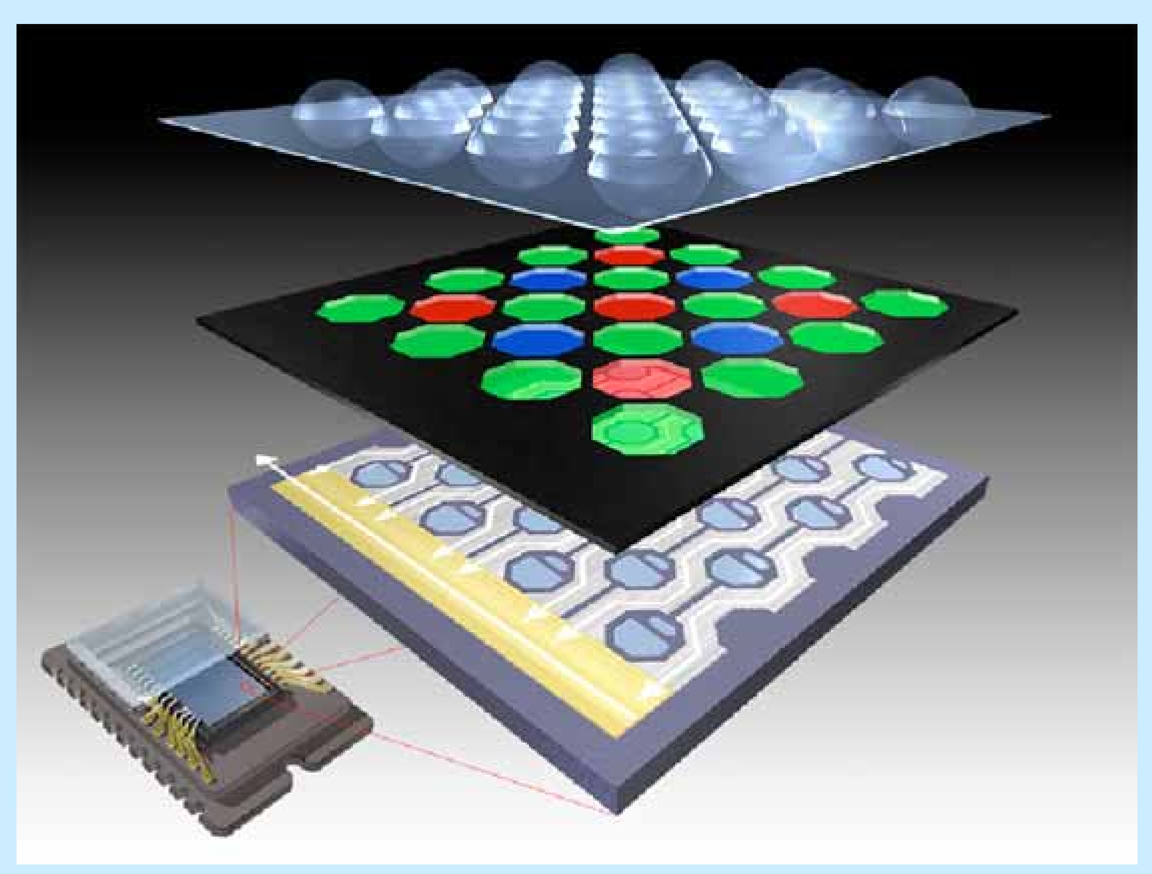


How It Works



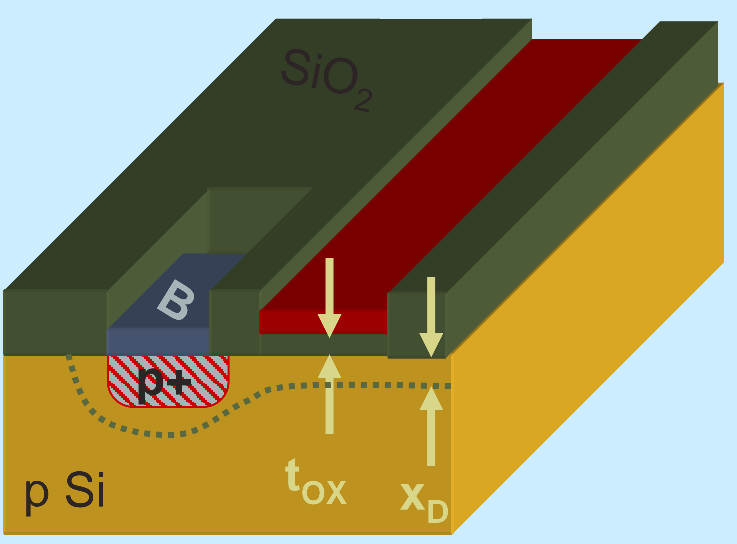


Add Microlens and Color Filter



- Microlens array recovers some of the fill factor
- Opaque walls between cells reduces cross-talk
- Color pattern matched to algorithm

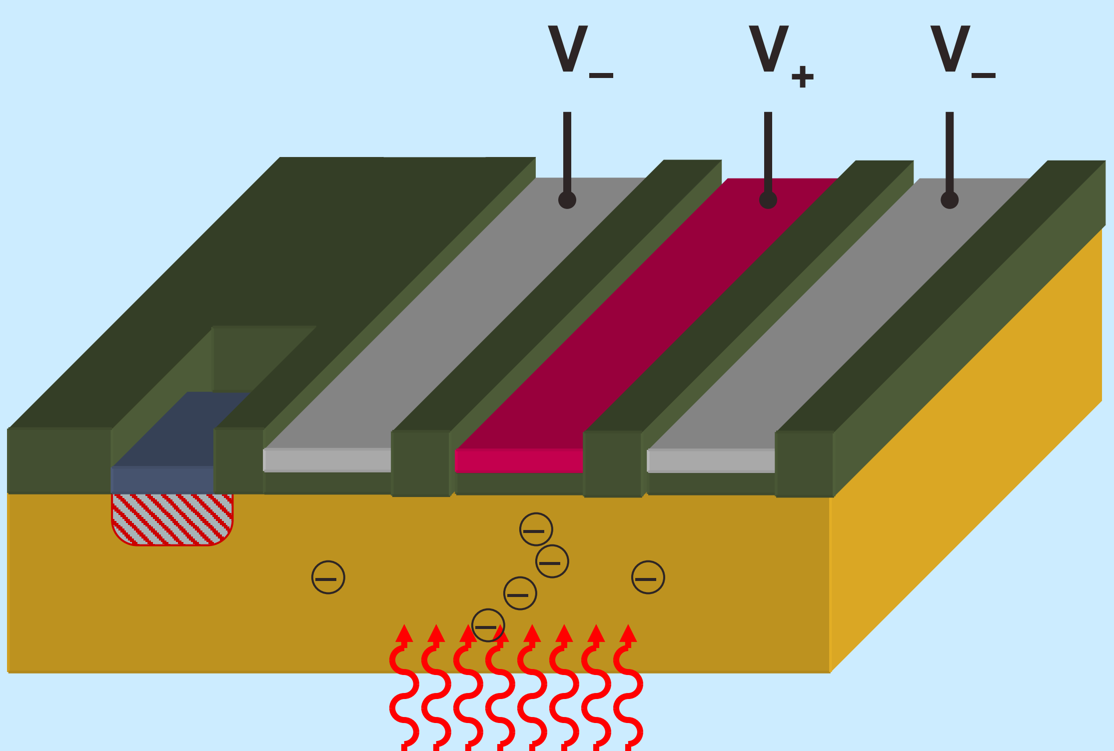
Integrated Circuit Elements



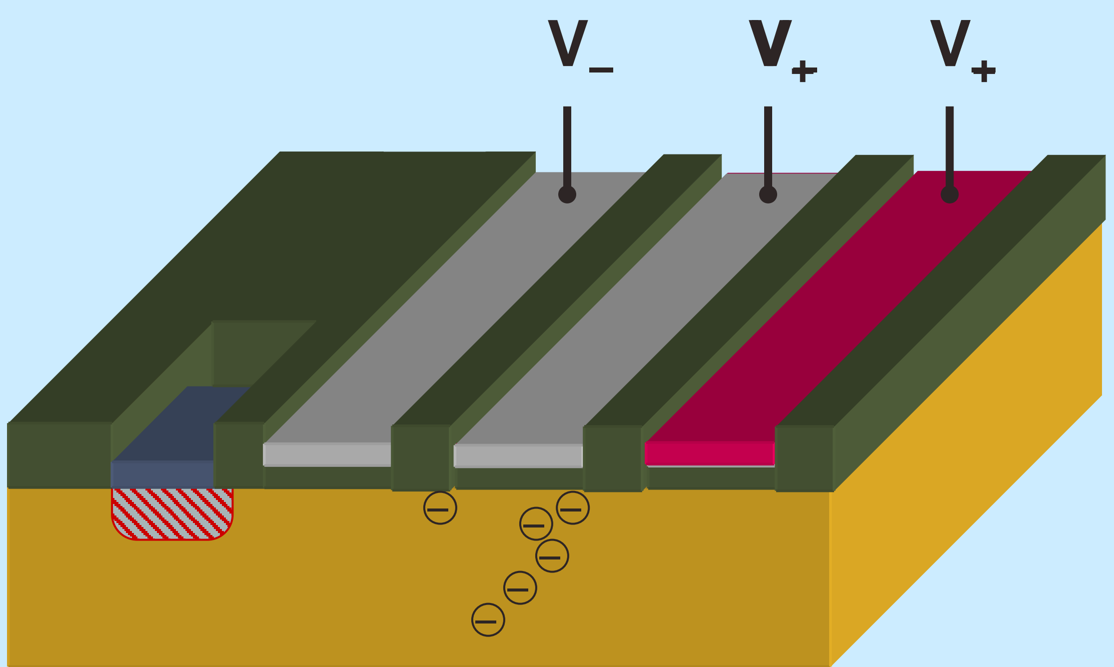
$$C = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_{DEP}}}, \quad C_{OX} = \frac{\varepsilon_{SiO_2}}{t_{OX}}, C_{DEP} = \frac{\varepsilon_{Si}}{x_D}$$

MOS Capacitor

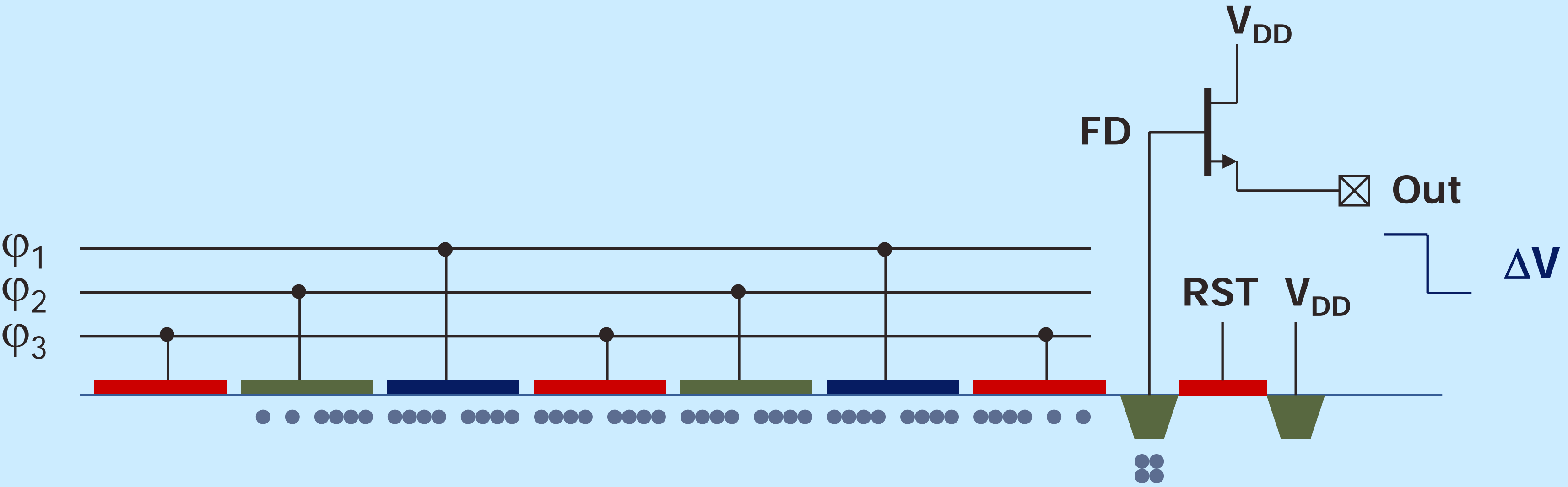
Accumulate Charge



Accumulate and Transfer Charge



Conventional 3-Phase CCD



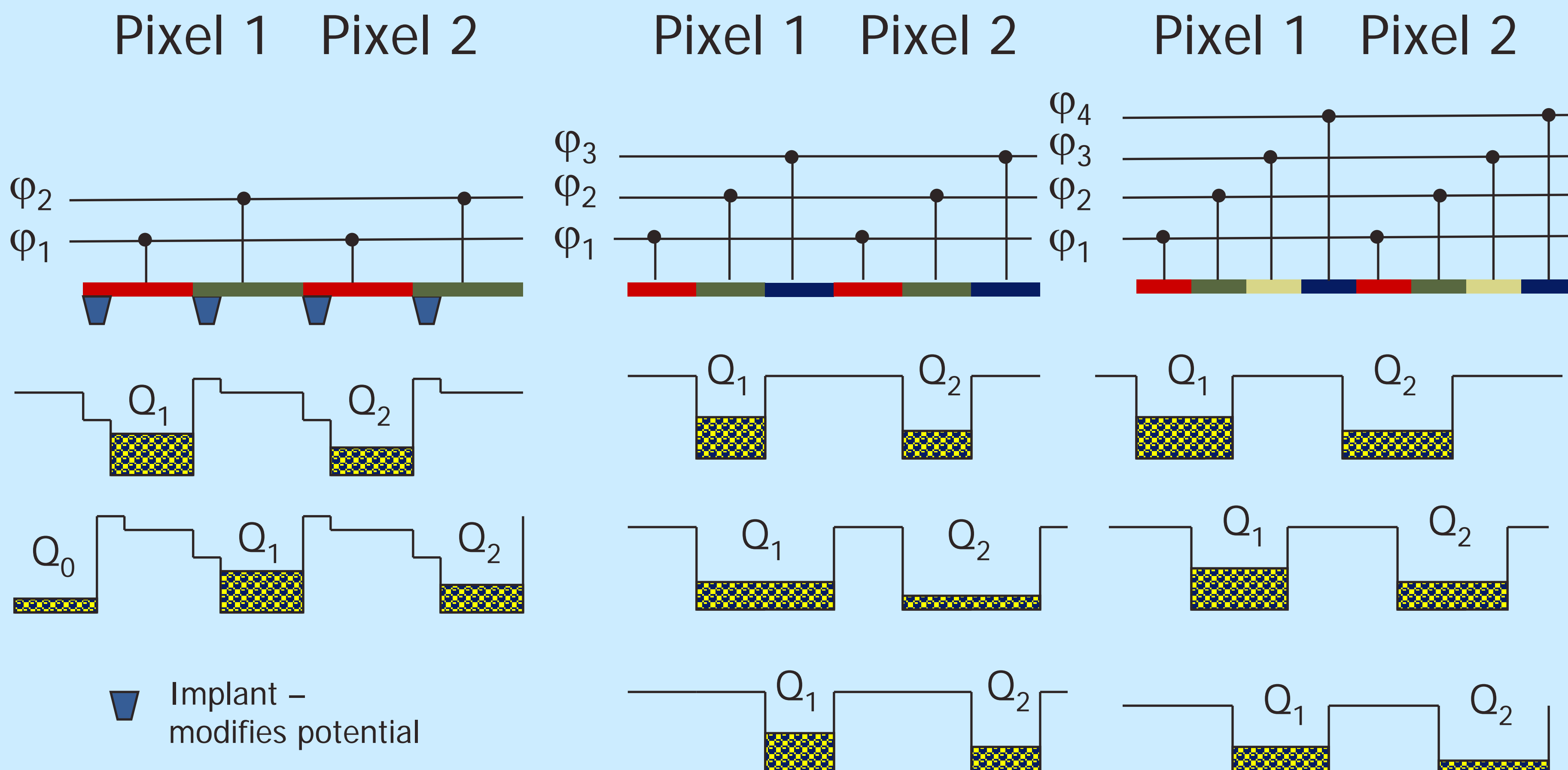
- Noiseless, ~lossless charge transfer
- High gain charge-to-voltage conversion $\Delta V = q/C_{FD}$
- Output amplifier (source follower, or ...) on-chip

Scientific CCDs

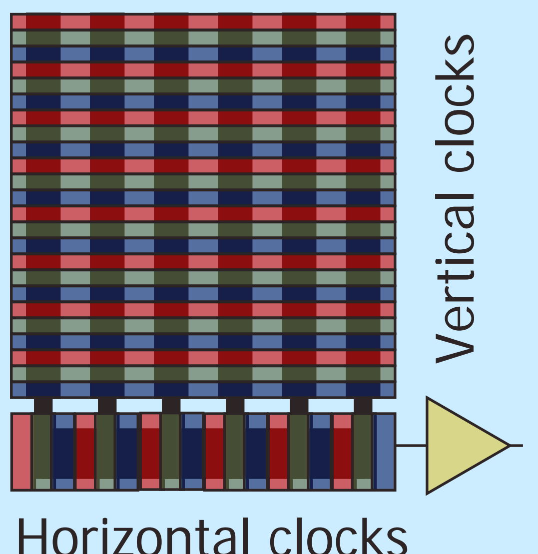
Dumbbell nebula - LBNL CCD
Blue: H-α at 656 nm
Green: SIII at 955 nm
Red: 1.02 mm

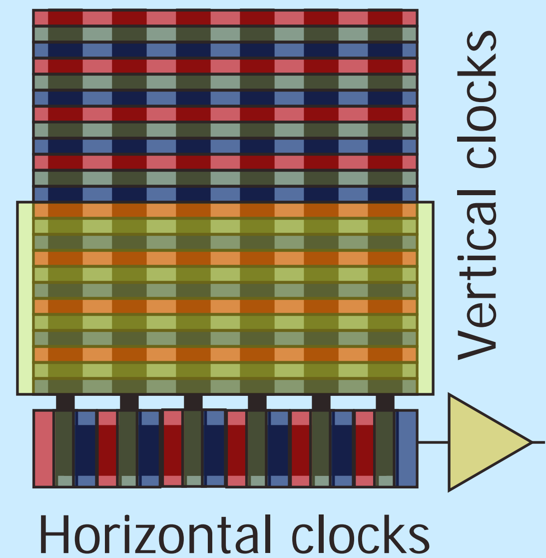
- CCD invented in 1969 by Boyle and Smith (Bell Labs) as alternative to magnetic bubble memory storage
- LST ("Large Space Telescope" – later Hubble) 1965 – how to image?
  - *Film was obvious choice, but -*
    It would "cloud" due to radiation damage in space
    Changing the film in the camera not so trivial
  - *1972 CCD proposed*

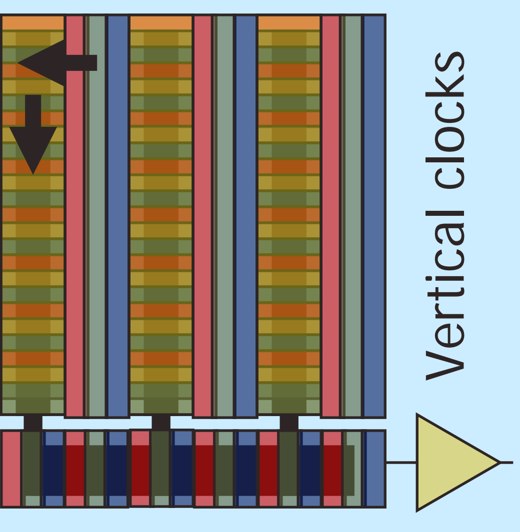
Many ways to do this



Several architectures







Full frame

Frame transfer

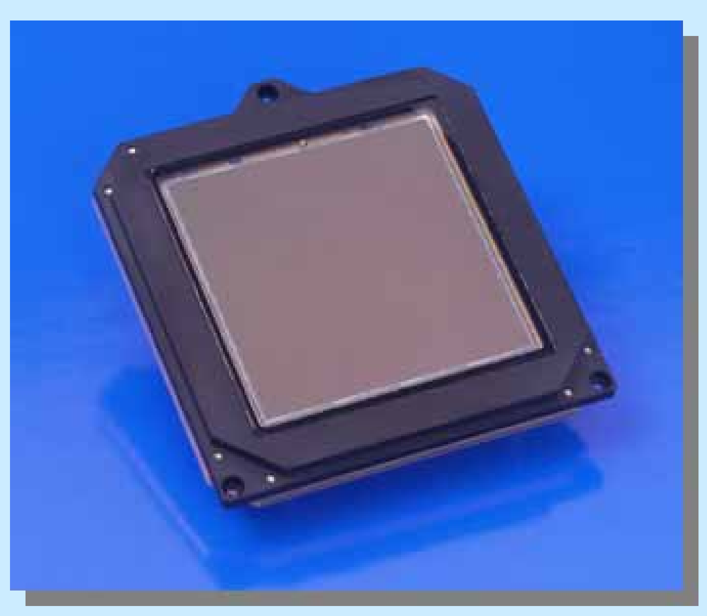
Rapid shift from image to storage

Slower readout of storage during integration

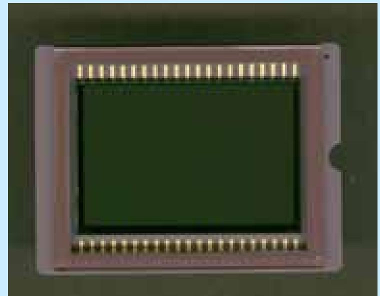
Interline

Very Large Format CCDs (and CMOS imagers)

- Fairchild Wafer Scale Full Frame CCD
  - *9216 x 9216 x 8.75 μm pixel*
  - *80.64 x 80.64 mm^2 size CCD*
  - *Eight 3-stage output amplifiers*
  - *Readout noise < 30e- @ 2/fps*



- Cypress CYIHDS9000
  - *3710 x 2434 x 6.4 μm pixel*
  - *23.3 x 15.5 mm^2 size APS*
  - *0.13 μm imaging CMOS process*



- Canon 16.7 MPix
  - *36 x 24 mm^2 4992 x 3328*
- Kodak 39 MPix
  - *36 x 48 mm^2*

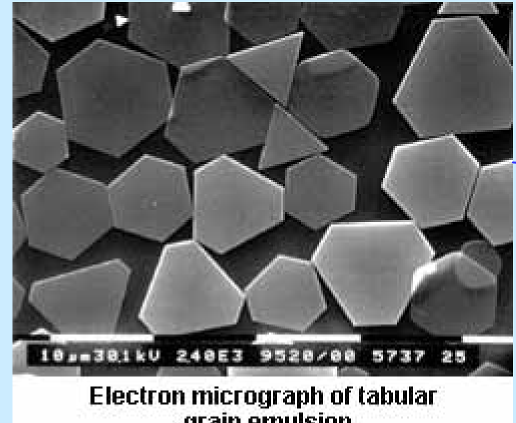
APS vs CCD

- APS – moves a ***voltage*** down the column
- CDS either in pixel or "digital"
- Addressable readout
- Backside illuminated devices not yet really practical
- Support circuitry (clock drivers, digitizers) required

- CCD – moves a ***charge*** down the column
- "Intrinsic" CDS
- Sequential readout
- Backside illuminated devices practical (thick ones, too)
- Can be monolithic – one chip

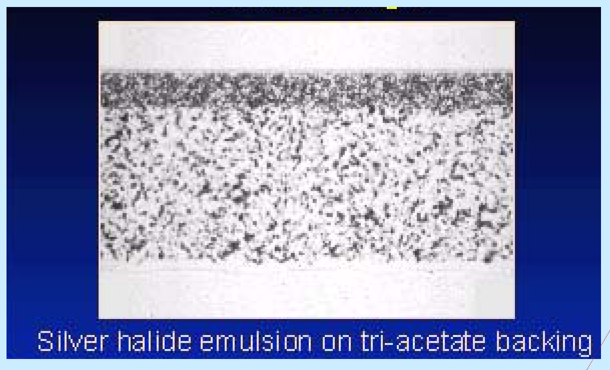
Otherwise roughly the same. In principle, equivalent dynamic range.
In principle, same leakage current (but not in practice)
Monolithic device much more profitable → prevalence in market

The Competition - Film



Electron micrograph of tabular grain emulsion

AgX + gelatin
(emulsion)

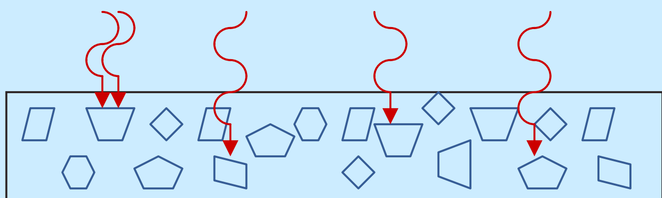

Silver halide emulsion on tri-acetate backing

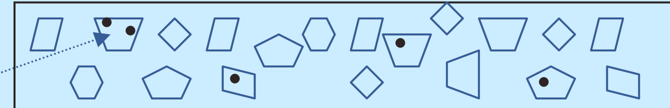
backing

sub-micron to few micron grains
CMOS / CCD ~7 – 10 μm

How it works

Incident light

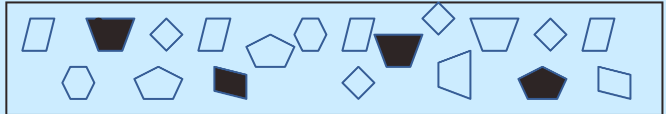




phototelectrons convert Ag^+ sites to Ag^0 – at the same time, thermal fluctuations tend to “erase” the image. Generally, a few photons are required to leave a “latent” image on a grain

larger grains have larger cross section, so they are more likely to get hit. Thus, larger grains are “faster” but “grainier”

How it works

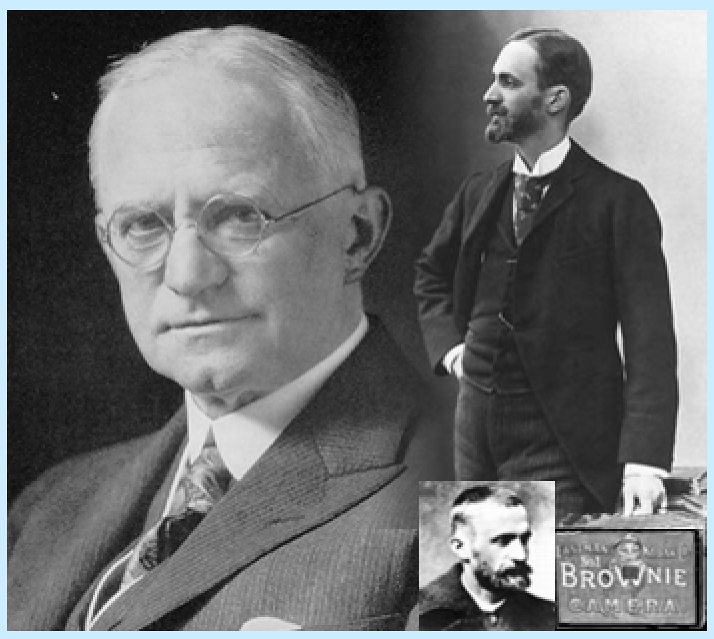


“develop” the image so that the sensitized AgX is reduced to black metallic silver

“fix” the image – removing the unexposed AgX

The chemistry and physics of photographic film is not trivial

Historical Footnote



George Eastman
"You press the button, we do the rest"

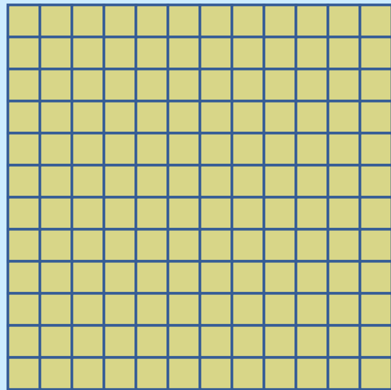
Hannibal Goodman
Minister at the House of Prayer in Newark, New Jersey
(files for patent in 1887 – granted 1898)

The devil is in the details: “photographic plates” (emulsion on glass) → cellulose nitrate for first motion pictures (tends to burn – don’t yell “fire” in a theater → “safety film” (Kodak 1911) – not really perfected until 1948 (triacetate)

Who Wins?

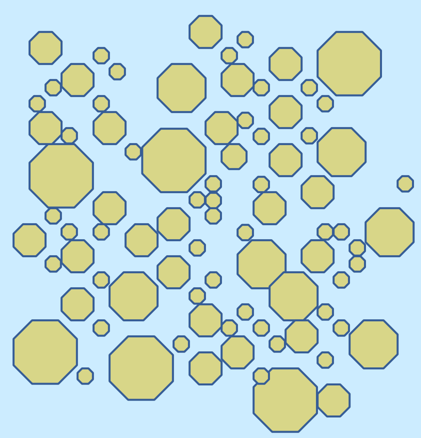
Silicon

Film

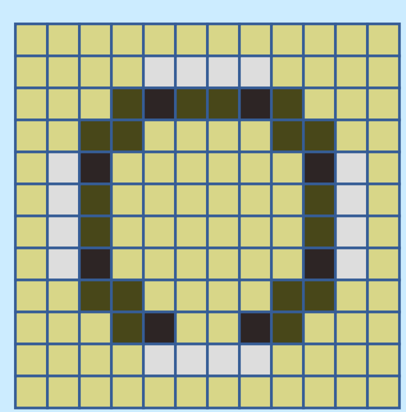


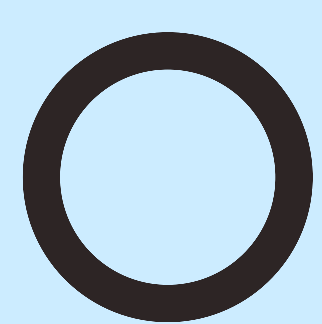
Regular array of pixels
pitch p

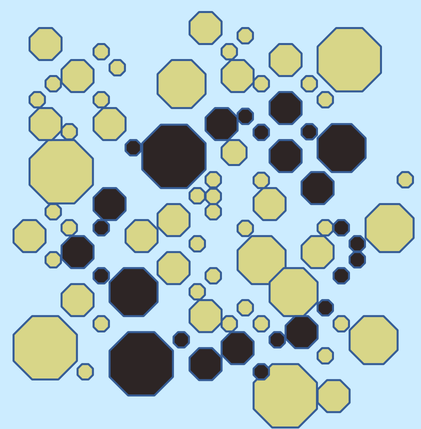
Random collection of
different grain sizes



For now film grains smaller than silicon pixels







Analog

Digital

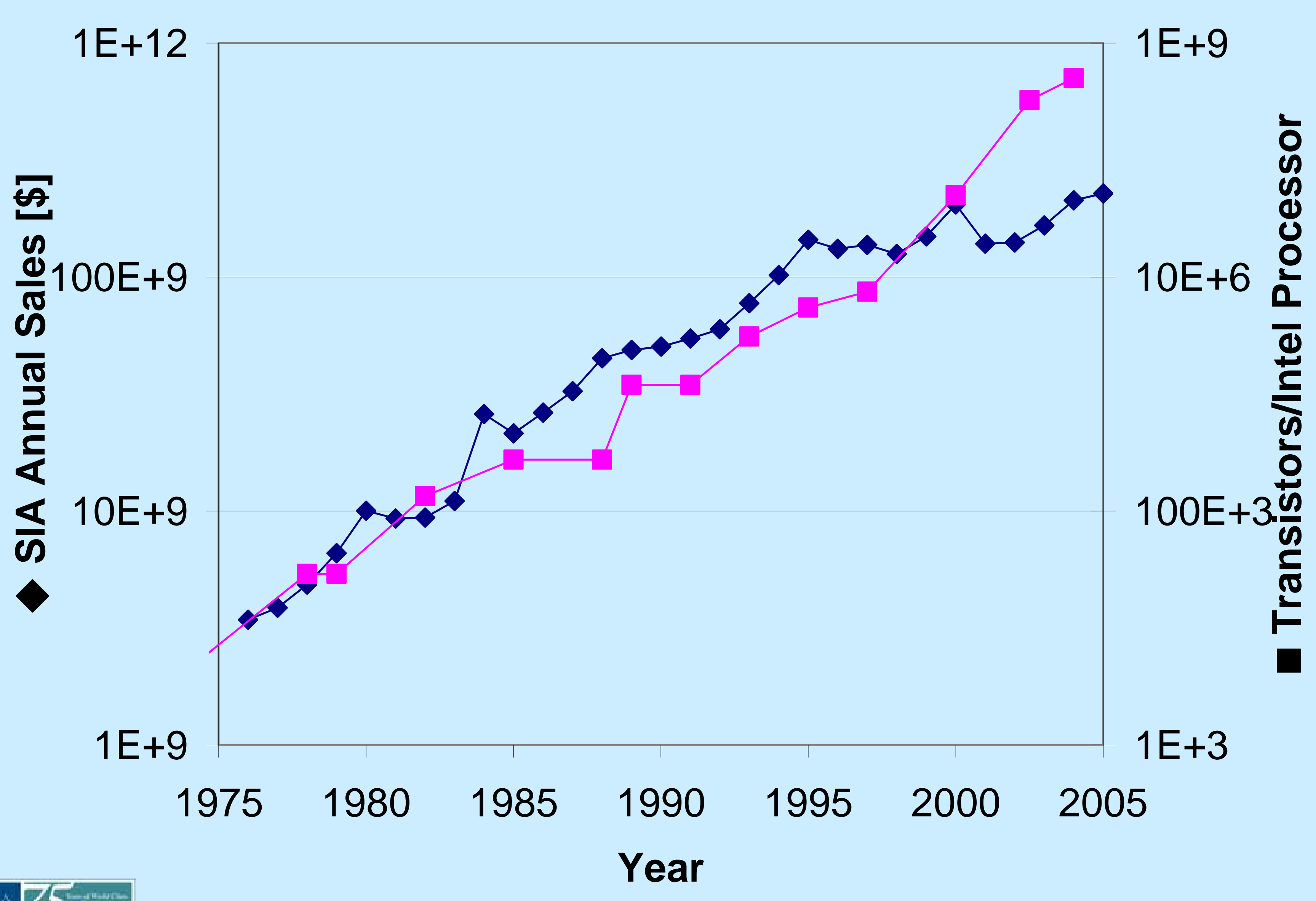
Pros and Cons

	Silicon	Film
Processing	Electronic	Chemical
Linearity	"ideal" $n(e^-) = QE \times n(\gamma)$	non-linear – n γ required to flip a grain; thermal fluctuations vs grain size
Resolution	Larger pixels	Smaller grains
Dynamic range	CCDs – 16 bits	Locally, ~4 bits
Integration time	Ultra-high quality process – minutes; opto process – seconds; normal process – ms	"long" (also thermally limited)
MTF	Regular pattern – aliasing	Given by smallest grains, no aliasing
MTF x S/N	Better	Worse

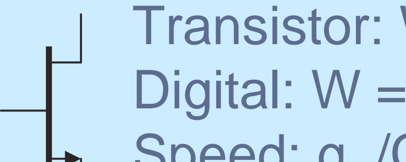
Marketplace has decided

Photo Marketing Association International 2005 Outlook

Technical Drive for Industry



Exponential Growth Achieved by Feature Size Shrinkage

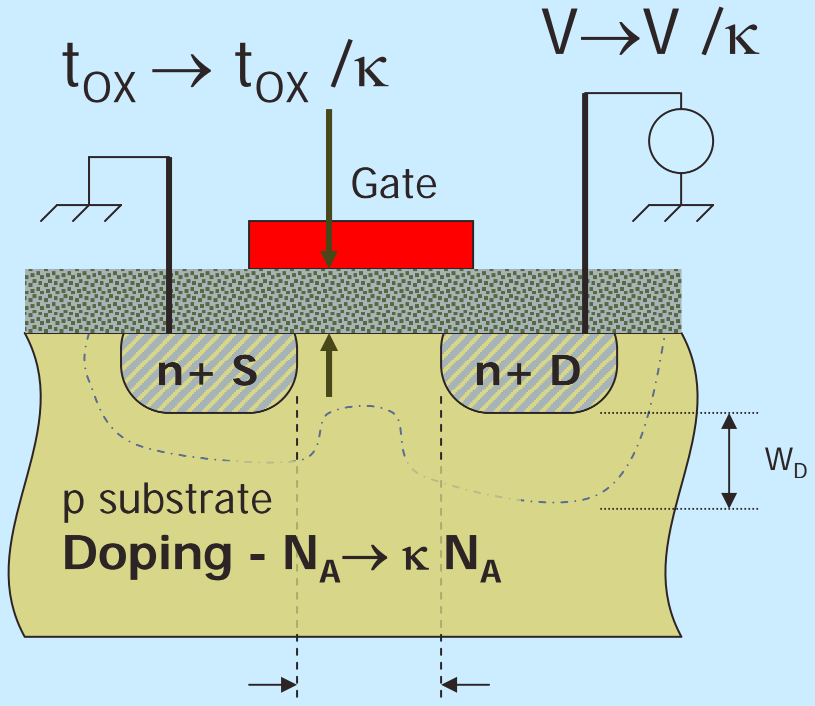


Transistor: W, L
Digital: W = *c*L
Speed: g_m/C
Size: WL

$$g_m \sim \mu \frac{\varepsilon_{SiO_2}}{t_{OX}} \frac{W}{L} (V_{DD} - V_t)$$

$$C \sim \frac{\varepsilon_{SiO_2}}{t_{OX}} WL$$

CMOS driven by **constant field** scaling*



Channel Length L →L /κ

**Not the only way, but life is digital (evidently)*

Why constant field scaling?

	Scale geom. W, L, t_{OX} ↓κ	Scale voltages too V_{DD} and V_T also ↓κ
Area	$1/\kappa^2$	$1/\kappa^2$
$g_m \sim \mu \frac{\varepsilon_{SiO_2}}{t_{OX}} \frac{W}{L}(V_{DD} - V_t)$	κ	1
$C \sim \frac{\varepsilon_{SiO_2}}{t_{OX}} WL$	$1/\kappa$	$1/\kappa$
Speed $\sim g_m/C$	κ^2	κ
Power $\sim CV_{DD}^2$/speed	κ	$1/\kappa^2$
Power density ~Power/Area	κ^3	1

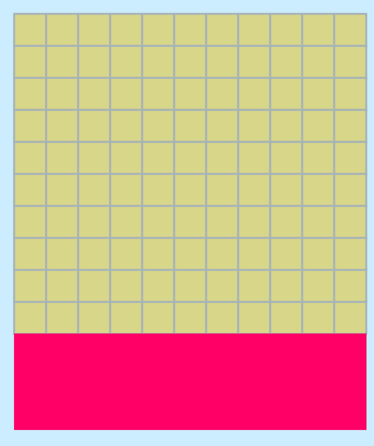
What This Means

Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										
V_{DD} (V)	5.0	5.0	5.0	3.3	3.3	2.5	1.3	1.2	1.1	0.8
t_{OX} (Å)	350	250	180	120	100	70	30	13	9	6
Oxide field (10^6 V/cm)	1.4	2.0	2.8	2.8	3.3	3.6	4.3	9.2	12	13
Production	1980	1983	1988	1991	1995	1997	2001	2003	2007	2012

How long this can go on is a good topic for another talk …

Why not combine CMOS and CCD?

a dream process?



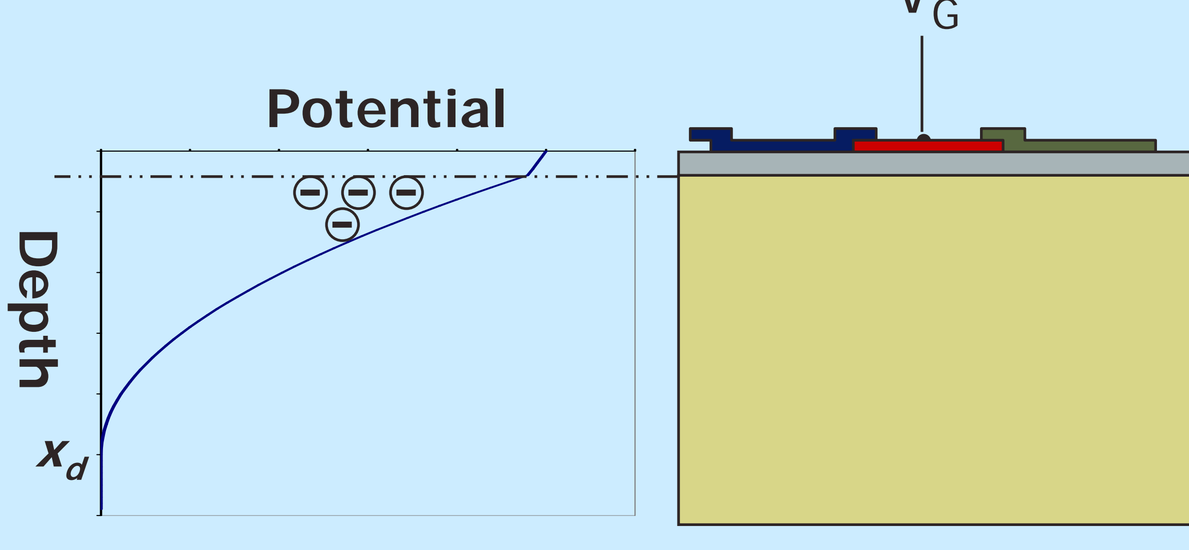
CCD pixel region

CMOS amplifiers/digitizers

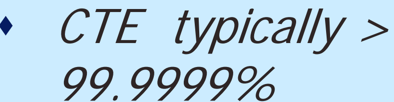
CCDs have certain specialized requirements

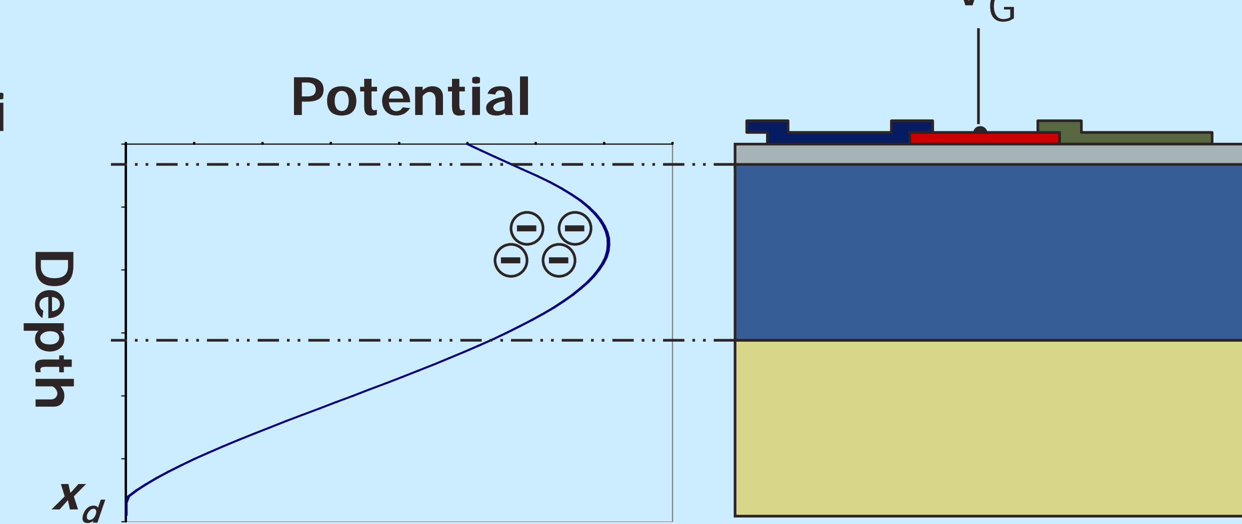
Surface vs buried channel CCD

- MOS capacitor
- Potential maximum at Si – SiO_2 interface
  - *CTE < 1 due to trapping at interface*



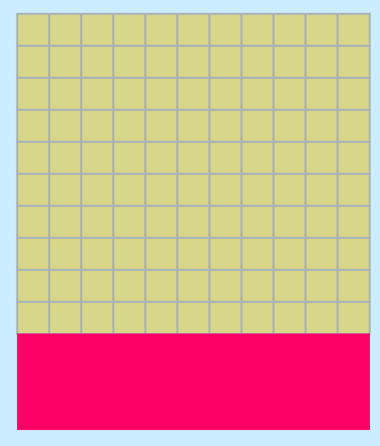
- Potential maximum not at Si – SiO_2 interface
  - *CTE typically > 99.9999%*





Why not combine CMOS and CCD?

a dream process?



CCD pixel region

CMOS amplifiers/digitizers

CCDs have certain specialized requirements
- buried channel
- triple poly (for 3-phase CCDs)

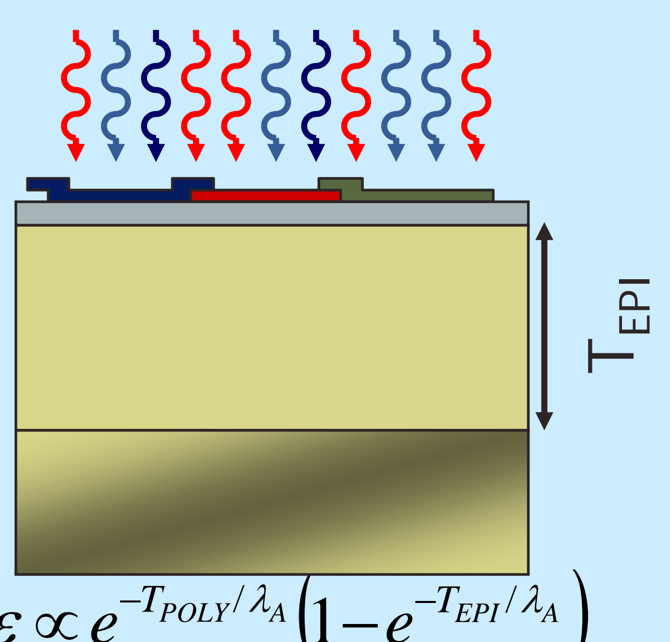
- deep implants, thick low doping regions, thick gate oxides (high voltages) all go in the opposite direction of shrinking CMOS

CCD vs APS

- CCD will survive (genuinely better for certain applications – see below), and will continue to be the best solutions for max(area, pixels, dynamic range, speed)
- APS will (is) dominating consumer market
  - *APS can be a single chip solution*
  - *CCD needs clock drivers, digitizers, digital logic so APS is ultimately cheaper for mass-market applications*
- One could combine CCD and CMOS, but (so far) there's no commercial push.

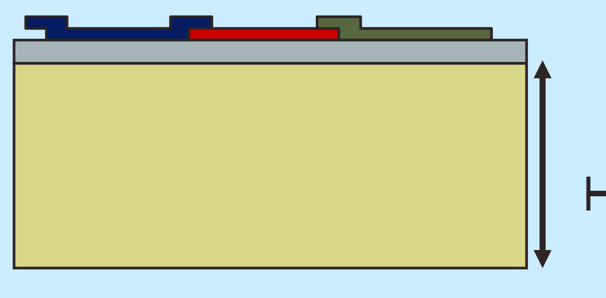
- One area where CCDs offer an advantage is:

Frontside/Backside Illumination



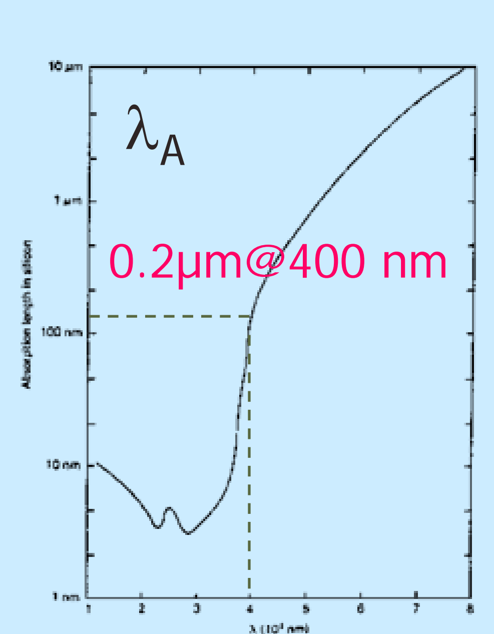
$$\varepsilon \propto e^{-T_{POLY}/\lambda_A}\left(1-e^{-T_{EPI}/\lambda_A}\right)$$

Fill factor < 1

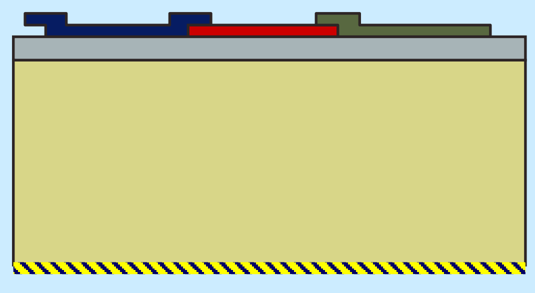


$$\varepsilon \propto \left(1-e^{-T_{EPI}/\lambda_A}\right)$$

Fill factor = 1



Backside Illumination



This should be depleted – generally thin with conventional processes

→ add a layer which can be used as an electrode

PROPOSAL:
Make a thick CCD on a high-resistivity n-type substrate, operate fully depleted with rear illumination.

3-phase CCD structure

Poly gate electrodes

buried p channel

n^{--} (10 kΩ-cm)

photo-sensitive volume (300µm)

Transparent rear window

Advantages:

1) Conventional MOS processes with no thinning => "inexpensive"
2) Full quantum efficiency to > 1 µm => no fringing
3) Good blue response with suitably designed rear contact
4) No field-free regions for charge diffusion, good PSF

Disadvantages:

1) Enhanced sensitivity to radiation (x-rays, cosmic rays, radioactive decay)
2) More volume for dark current generation
3) Dislocation generation

seh_newccd2.eps

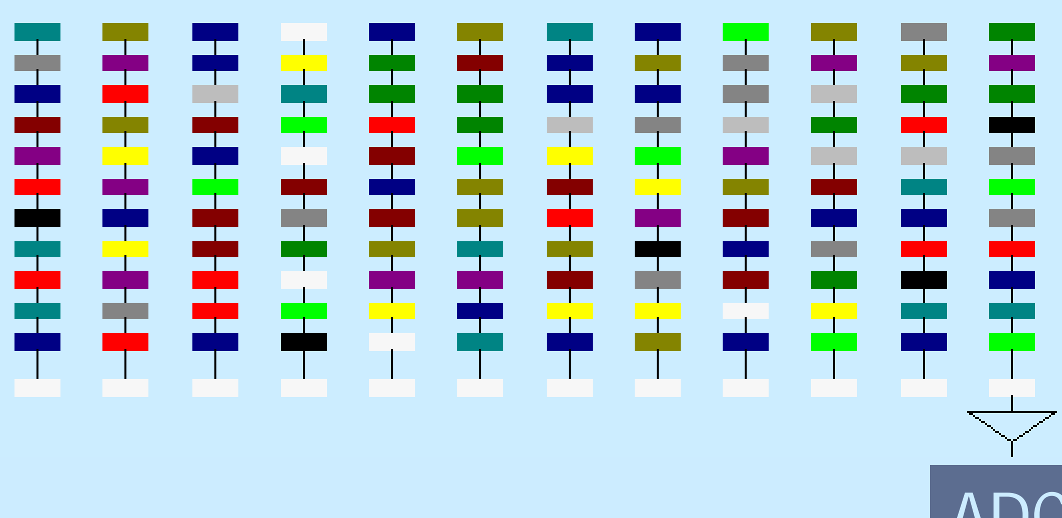
LBL CCD – S. Holland et al.

CCDs are wonderful

But they are slow

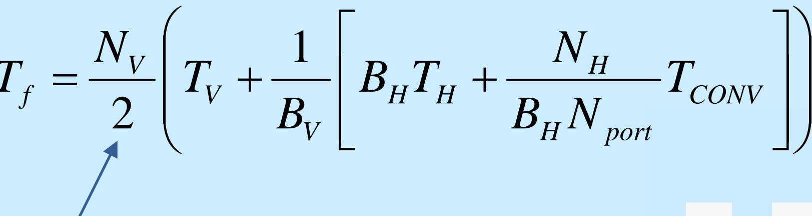
- Parallel exposure
- Serial readout

- Vertical clock
- Horizontal clock
- External, high resolution ADC



Now it gets more difficult

Increase ADC speed



$$T_f = \frac{N_V}{2}\left(T_V + \frac{1}{B_V}\left[B_H T_H + \frac{N_H}{B_H N_{port}} T_{CONV}\right]\right)$$

top+bottom readout

N_V, N_H = # H, V pixels

B_V, B_H = H, V binning

T_V, T_H = H, V shift time

N_{port} = # ports

T_{CONV} = total conversion time including reset, summing well, …

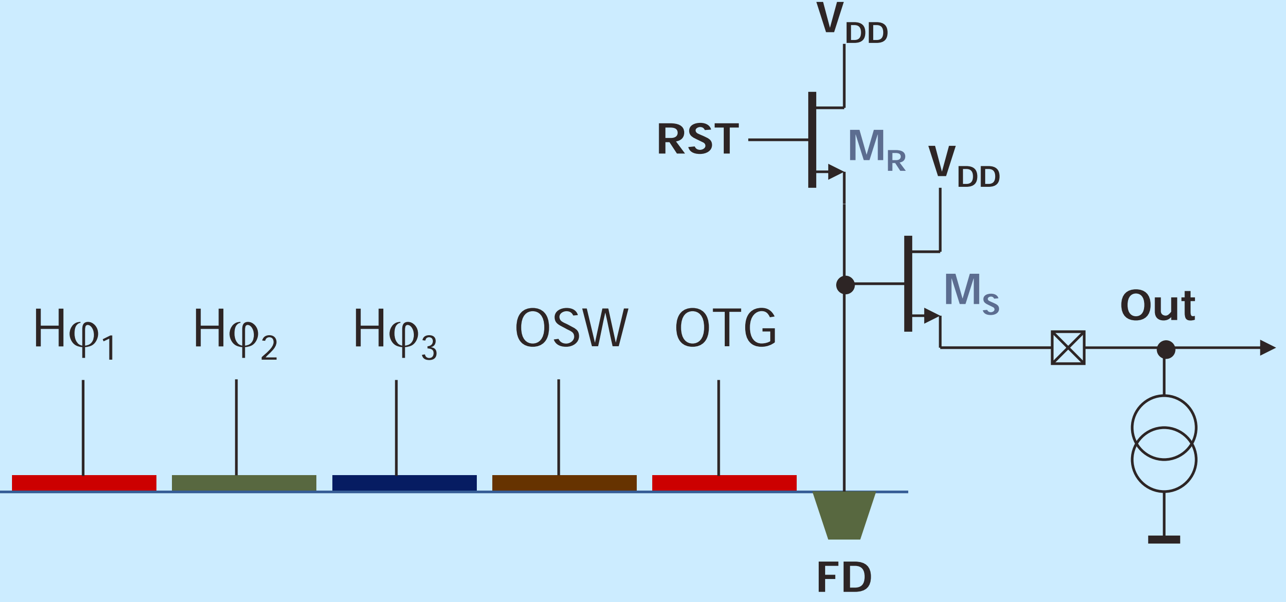
ADC

ADC

ADC

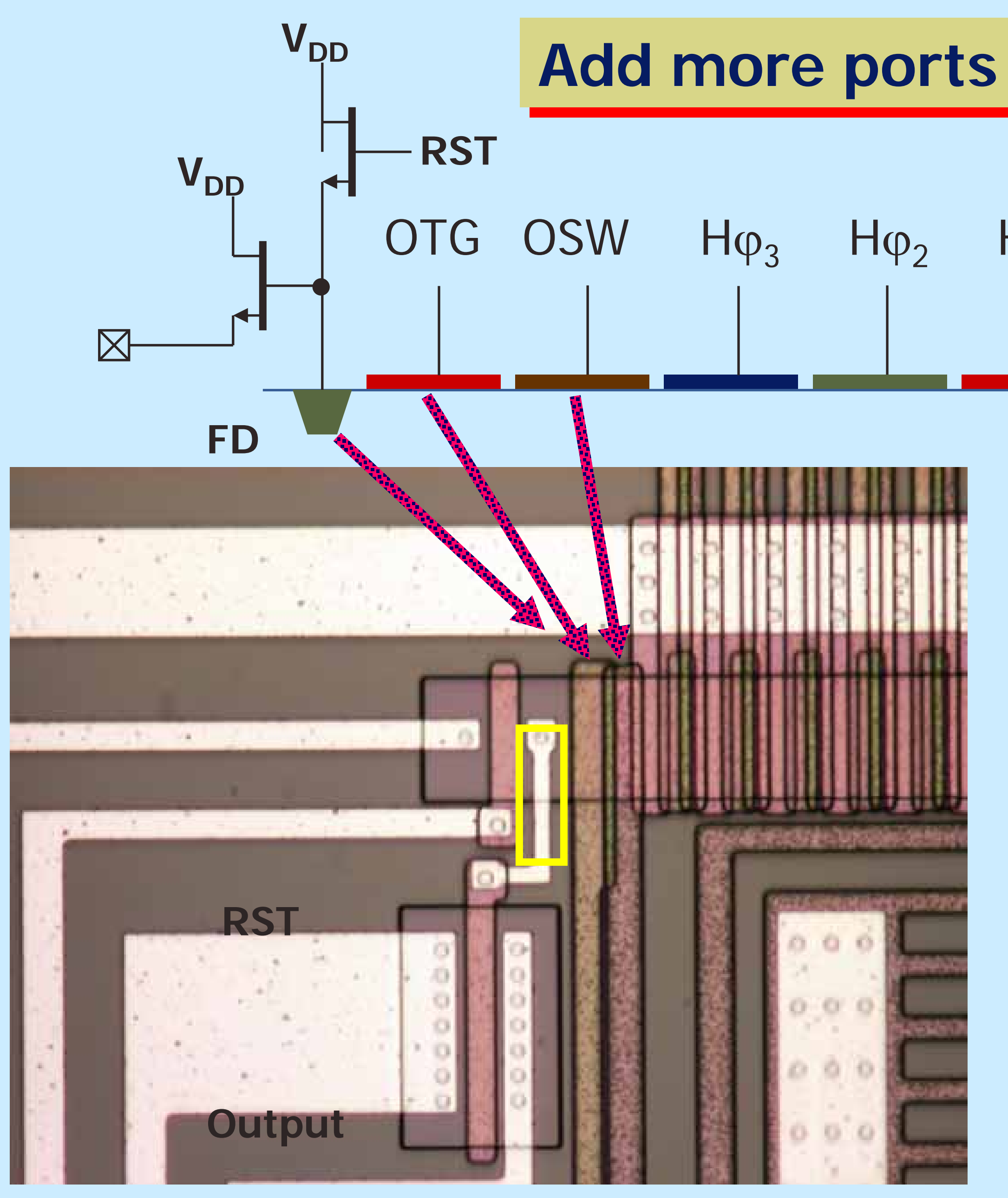
ADC

Limitations



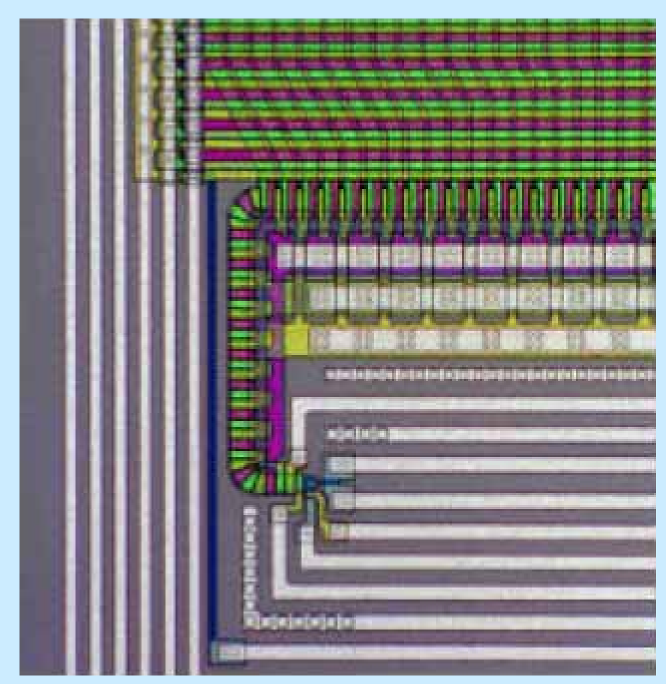
- $\sqrt{kTC}$ Noise contribution from M_R (reset switch) removed by CDS (correlated double sampling – measure V_R and $V_R + V_S$)
- Noise contributions from M_S (source follower) ↑ ~ √rate
- Ultimately limitations in charge transfer

Add more ports



- Reset and output transistors need room
- Want to minimize C_{FD}
- Need space for the output stage!

One way to gain space



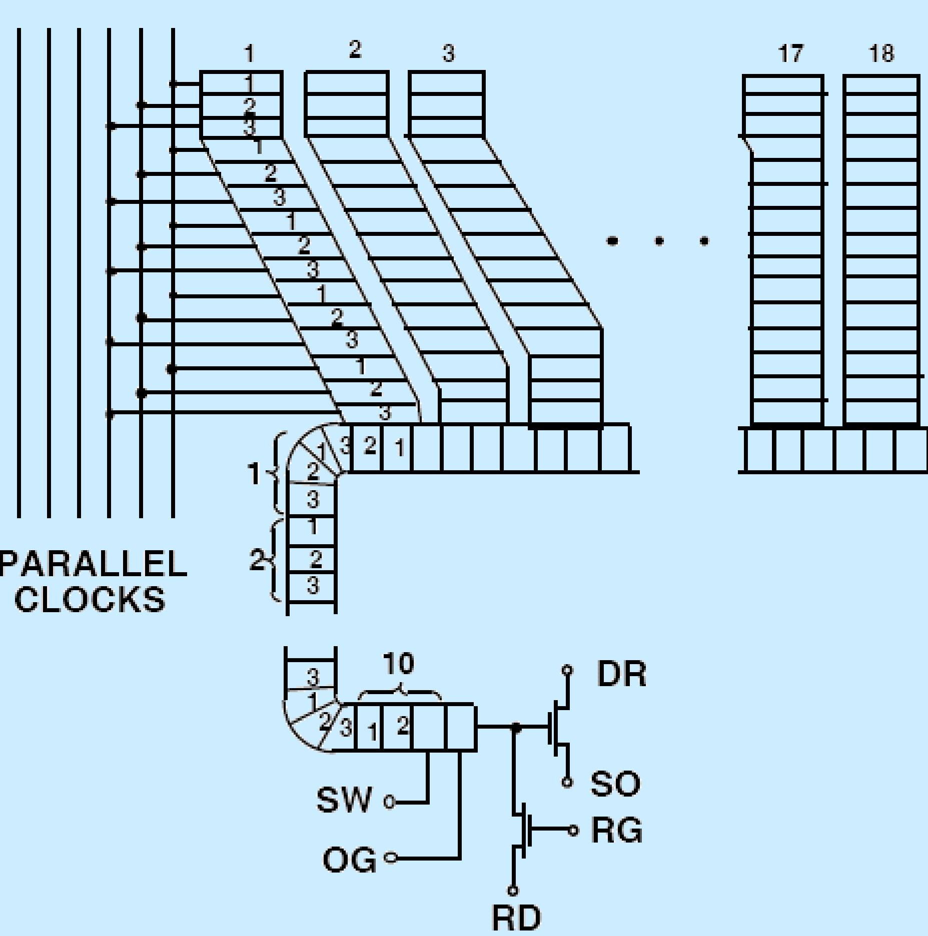
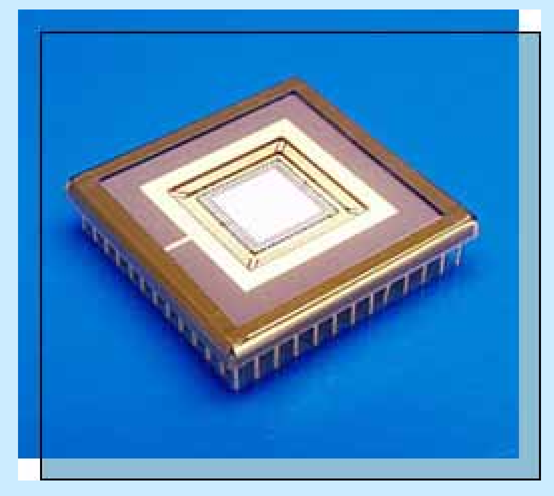


Figure 4. Depiction of the region around the output circuit

MIT Lincoln Labs multi-port CCD

For example

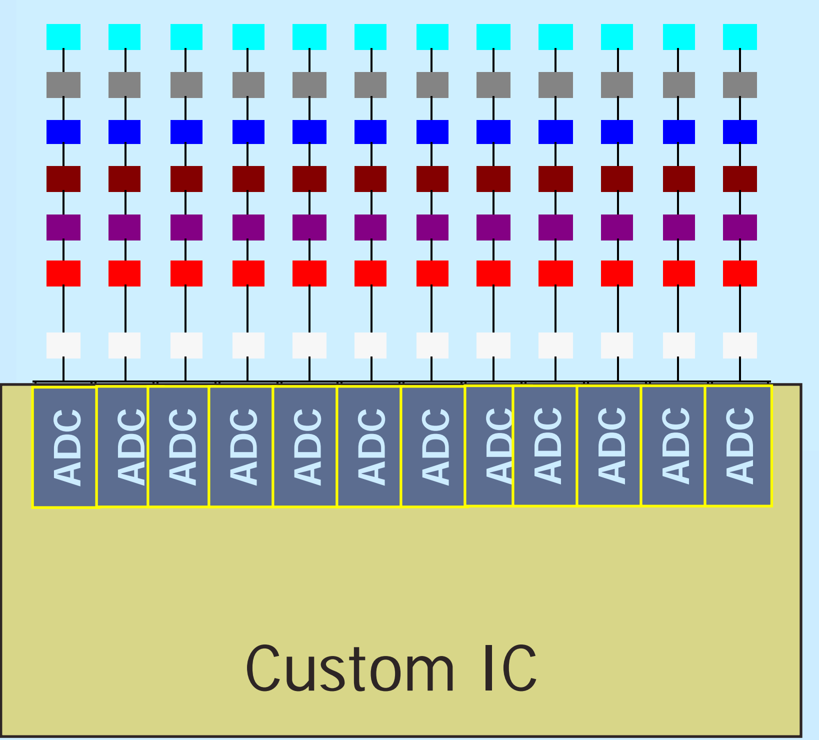


- Fairchild 456
- 512 x 512 x 8.7 μm pixel (19% FF)
- Interline transfer / 32 ports
- 1000 fps = 250 MPix/s

- On-chip current sources for 3-stage output ⇒ 2.5 Watts

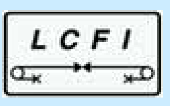
At some point, adding more ADC ports becomes a connection nightmare → integrated circuit solution needed.

Fully column-parallel

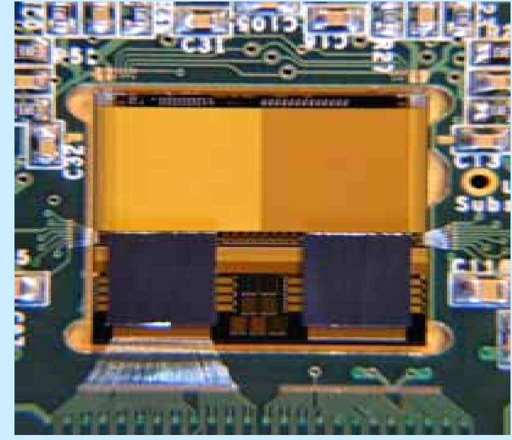


- 1 ADC/column
- Bump bonding required
- No source-follower

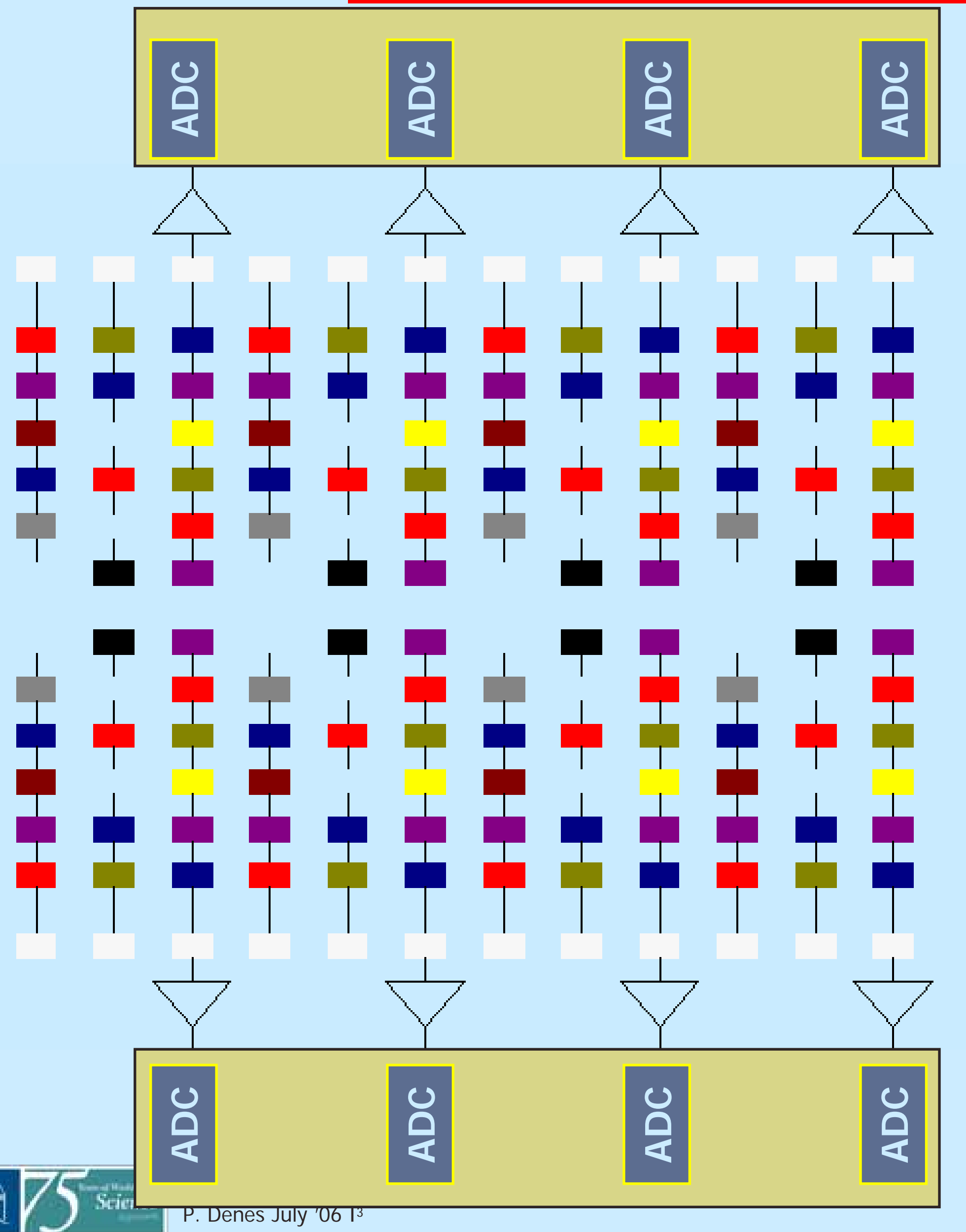
- Example – developments for ILC Vertex Detector
  - *50 MHz column readout*
  - *4-5 bits dynamic range*



RAL et al.



(Almost) Column Parallel CCDs



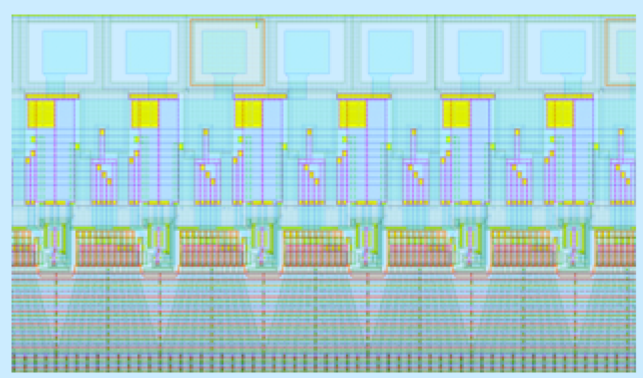
Problem

CCDs are the ubiquitous imagers for synchrotron radiation applications, but in many cases $T_{INT} << T_{RO}$

Solution chosen

- Speed increased by N_{PORTS}
- N_H *large* enough to minimize the number of ADCs needed
- N_H *small* enough to ensure fast readout
- Wire bonding still possible

Prototype – 480 x 480 x 30 μm pixels



- Constant area taper
- 10 pixels/SR
  - *300 μm output pitch*
- Metal strapped
- Thick "LBL CCD"

fCRIC – CMOS 0.25 μm

LDRD

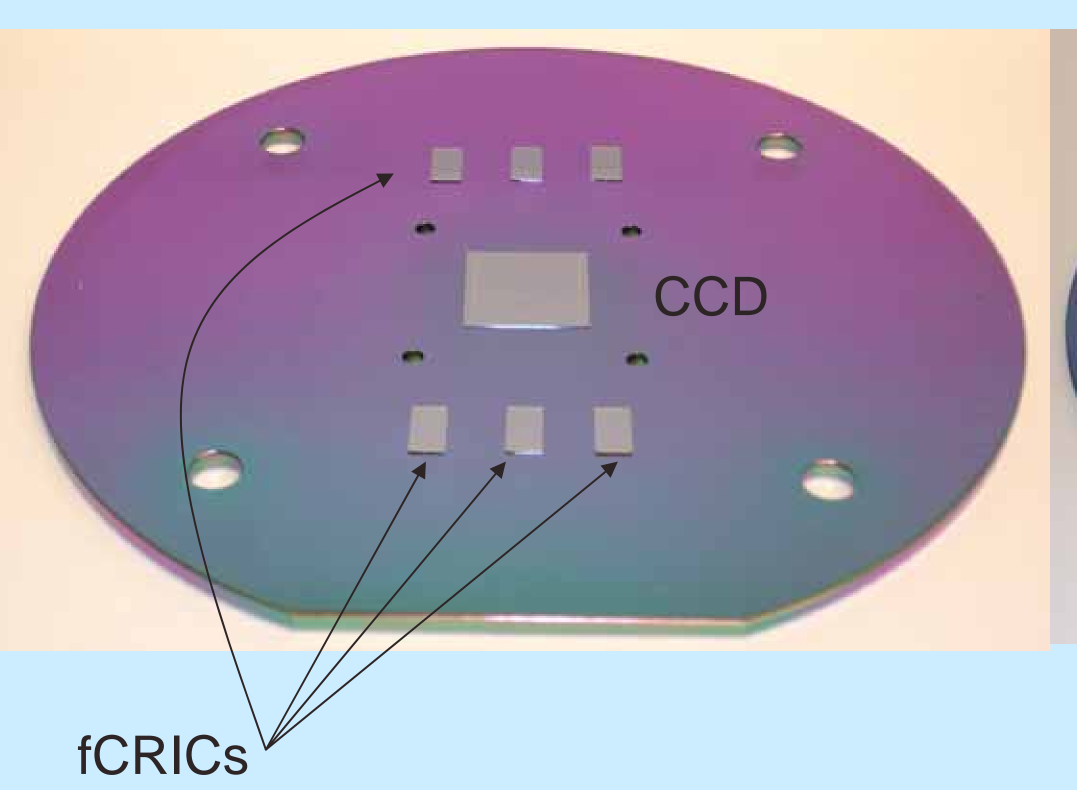
16xFE

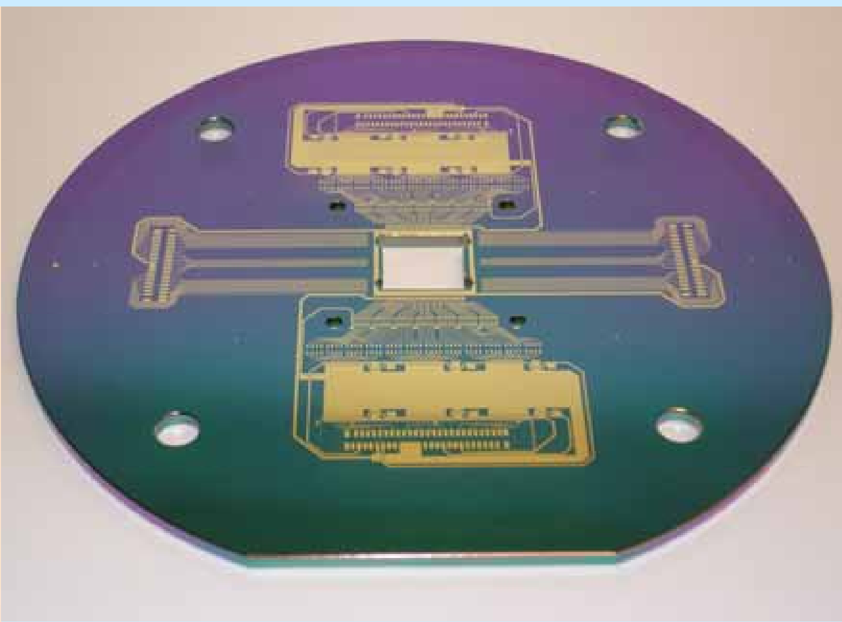
16xADC

Digital Control and I/F

All Mounted on a 6″ Si Substrate

“Silicon is a good CTE match to silicon”



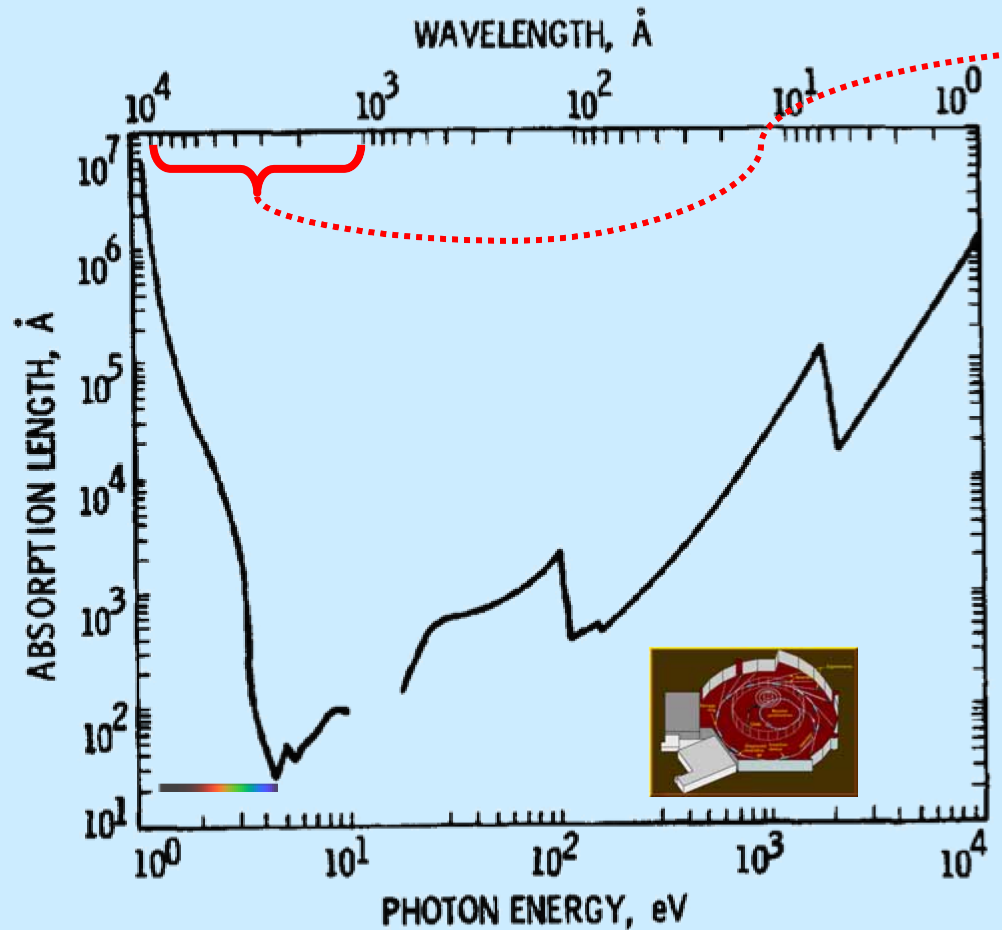


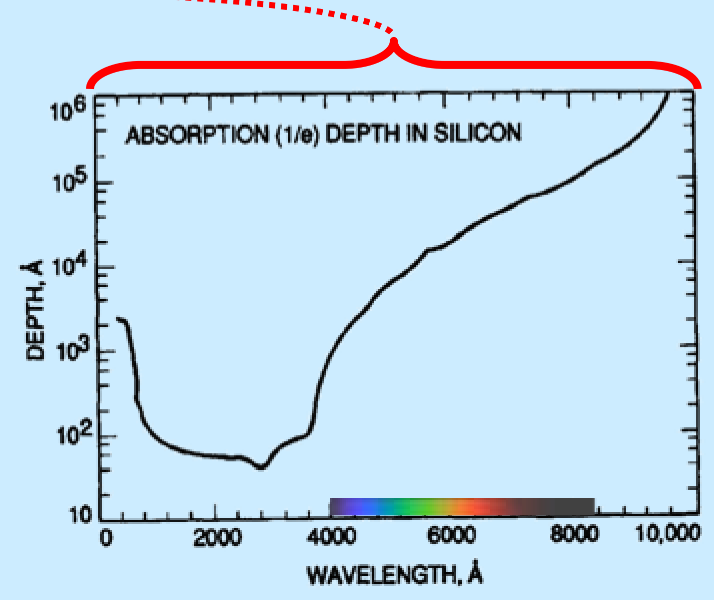
Fast CCD Camera Specifications

Detection	GdO_2S:Tb phosphor – or – direct
CCD Well depth	$>10^6$ e^- (30 µm pixel)
Nominal rate	400 fps (480 x 480, "zero integration")
Sensitivity at nominal rate	3.5 µV/e^-
FS at nominal rate	128k e^-
Noise at nominal rate	<10 e^-

Conversion gain fixed by CCD and integration time. Larger FS possible with shorter integration time.

Absorption in Si





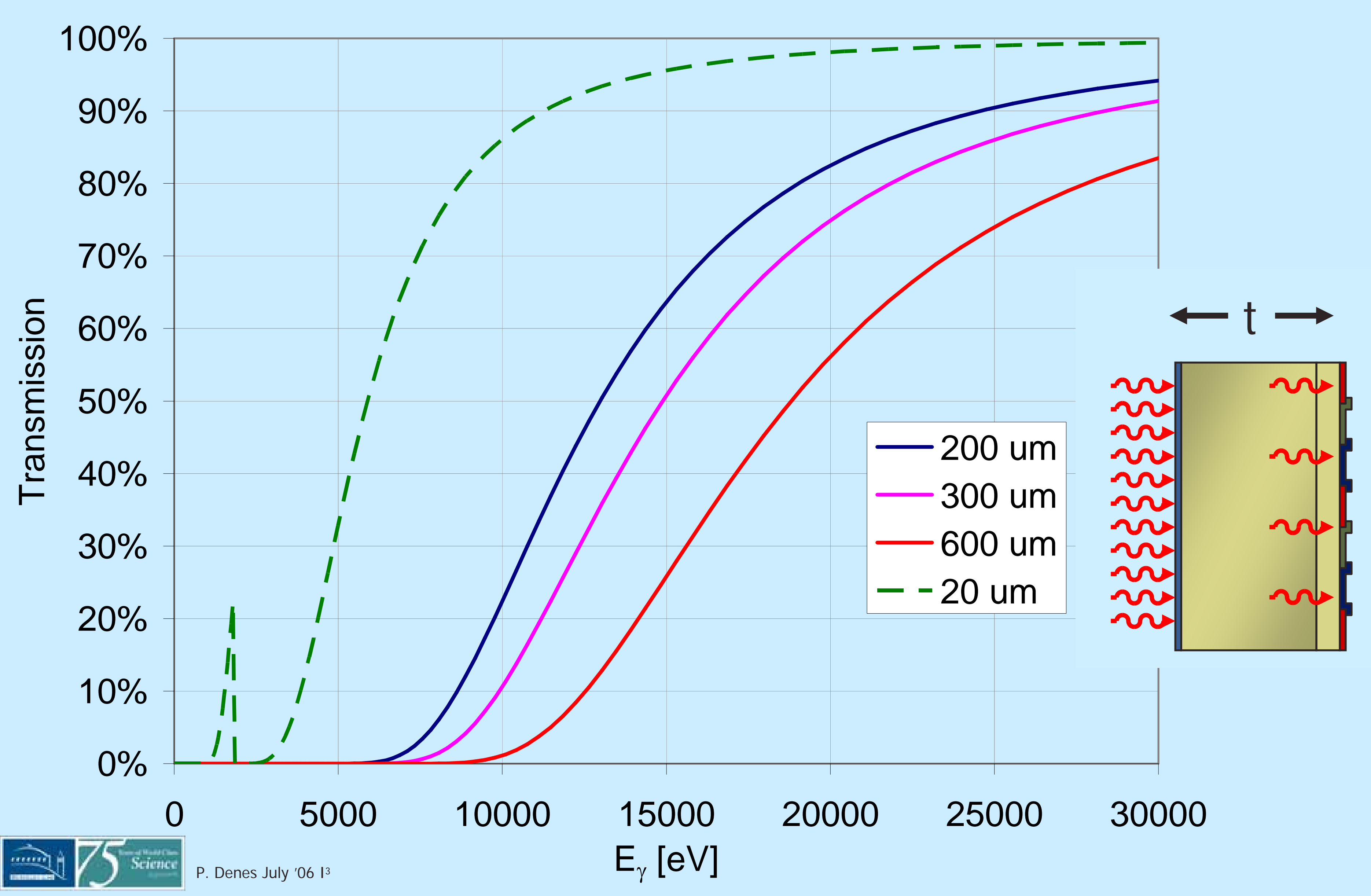
Ignoring reflection …

Visible light or x-rays:
4-5 orders of magnitude

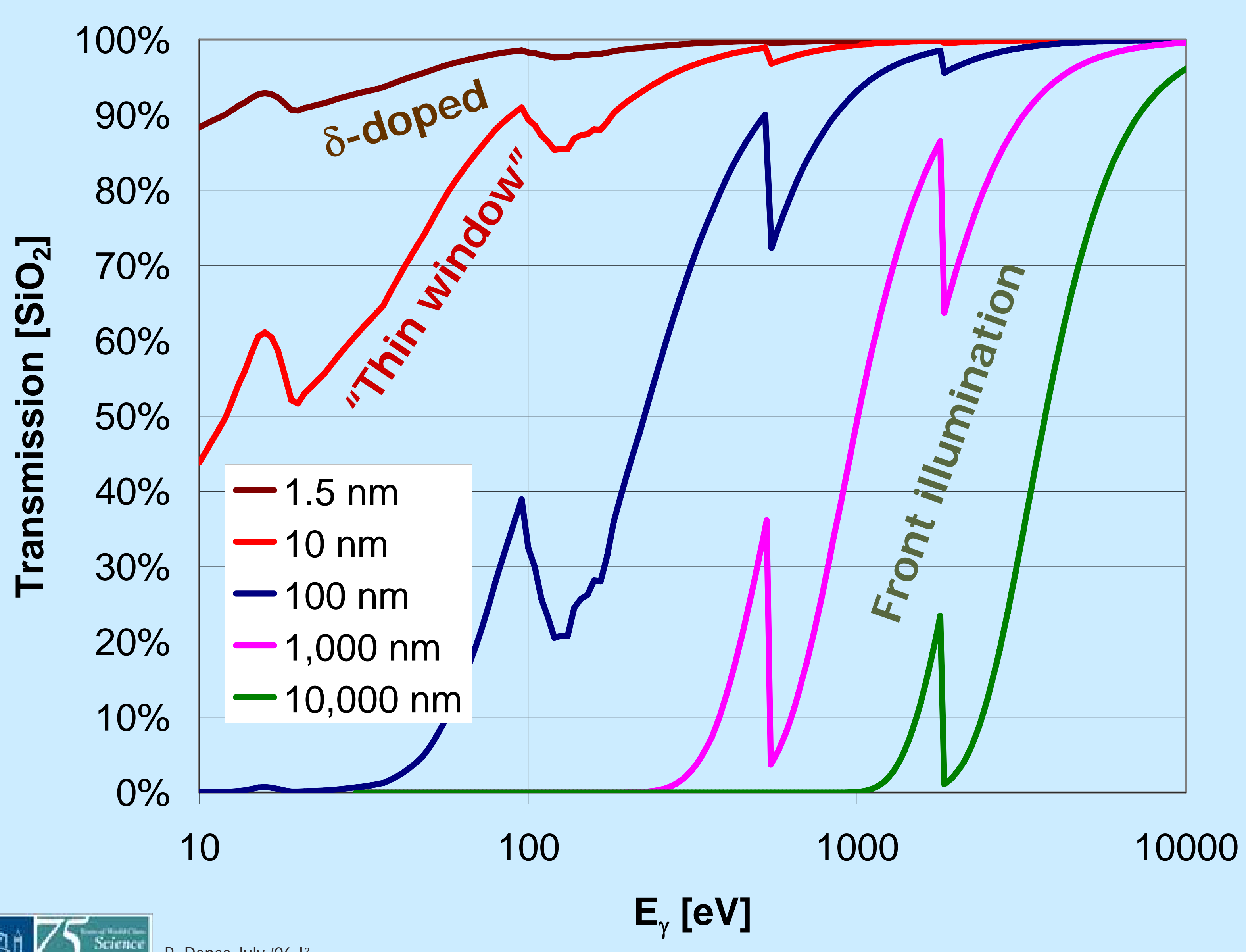
Bandgap of Si at 300K = 1.1 eV
→ pure Si transparent for $\lambda > 1.1\ \mu m$

From Janesick

Thick Silicon for x-rays

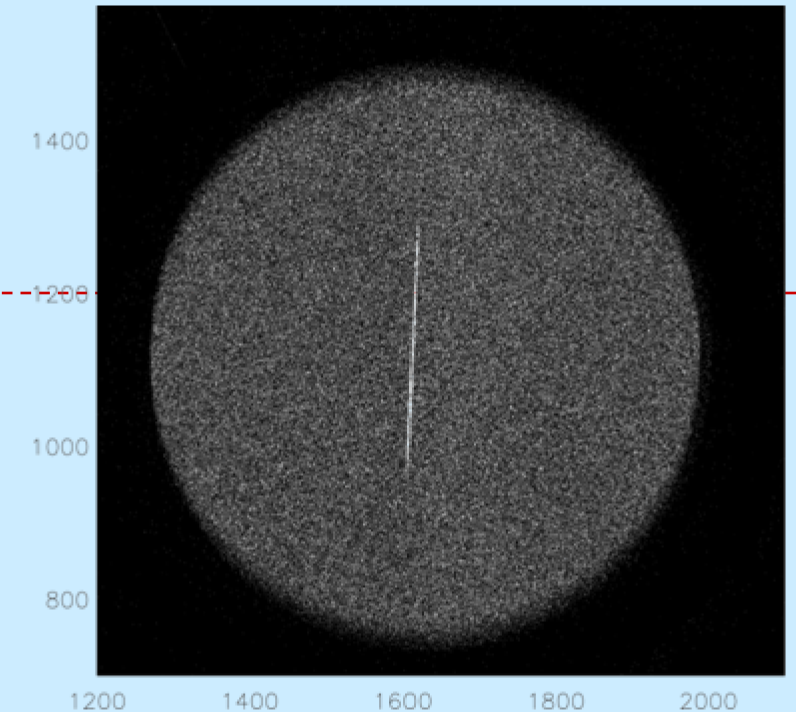


Back-illumination preferred

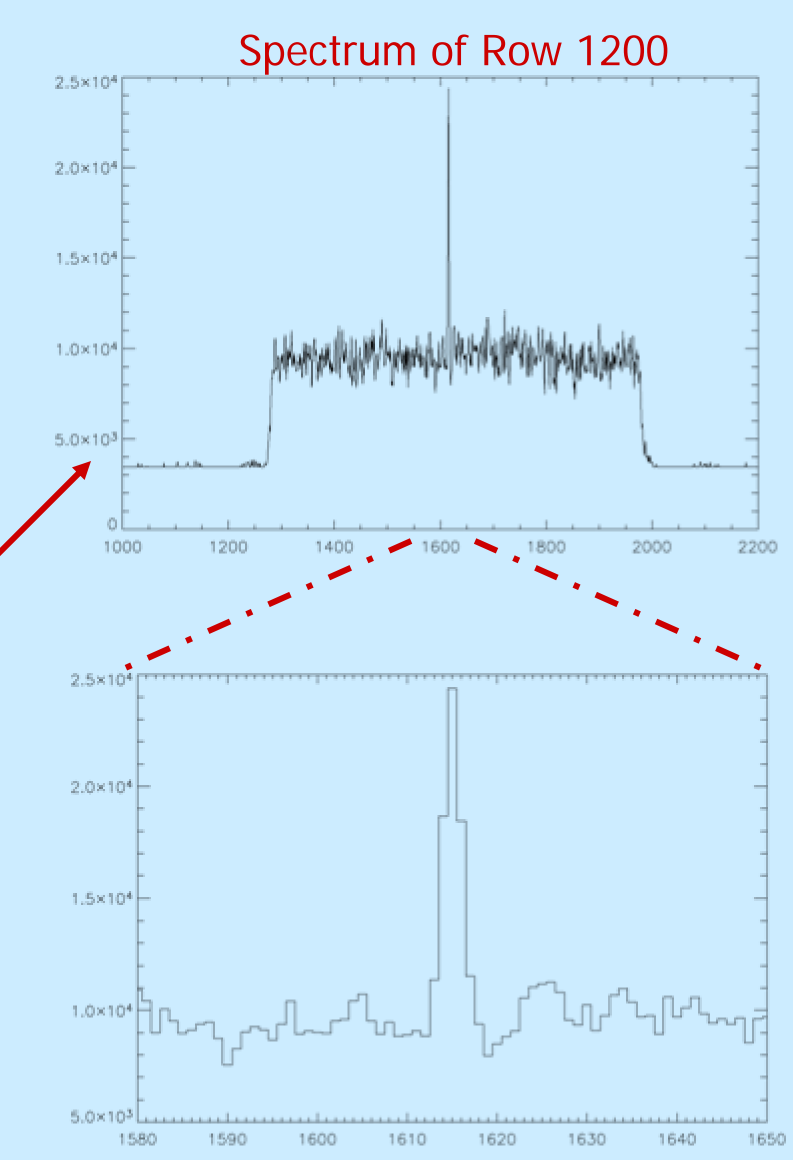


1st x-ray images in LBNL CCD

3,512 x 3,512 x 10.5μm pixel CCD
200 μm thick
Cu anode, 140K, 70 kHz

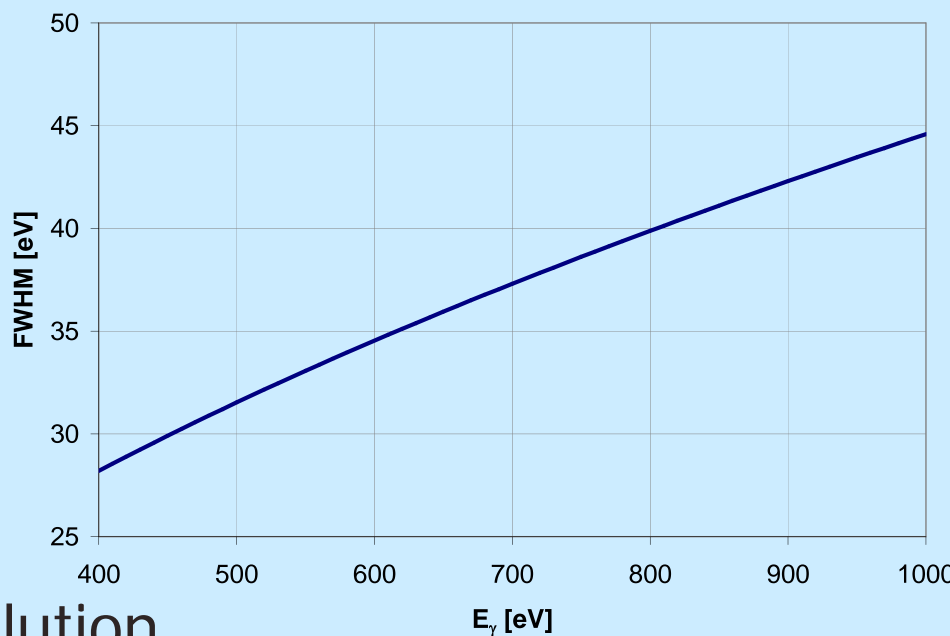


5 μm slit in semi-transparent stainless steel



x-rays in CCDs

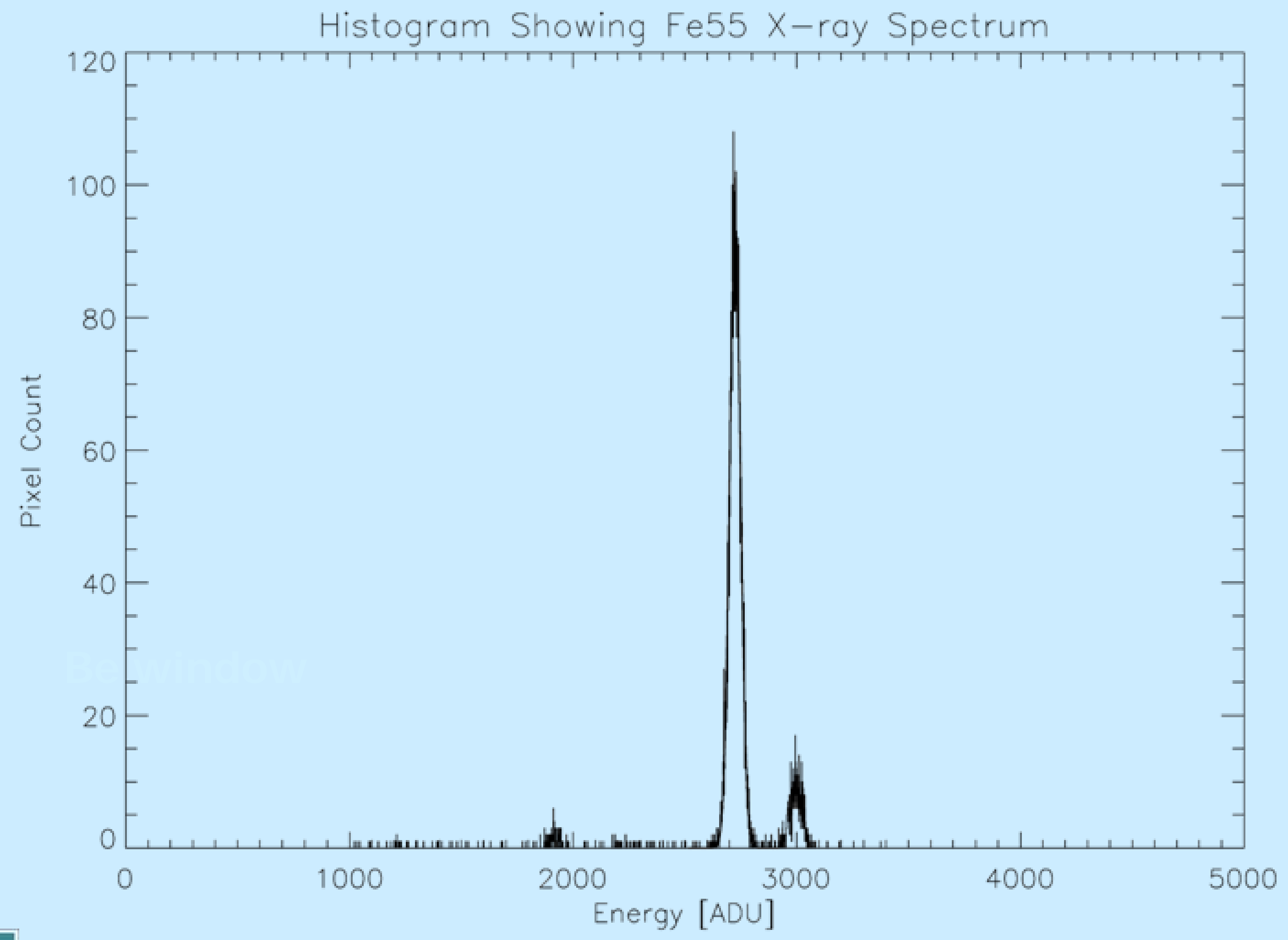
Intrinsic resolution in Si



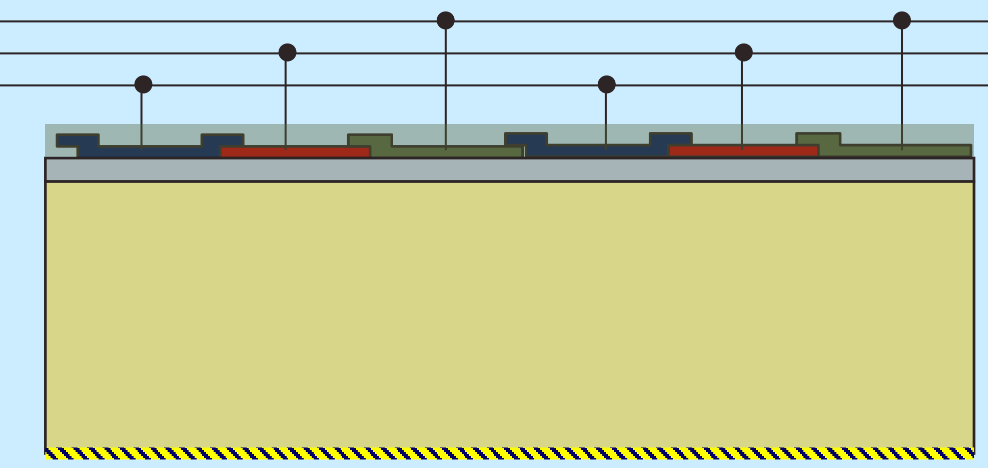
- Excellent spectroscopic resolution
- But only if not piled-up – low rate or fast readout
- $N_{\gamma,MAX}$ = Well Depth / (E_γ /3.6 eV)
  - *<1000*
  - *⇒ 9-10 bit ADC OK*
- Would really profit from high-speed readout as S/N is so high

650 μm thick CCD

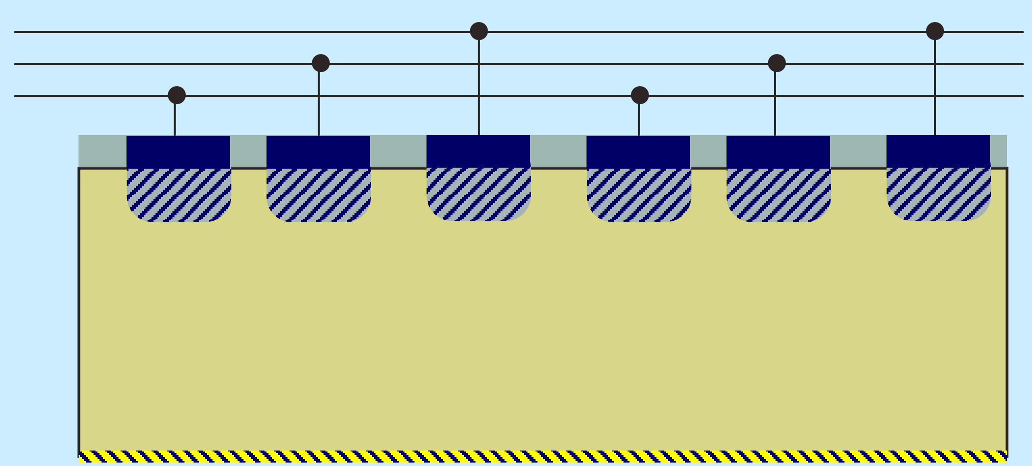
^{55}Fe K_{α} and K_{β}. Resolution ~ 126 eV at 5.6 keV



pn-CCD

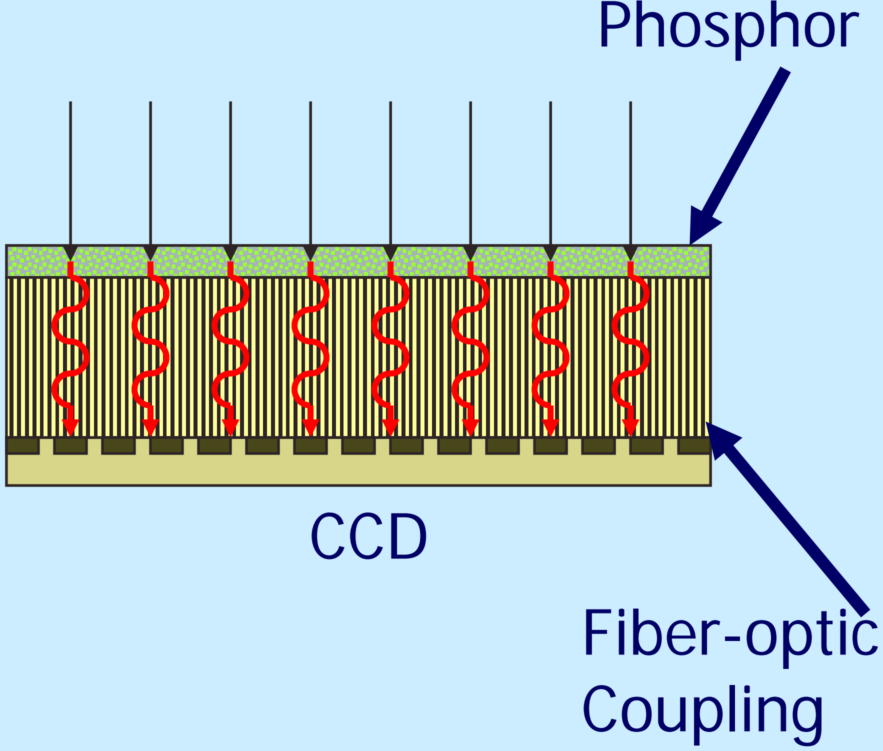


LBL CCD



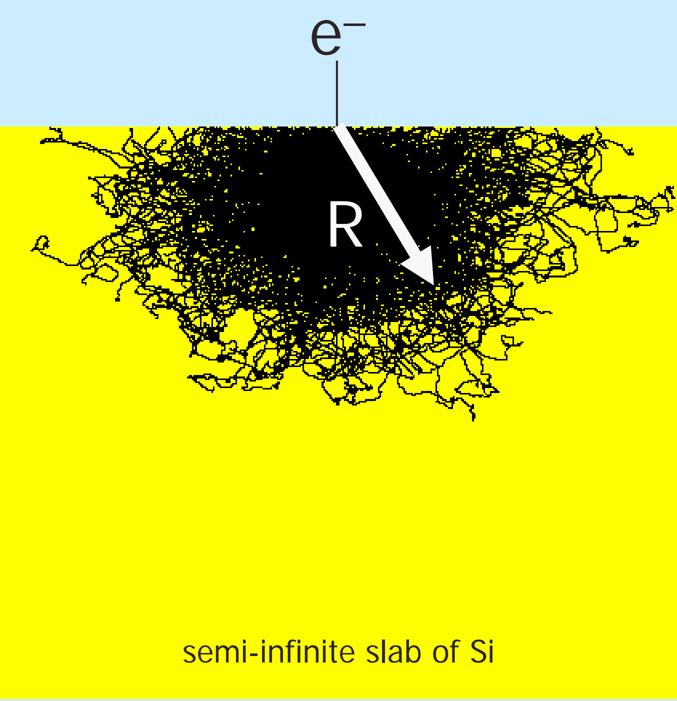
pn-CCD (MPI, …)
(Gatti, Rehak, Struder …)

Electrons



EM Detector

The Problem:

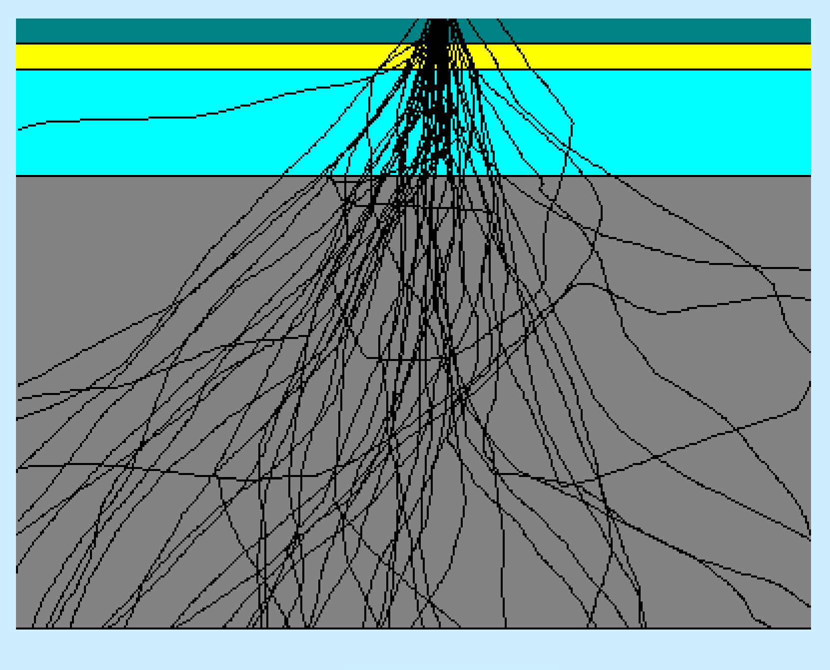


300 keV, 1 mm

R [μm] ~ E [keV]

The Solution:

300 keV e⁻



4 μm SiO_2
2 μm Al
2 μm SiO_2
8 μm
active Si

Inactive Si

50 μm total

40 μm

Optical Active Pixel

SiO_2

Si

Active Area

Fill Factor = Active / Total area

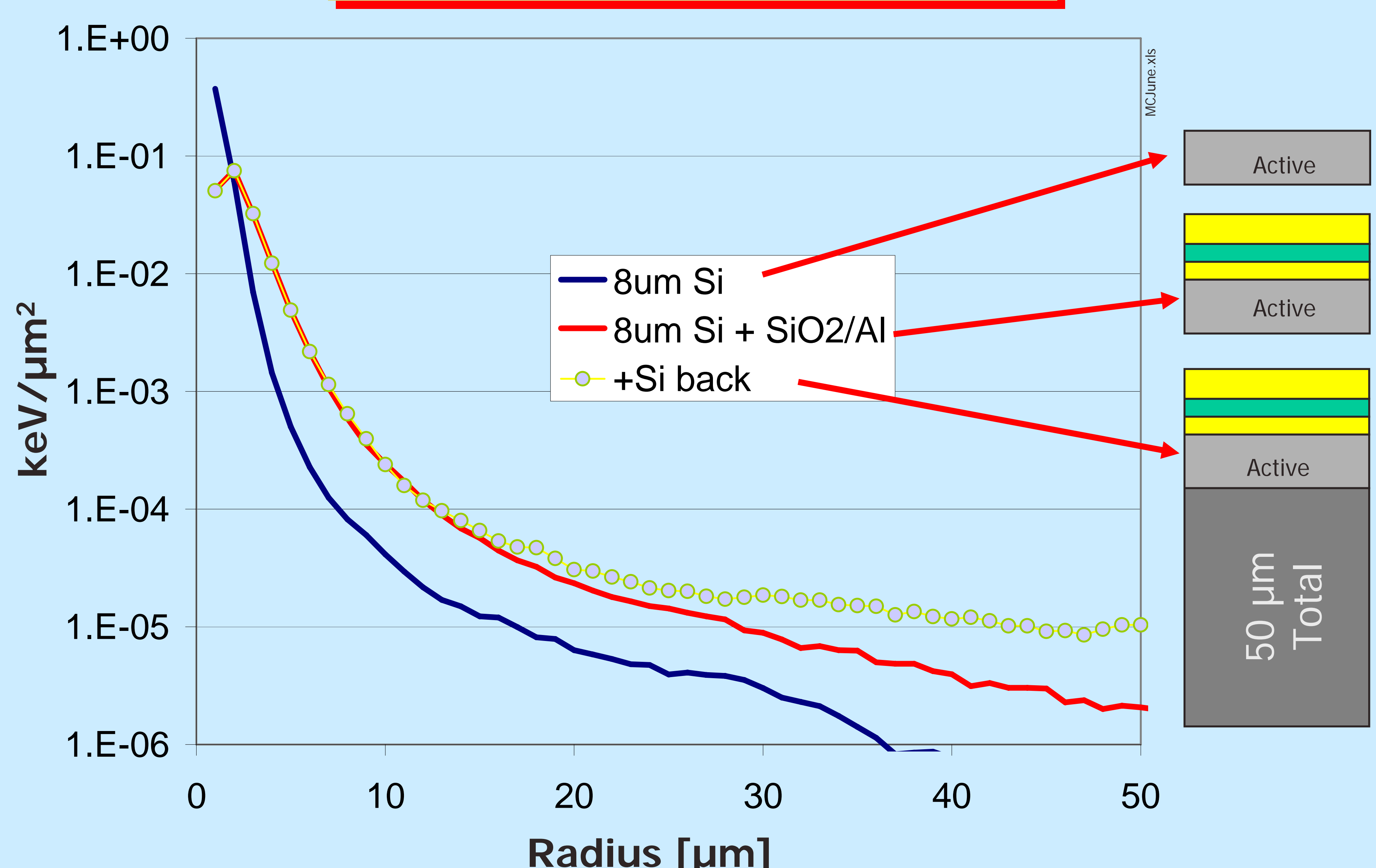
EM Active Pixel

SiO_2

Si

Fill Factor = 100%

Radial Distribution [300 keV]



50 µm Si thickness

Image of Beam Stop (200 keV)

PSF visibly < 10 μm

CMOS Imager

FILM

25 μm

10 μm Pixels

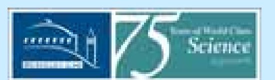
20 μm Pixels

40 μm Pixels

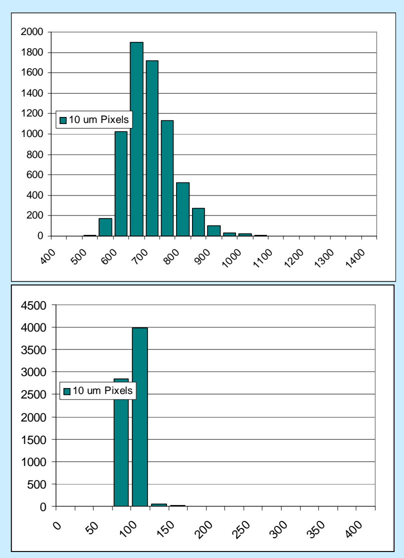
Noise limited – no cooling

Test Chip in AMS C35O

Beam stop on 200CX Microscope at NCEM



Monolithic Imagers for EM



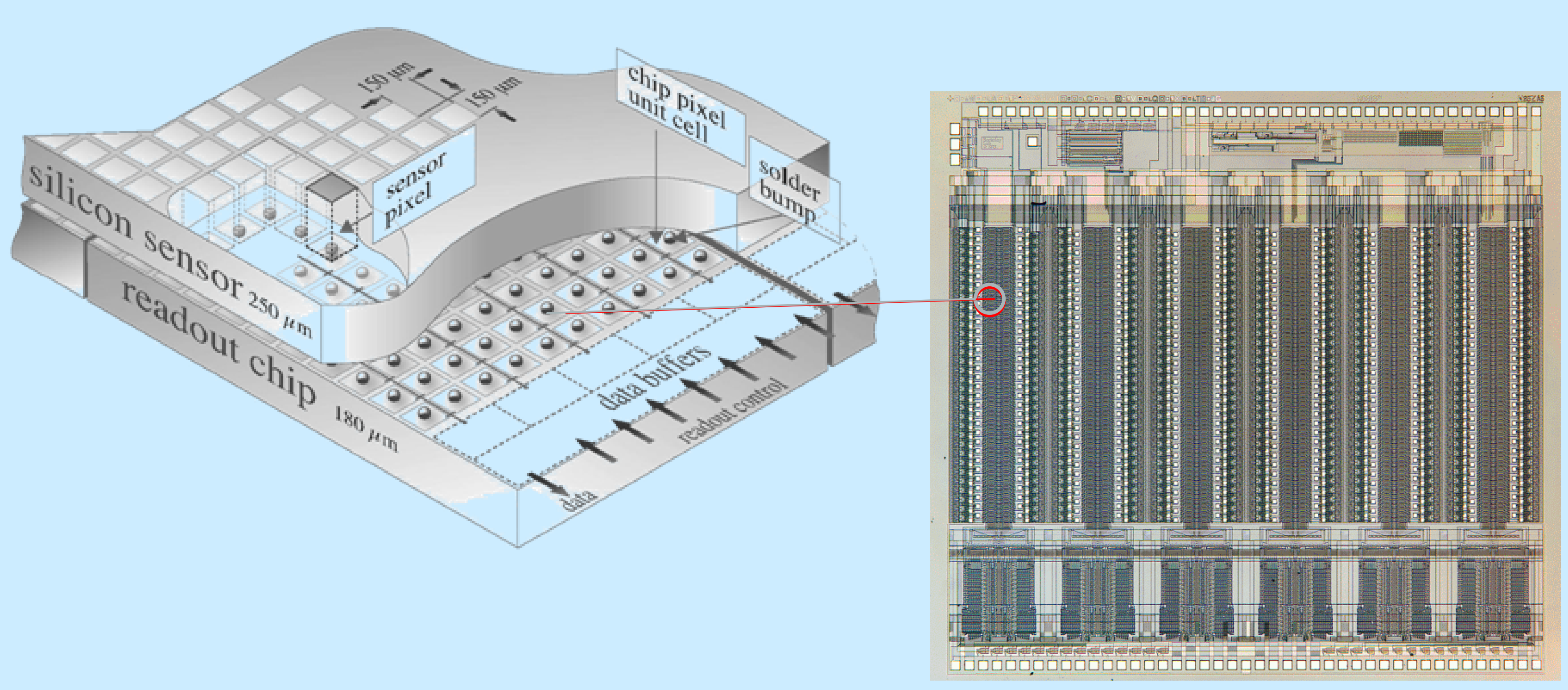
Signal:
25 mV/e^-
(200 keV)

Noise
3.0 mV

- **Single electron sensitivity** (SNR 8.3 here, will improve with cooling)
- ~μm PSF
- High-speed readout (dynamics)

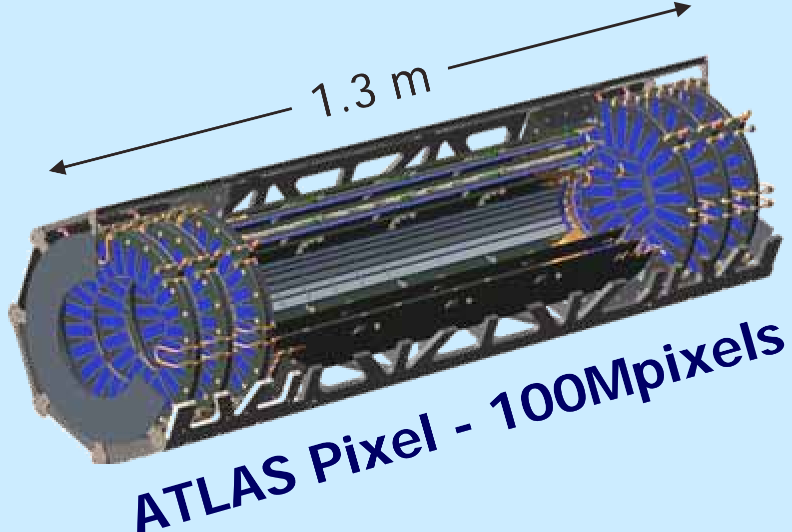
Next step: 3k x 3k high-sensitivity (bio) chip

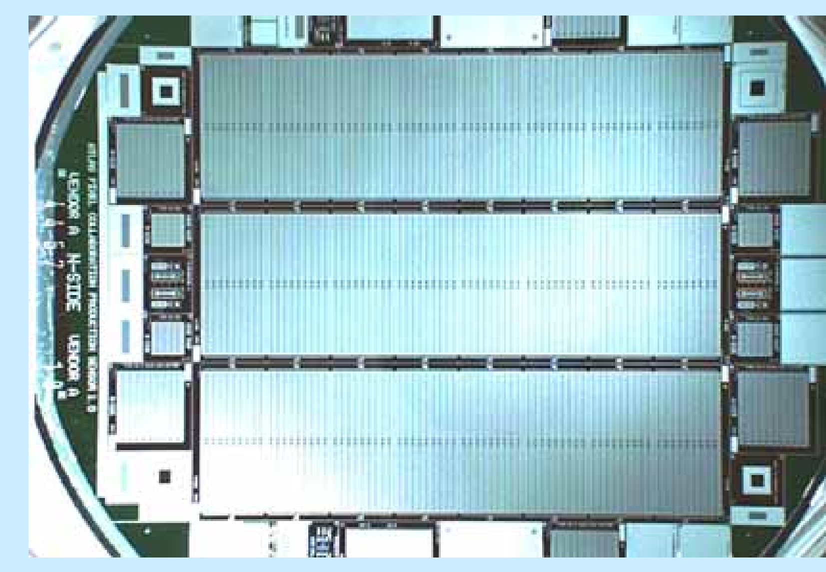
Hybrid Pixel Detectors



Advantage over monolithic detectors: much more sophisticated electronics per pixel

e.g. ATLAS Pixel Detector

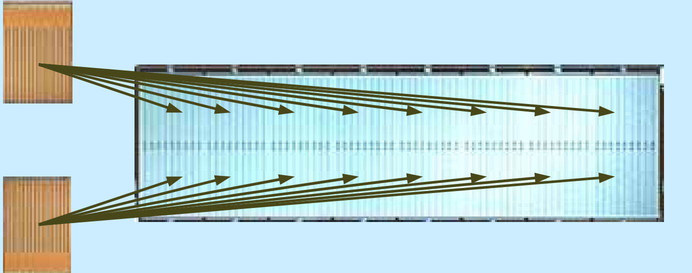


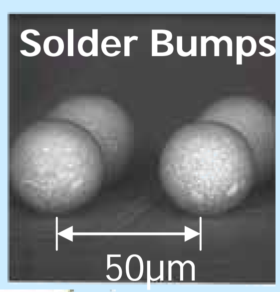


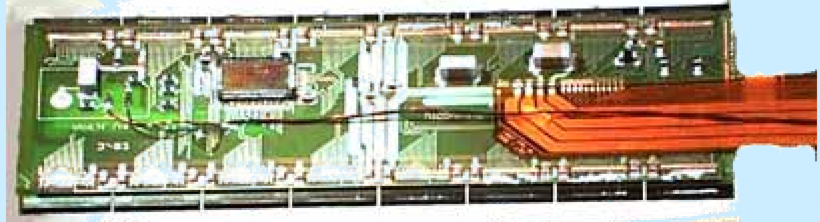
Readout ICs

18x160 pixels

Readout





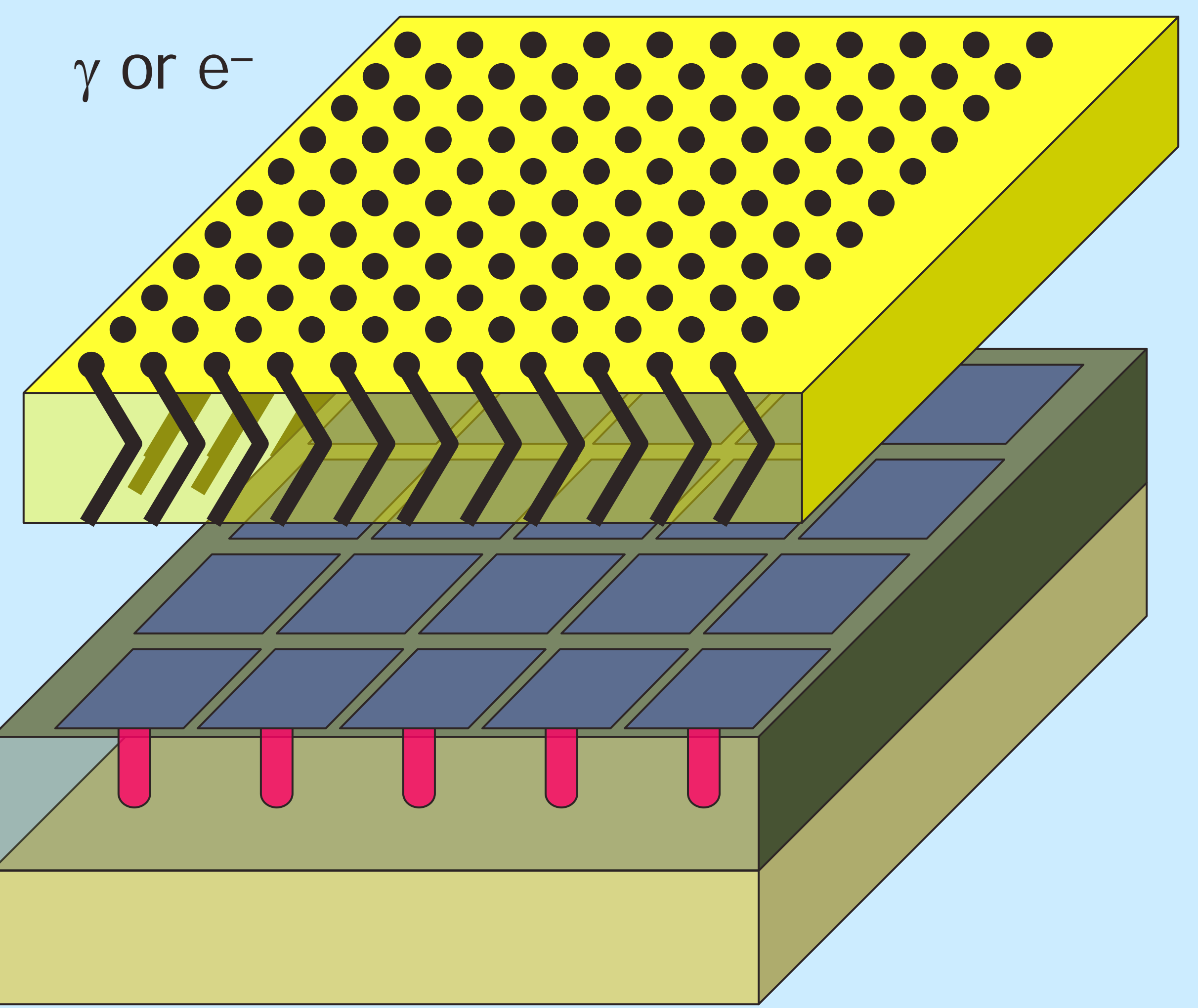


A "module" is 1 sensor with 2x8 bump-bonded chips

☺ and ☹ of Hybrid Pixels

- Interconnect – generally implies relatively large pixels
- Large pixels can have much more "intelligence"
  - *measure per event (e.g. E, t)*
  - *complex functions (e.g. temporal autocorrelation)*
  - *spectroscopy*
- Large pixels make large pixel-count detectors challenging (c.f. ATLAS pixel detector)

Another kind of Hybrid Pixel



MCP

Readout chip or CCD (esp. LBL CCD)

MCP – large electron multiplication gain

For e⁻ Maybe LBL CCD and no MCP

"Thin"

Detected electrons / Incident electrons

300
250
200
150
100
50
0

SEM Measurements

UHV Measurements

Delta-doped CCD

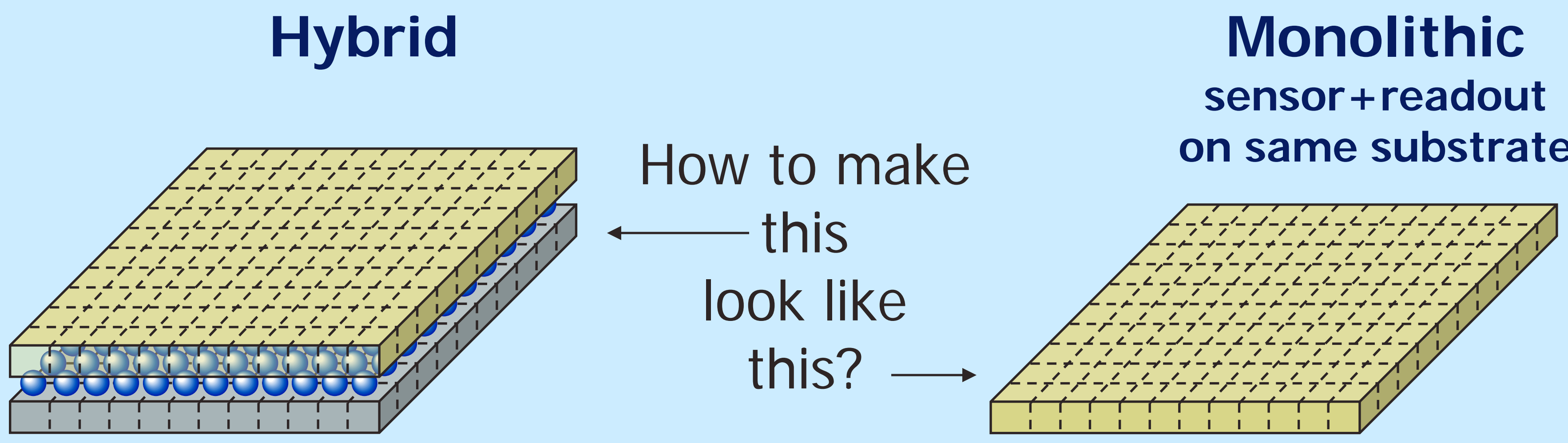
Untreated CCD

0 200 400 600 800 1000 1200

Electron Beam Energy (eV)

Nikzad et al SPIE 97

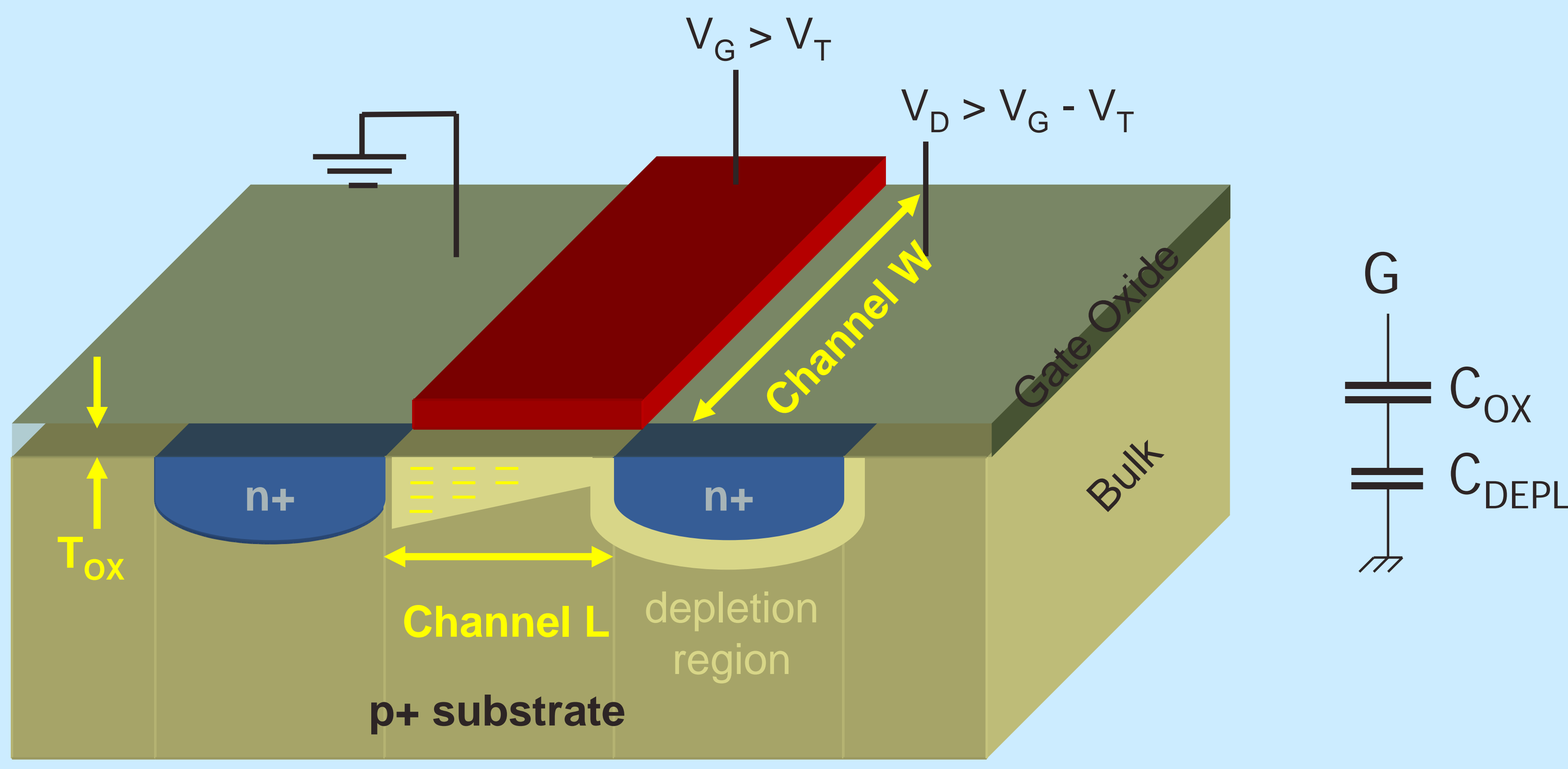
Monolithic Hybrid Detectors?



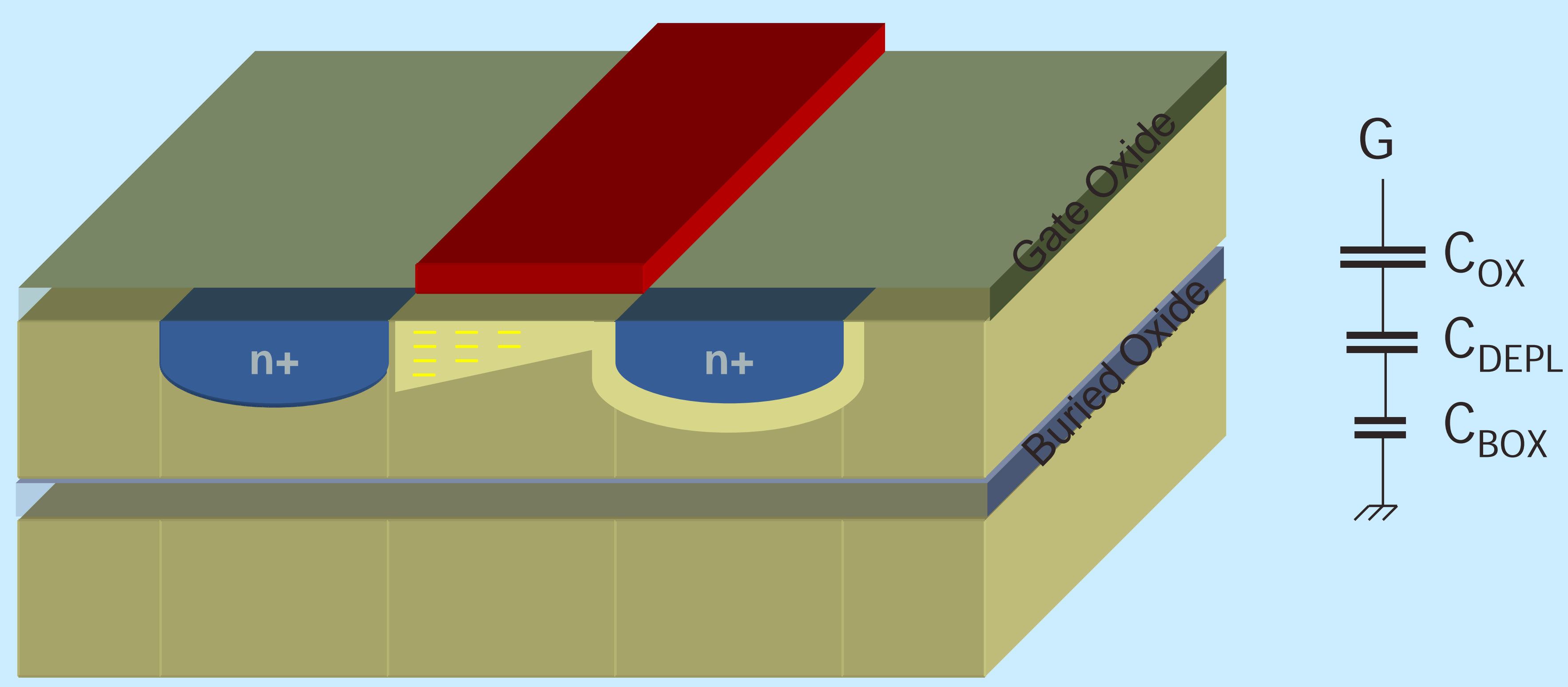
Bump-bonding works, but is “R&D” for pitch < ~200 μm and is best done “wafer scale”

(Bulk) MOS Transistor

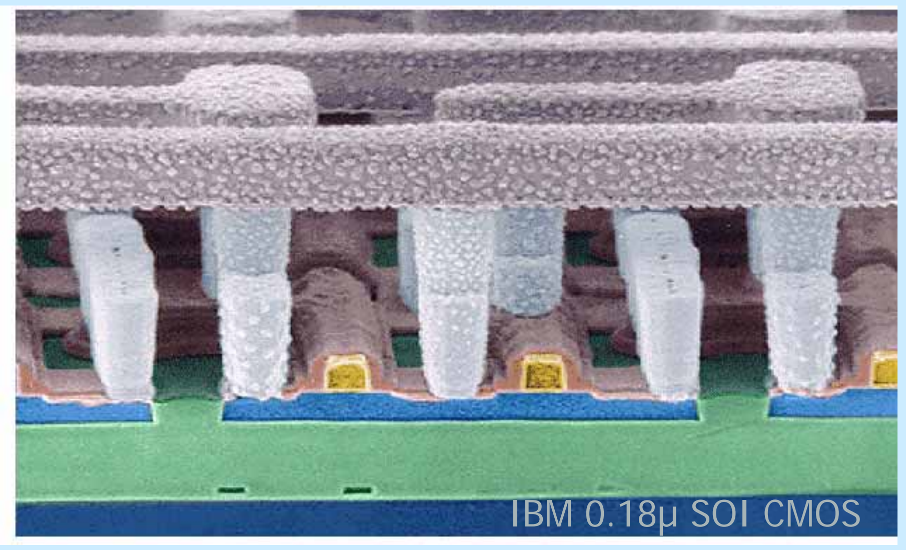
Saturation – $V_G > V_T$, $V_D > V_G - V_T$



Silicon-On-Insulator



Advantages of SOI



Metal Interconnect

Metal Interconnect

Polysilicon gate

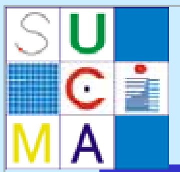
Box

- Reduces substrate coupling
  - *higher speeds*
  - *lower power*

For lowest power, want a high-resistivity substrate

- Improves radiation hardness
  - *no latch-up through substrate*
  - *complete di-electric isolation possible (with trench isolation)*

"Artisanal" SOI Pixel



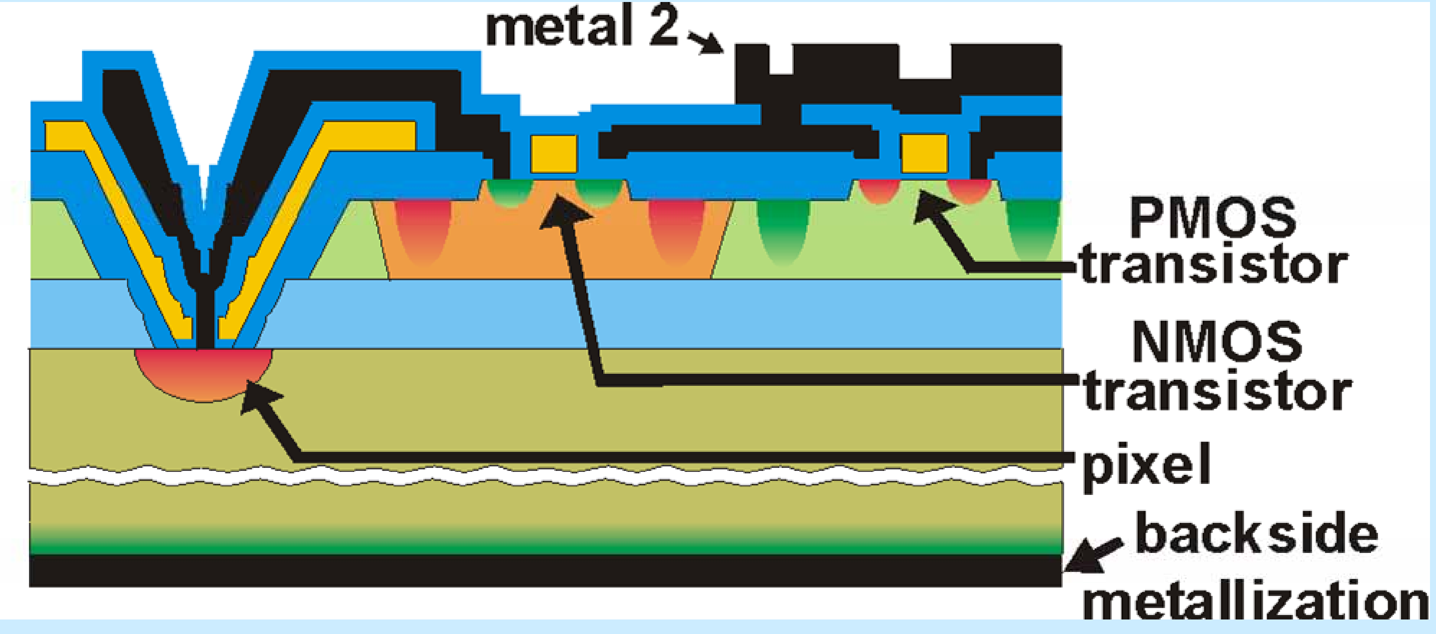
SOI Imager – Main Concept

Detector → handle wafer

- High resistive
- 300 μm thick

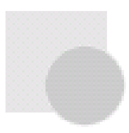
Electronics → device layer

- Low resistive
- 1.5 μm thick



Saved by the Watch?

- Commercial SOI on high-resistivity silicon (without contact)
- 0.15 μm CMOS
- Dream process?
  - *Almost – see next page*
- KEK HEP group working on SOI pixels for particle tracking



Fully-depleted Type SOI Device Enabling an Ultra Low-power Solar Radio Wristwatch

Masafumi Nagaya

On May 19, 2002, Casio Computer Co., Ltd. launched sales of the Tool Concept PRG-50, a new addition to its Pro Trek series of "outdoor" watches which provide compass direction and altitude readings. Moreover, these watches run on solar power, so there is no need to worry about battery replacement. (See Fig. 1.)

The Tool Concept PRG-50 employs a low-power LSI IC designed for watches which includes an Oki Electric fully-depleted type SOI (Silicon-On-Insulator) CMOS device (FDSOI-CMOS)[1,2,3] for greatly reduced current consumption. Thanks to the high-performance solar drive system built into this chip, plus a solar panel that provides highly efficient power generation and a high-storage-capacity battery, this watch is able to use solar power to operate direction and altitude functions-features not found in conventional solar watches. As such, the Tool Concept PRG-50 is a high-performance outdoor watch that hikers and trekkers can trust, without any worries about low batteries.

The following[4] describes how the fully-depleted type SOI CMOS device (FDSOI-CMOS) was developed for Casio for use as a watch-type LSI IC (product name: ML6126) that boasts the world's lowest current consumption.

Fig. 1 Tool Concept PRG-50

Reducing Current Consumption In LSI ICs for Watches

The push for lower current consumption in Casio's LSI ICs for watches began in earnest around 1997. In addition to meeting the needs for longer watch battery life and reduced environmental impact, Casio was seeking to use thinner button-type batteries to power their watches. Using these button batteries would enable the watch itself to be made thinner and more fashionable.

Conventional IC chips for watches, such as the MSM6118, were rated (in chip-specific electrical characteristics) to consume 1.55 μA of current. Since 1997, current consumption has been successively reduced by circuit design measures, use of the multiple threshold value process, and layout techniques scaled to 1.3 μA (in the MSM6121), then to 0.7 μA (in the MSM6122). (The multiple threshold value process uses at least two different threshold values. Transistors that require only the lower threshold value are designed to use that lower value while other transistors use the higher threshold value, which enables both low leakage current and low-voltage operation.)

In the MSM6122, when the threshold value is at the center of the target value range, the chip's actual current consumption is raised to 0.33 μA, and when the threshold value is at the worst level, the leakage current is increased such that the current rating becomes 0.7 μA. At the same time, even when the threshold value is at the center of the target value range, the charge/discharge current for the crystal oscillator circuit, main clock circuit, and display circuits made it difficult to reduce current consumption. Consequently an FDSOI-CMOS process using fully-depleted type SOI was adopted as a solution for reducing current consumption.

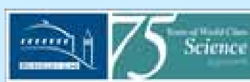
Advantages of the FDSOI-CMOS Process

Listed below are some of the advantages of using the FDSOI-CMOS process as a means of reducing current consumption in LSI ICs for watches.

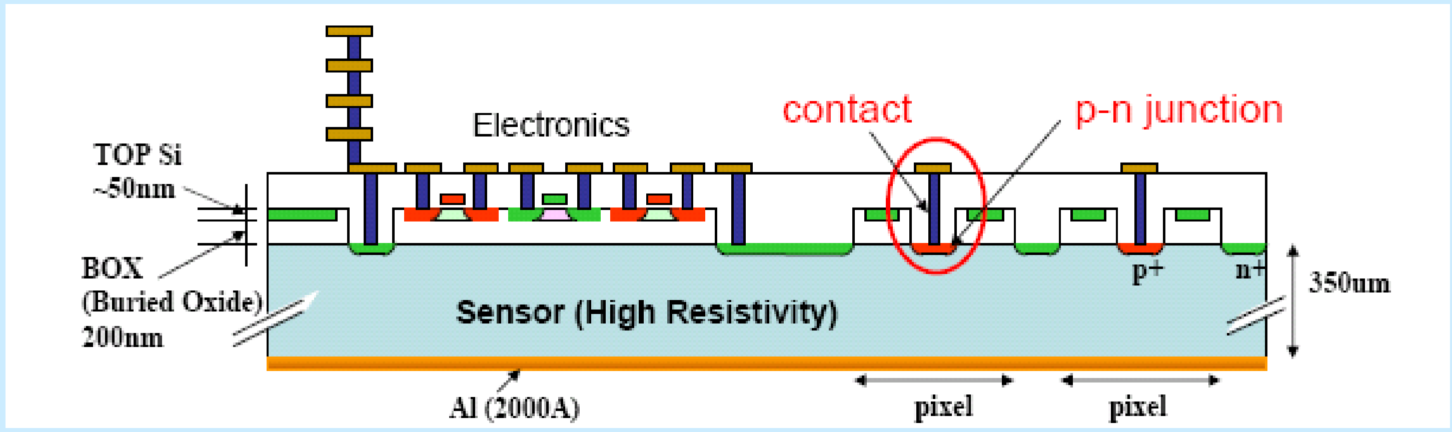
① Low parasitic capacitance
② The threshold voltage can be set lower than in bulk devices.

These advantages are further described below.

The junction capacitance that is a component of a MOS transistor's parasitic capacitance is proportional to the junction surface area, and the junction surface area is the sum of the plane and lateral surface areas of the source/drain diffusion layer. In FDSOI-CMOS devices, the bottom surface is connected to a thick oxide film (embedded oxide film), which greatly reduces capacitance[5]. As for the lateral areas, only the parts that face channels are affected, and the overall capacitance is reduced to about one tenth that of the source/drain junction area in conventional bulk devices. Accordingly, the capacitance subject to load charges and discharges is reduced, making for lower current consumption. For example, charge/discharge current for the watch's LCD driver block, step-up, and step-down circuits can be

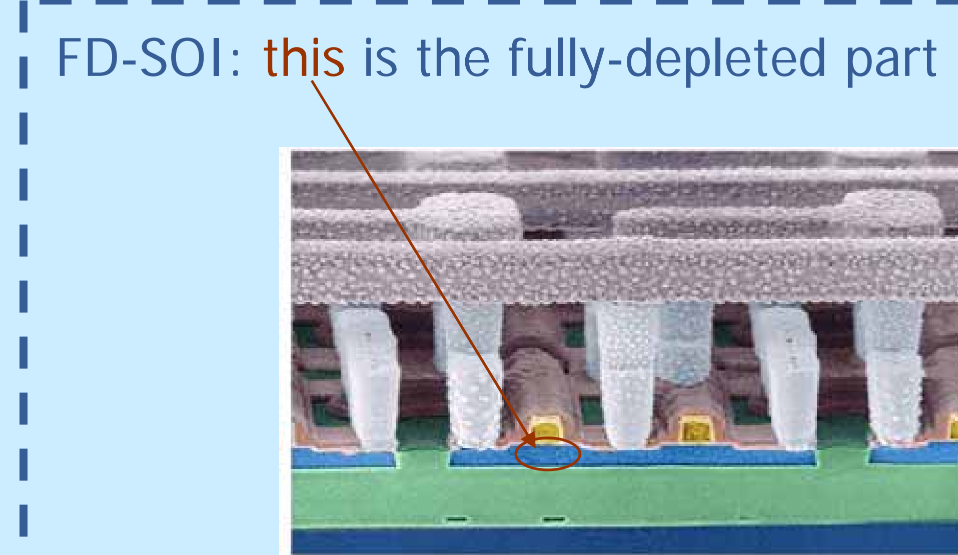


Modified Version of Oki 0.15 μm FD-SOI

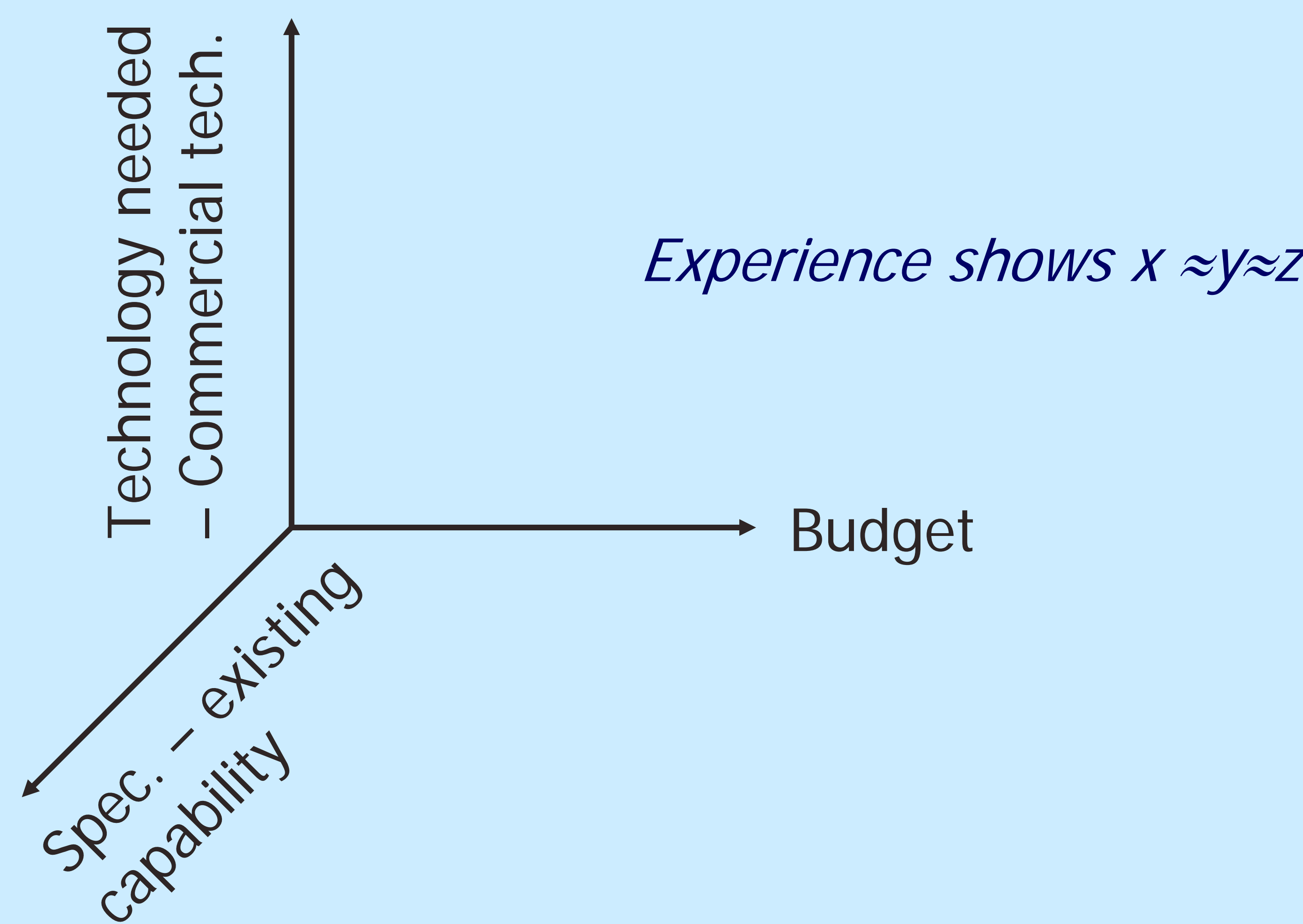


- 3 extra masks needed: (p+ and n+ implants and contact)
- Metal back-side contact
- "quasi commercial"

FD-SOI: this is the fully-depleted part

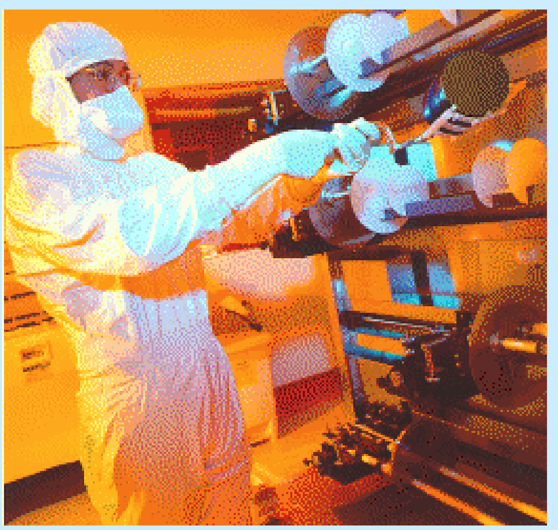


Caveat emptor



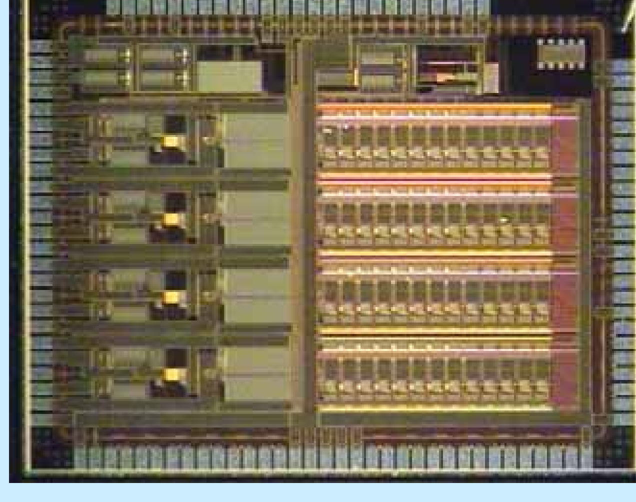
Experience shows x ≈y≈z

Many Interesting Challenges – to be solved



Microsystems Lab

Systems Expertise



Unique IC skills

+ materials development (life after Si?)
+ ...
+ (most important) user base

Then: "**You push the button, we do the rest**"

Now: "**We do the rest, you push the button**"