PowerGrid

"A Computation Engine for Large-Scale Electric Networks"

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DOE OE Visualization and Controls Peer Review Meeting

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Project Players

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PJM

Battelle/PNNL

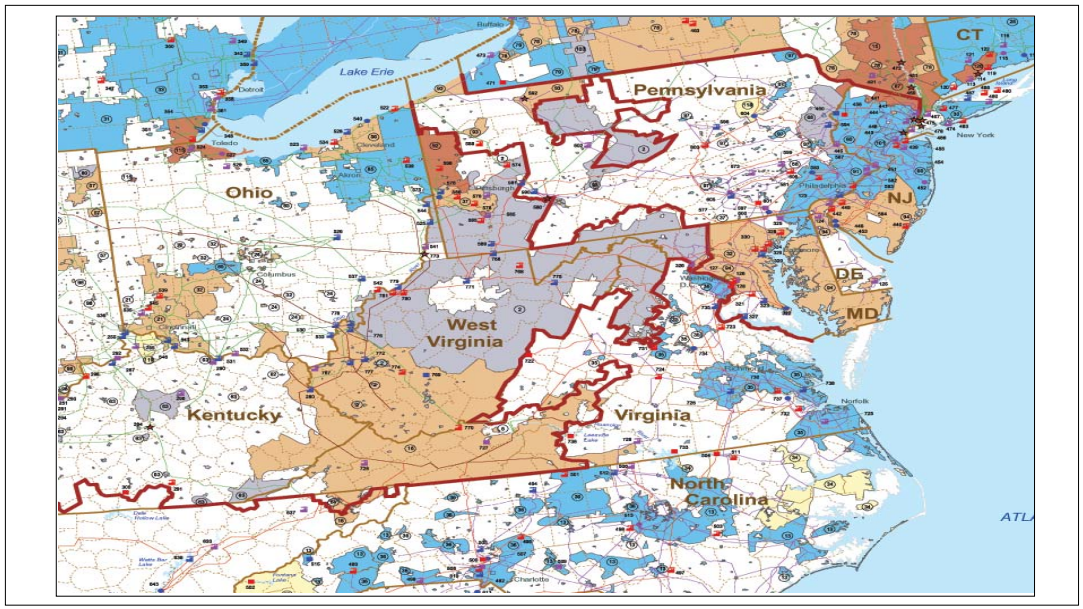
AREVA*

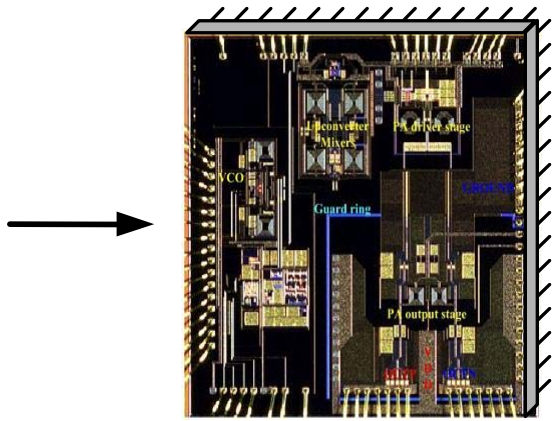
Sandia National Lab*

(*- to commence shortly)

Project Overview

Power Grid Emulation Engine – Power System on a Chip (PSOC)





PSOC

Features of PSOC:

1. Analog emulation of power system
2. Reconfigurable chips
3. Real-time computation of solution

Paths to the Development

We have three stages to fully develop the PowerGrid Simulator:

- Digital Approach
- Analog Approach
- Mixed-signal (analog-digital) Approach

Highlights of Past Year's Effort

- Implementation Studies of the Digital Approach as it relates to:
  - Validation of Model with hardware results
  - Load-flow speedup
- Implementation Studies of the Analog Approach as it relates to:
  - Development of PC-Board Based Emulator
  - Development of Static Power Flow Solver

Short-Term Future Plans

- Perform 6-month Industrial Feasibility Study of All Digital Approach through collaboration with AREVA
- Perform 6-month Industrial Feasibility Study of All Digital Approach through collaboration with Sandia National Labs
- Perform Interdependency Study of both Digital and Analog Approaches
- Enhance RoadMap for Mixed-Signal Approach with PJM

All-Digital Approach

Overview

What do we want to achieve?

Speedup the computation of load flow.

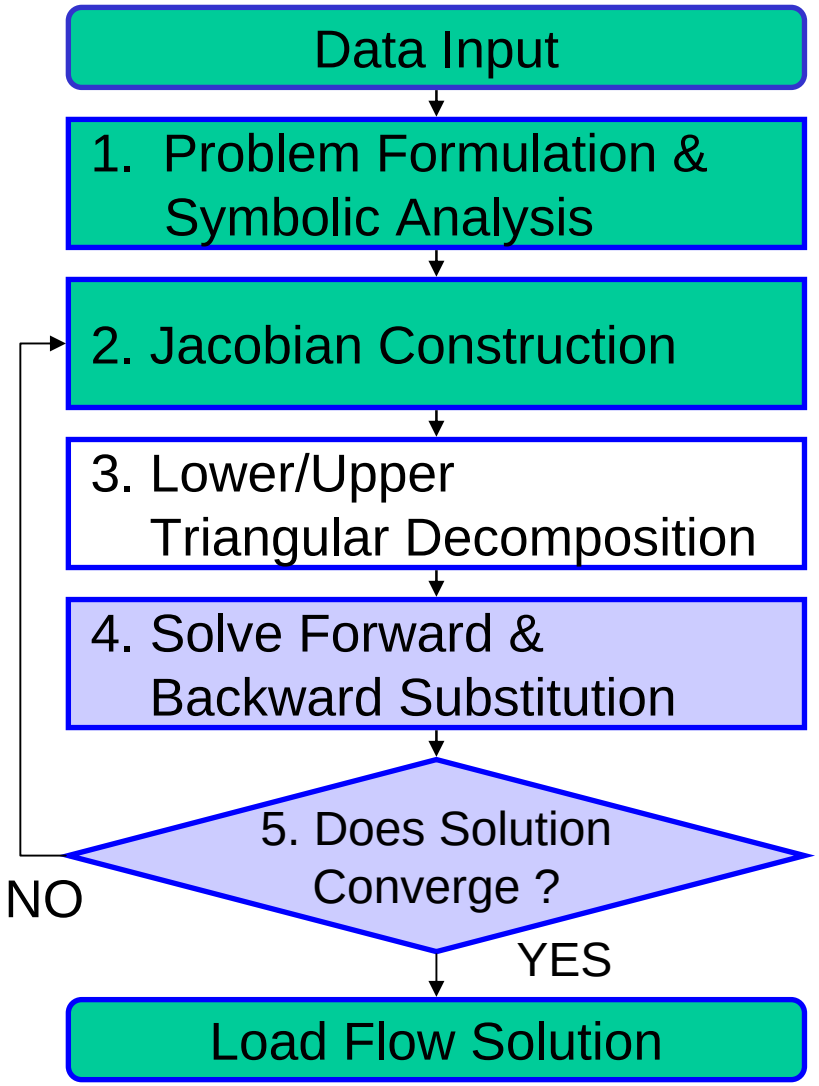
What is our approach?

Intelligent design of application specific hardware which accelerates the most time consuming part of load flow, lower/upper triangular decomposition (LU) , in order to reduce the total computation time.

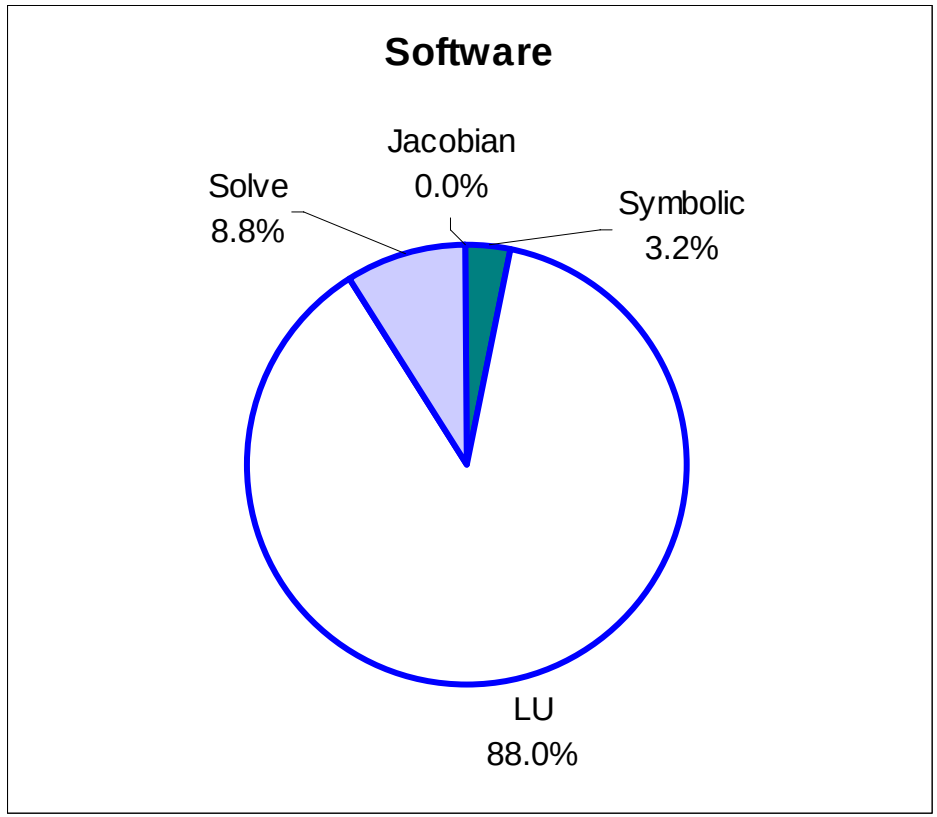
Where are we today?

Prototype of LU hardware has been completed and performance verified for systems up to 1648bus. Order of magnitude speedup in LU computation time is projected, based on clock speed and cycle count, resulting in a speedup of 5-6x for overall load flow computation.

Full AC Load Flow Computation



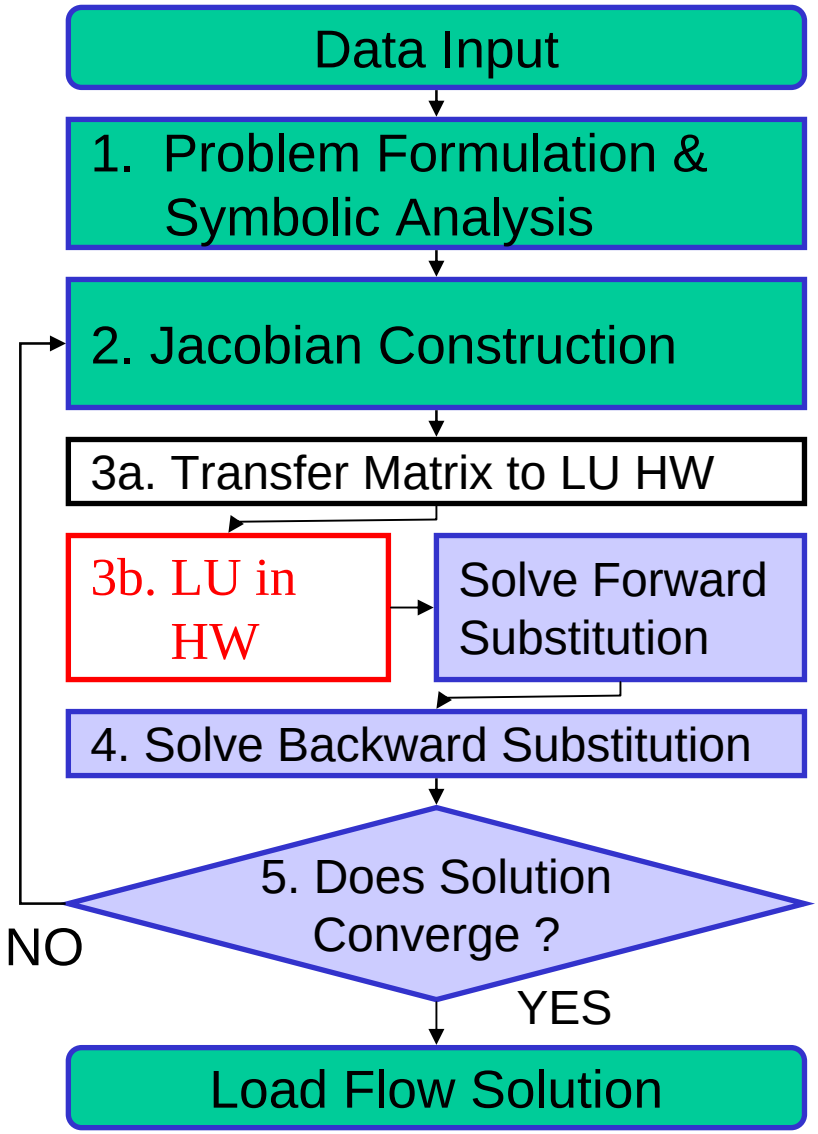
Host Processor (Pentium 4)

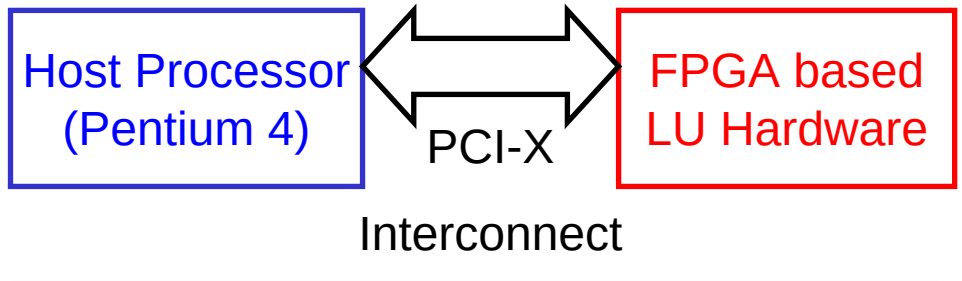


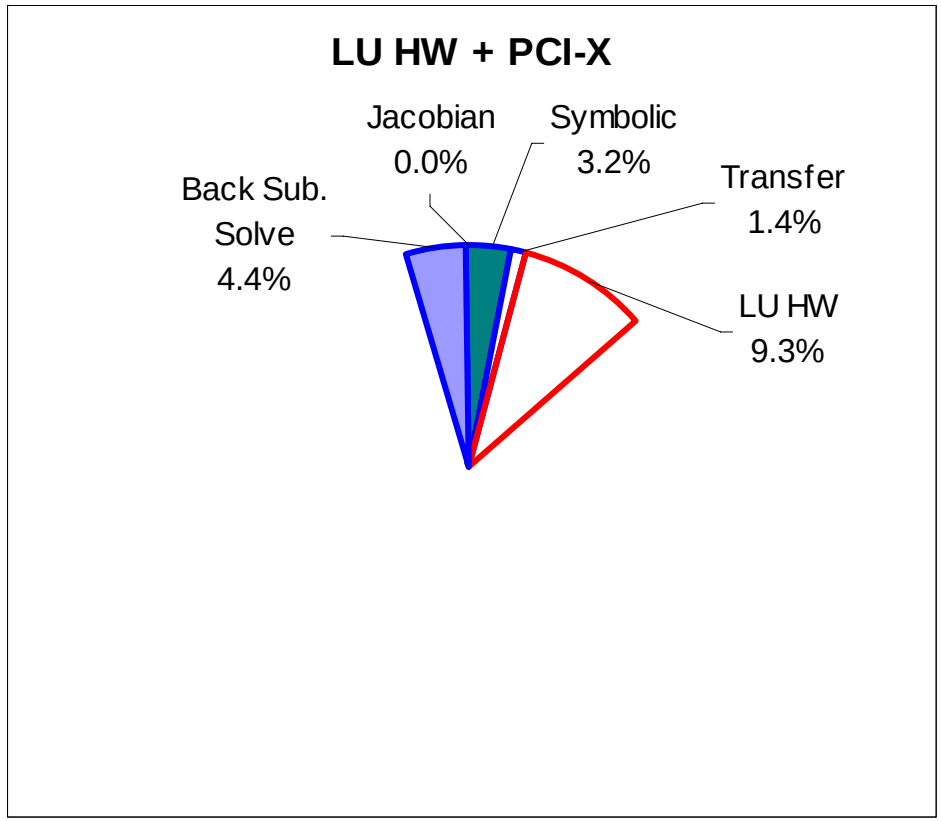
Limitations of Current Approach

- Current power flow sparse LU solvers are software programs written to run on general purpose processors such as the Intel Pentium 4
- General purpose processors are not well-suited to sparse LU computation
  - Floating point efficiency in sparse LU (state-of-the-art) 1-3%
- Cluster computing suffers from high communication overhead and load balancing issues with sparse LU
    - PNNL results show that for Altix 3000 Supercomputer (128 Intel Itanium processors) parallel sparse LU computation speedup is limited to 2 processors and results in 30% improvement in solve time
    - This confirms other studies in the literature and done by our group

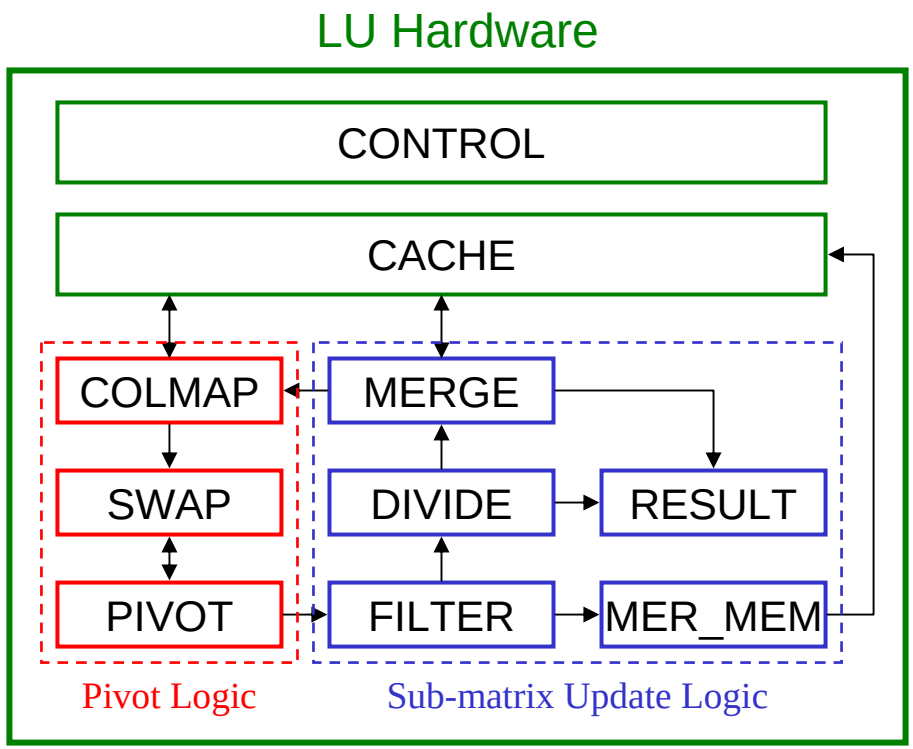
Load Flow With LU Hardware







LU Hardware Block Diagram

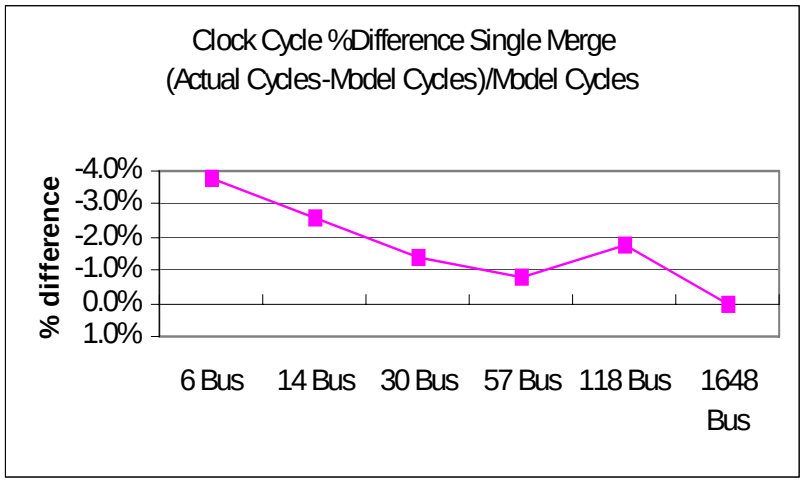


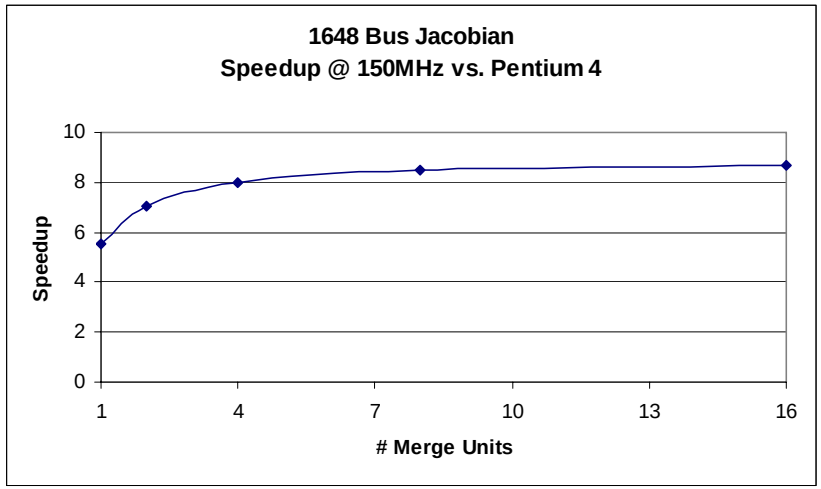
Current FPGA Development Boards

- SBS Technologies Tsunami
  - 64-bit PCI card
  - 5 Stratix 1S25 FPGAs

- Transtech Phoenix VPF1
  - VME/VXS Board
  - Dual PowerPC 7447
  - Dual Virtex II Pro XC2VP70 FPGAs

HW Prototype Results





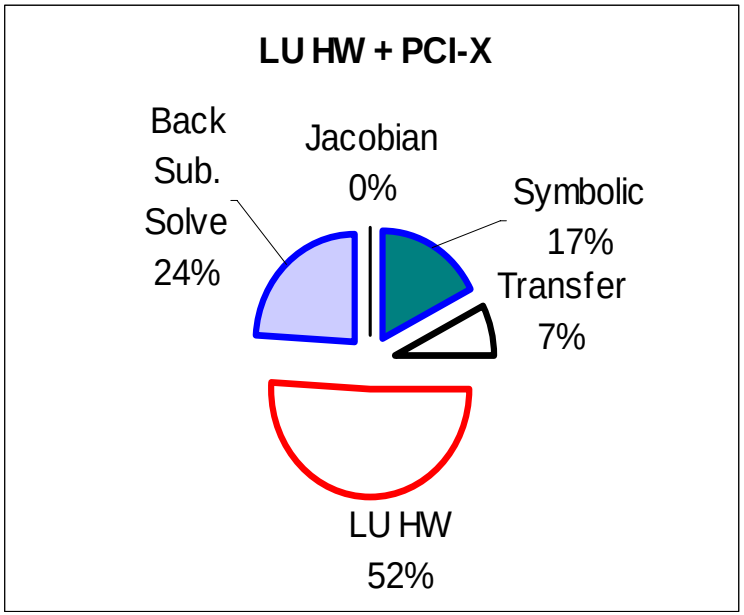
Difference between LU HW actual cycle counts and LU HW model cycle counts is less than 5% for both single merge and dual merge prototypes for Jacobian matrices tested (6 bus to 1648 bus)

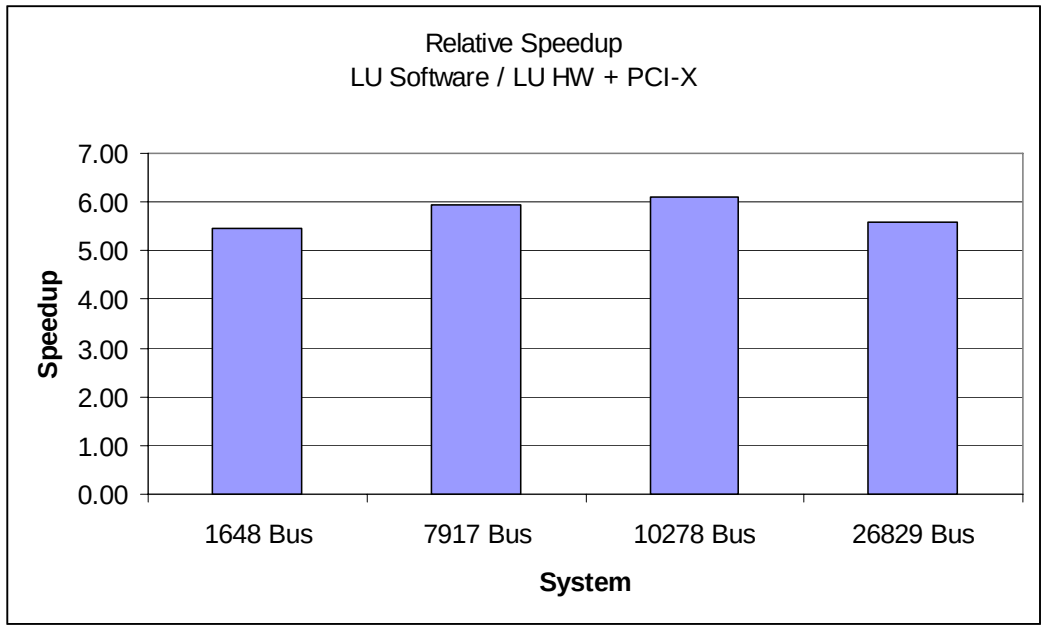
Projected speedups for LU HW operating at 150 MHz based on LU HW model; compared to Pentium 4 benchmark system (CPU time)

Benchmark system details:

- Pentium 4 2.60 GHz
- Atlas CBLAS libraries
- UMFPACK v4.2 sparse linear solver

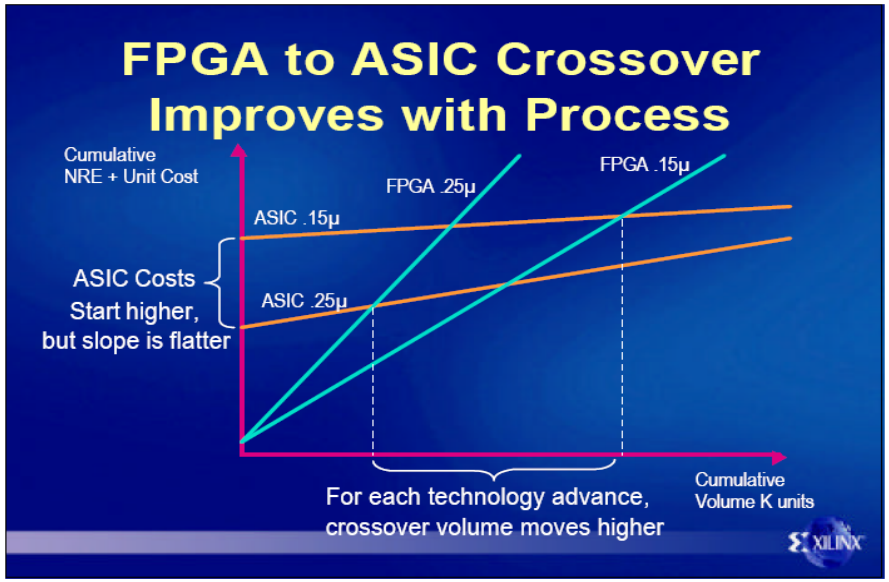
Load Flow Performance

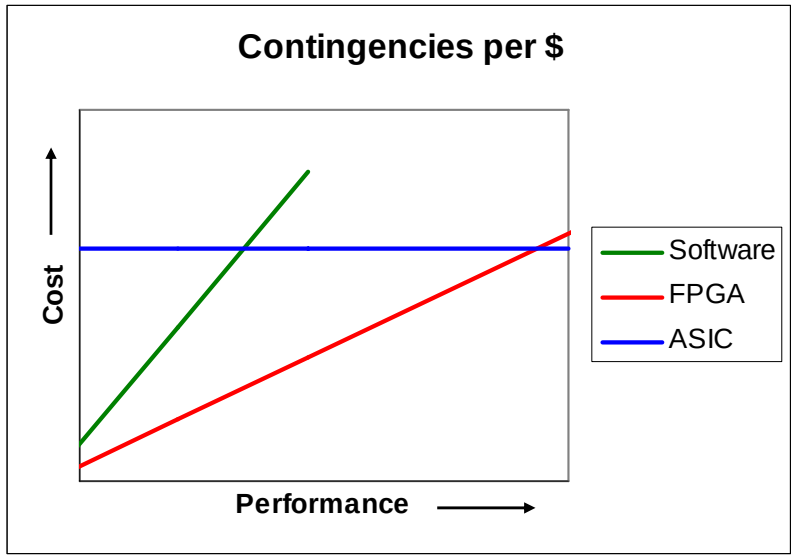




- 10x speedup in LU results is roughly 5-6x speedup in Load Flow
- Transfer time is not a bottleneck
- Diminishing returns on LU without speedup in other areas

Solution Comparison





- FPGA technology can provide higher performance (i.e. more contingencies computed) than current software technologies at a lower cost

- ASIC technology is very expensive to develop, but can provide higher performance and lower cost with high volume production

Accomplishments to Date

All Digital Track

- Benchmark Study of Load Flow Problem (In collaboration with Battelle/PNNL)
  - Exposed limitations in Current Software Approaches
  - Extensive analysis of characteristics of benchmark power systems used to justify approach and to assist with HW design
- LU Solver on FPGA
  - Software Performance Model Validated
  - 10x speedup
- Jacobian Construction on FPGA
  - Fast trigonometric computations using superpipelining
  - Not needed for current HW design
  - Needed when communication bandwidth is a problem
- Benchmark Study of Optimal Power Flow Problem
  - Software Performance Model

Project Remaining Timeline

All Digital Track

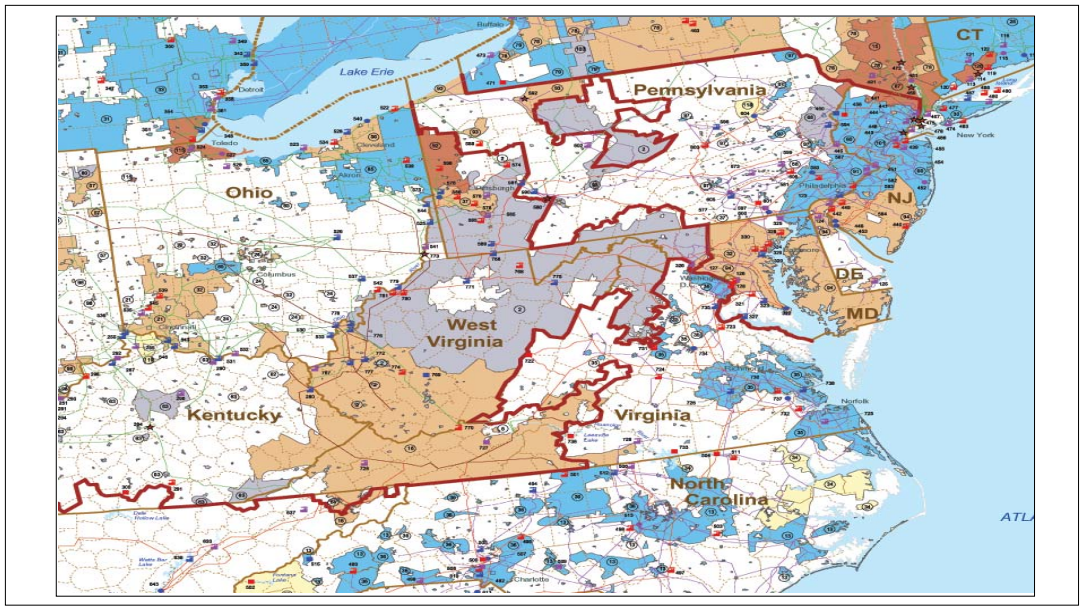
- Work with AREVA to plug in LU Solver into DTS
- Collaborate with Sandia to develop Industrial Grade LU-Solver
- Design FPGA board to compute multiple contingencies in parallel
  - Combine LU Solver with Jacobian Construction
  - Investigate LU/BDB Compound Solver for additional parallelism
- Complete and incorporate OPF Solver

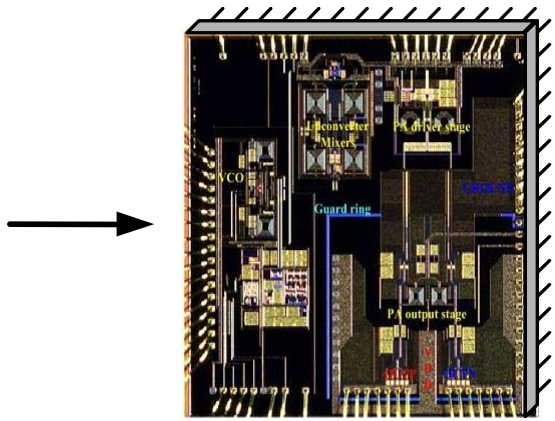
- Complete an independent technical and market assessment of All Digital Approach
- Create a rigorous developmental program plan for eventual technology integration of All Digital Approach

All-Analog Approach

Problems within a Problem

Power System on a Chip (PSOC) by “Analog Emulation”





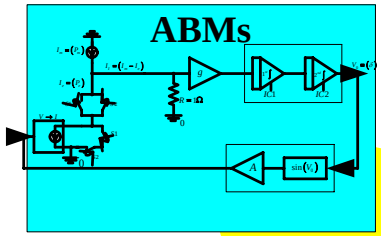
PSOC

Tasks:

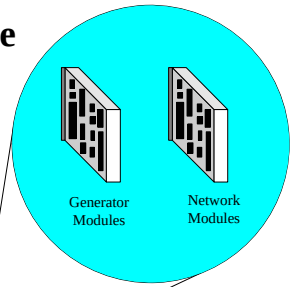
1. Develop power system-specific analog emulation modules
2. Develop appropriate signal conditioning and data acquisition for modules
3. Develop technological path to VLSI implementation

PowerGrid Development Cycle

Stage I
Feasibility Exploration using ABMs

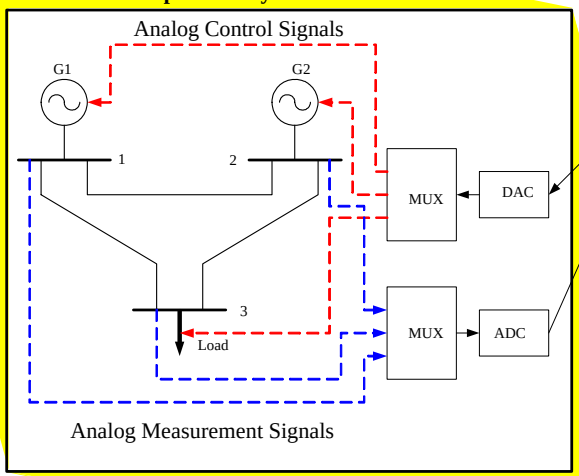


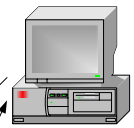
Stage II
PC Board Prototype



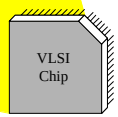
Currently in Stage II

VLSI Chip Power System Emulator





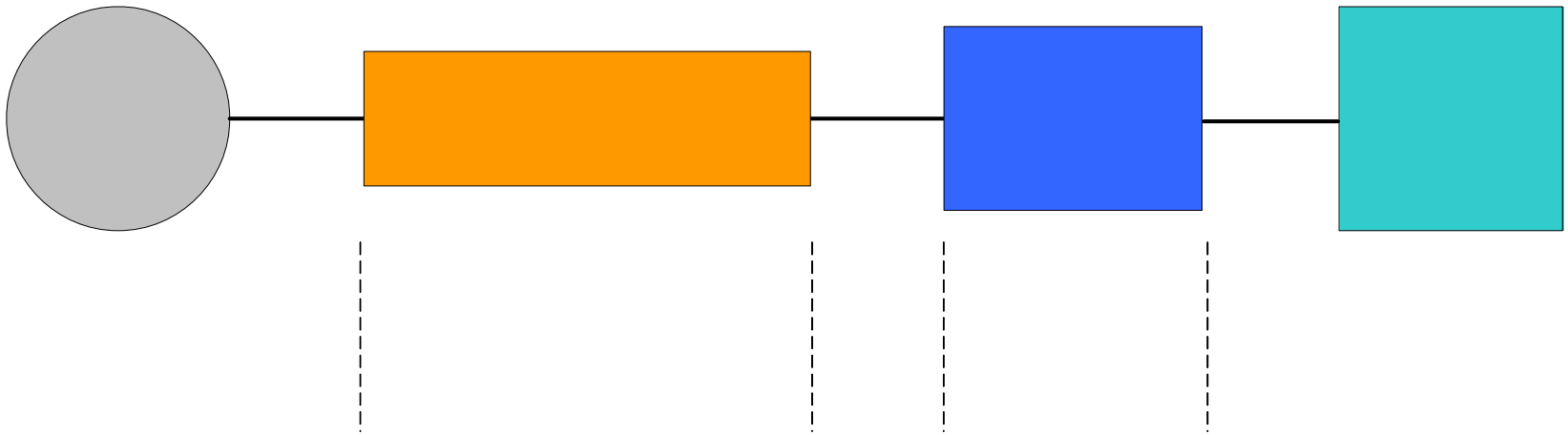
Stage III
VLSI Design



Stage IV
VLSI Development

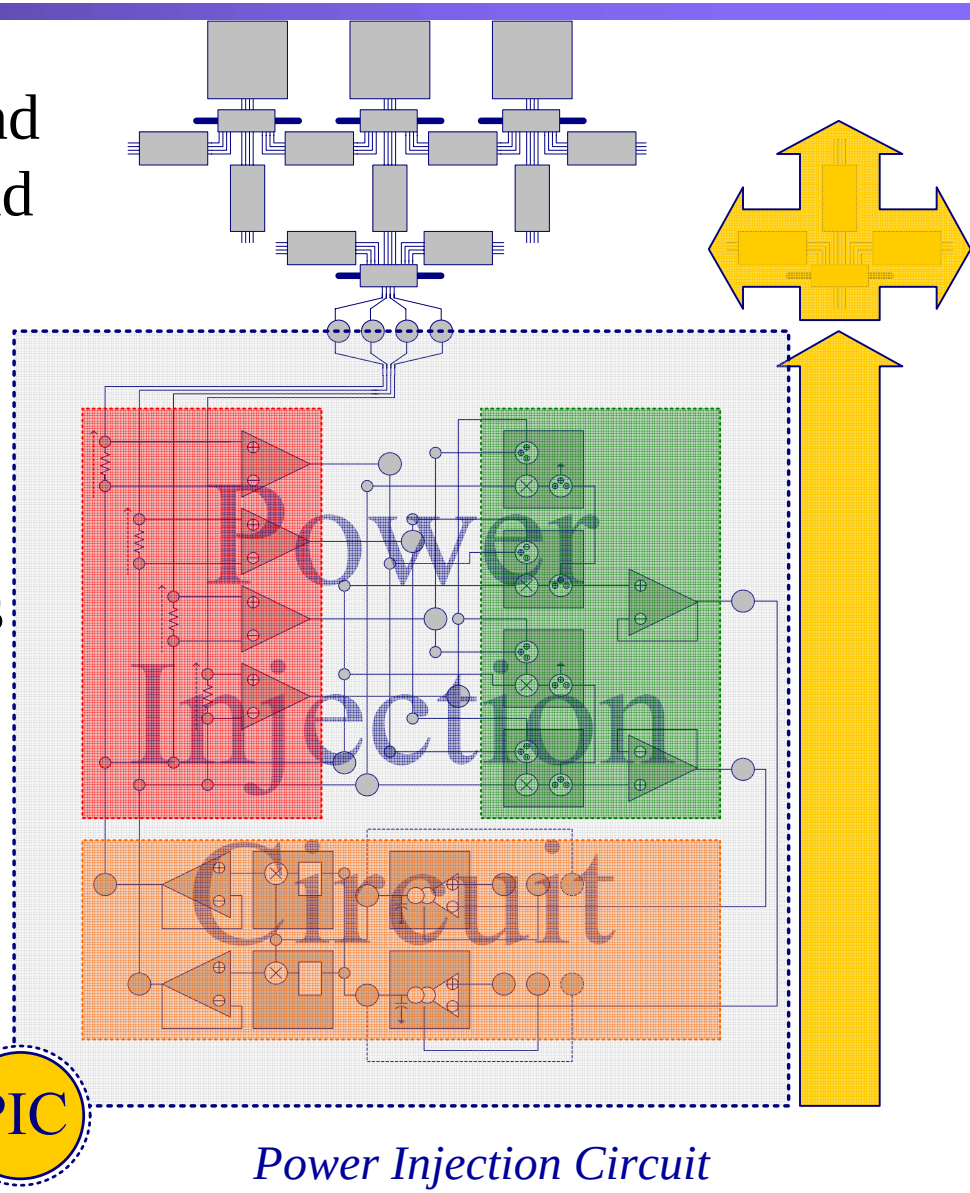
General Classical Model of a Power System

- The power system to be emulated consists of four major components:
  - Generators
  - Transmission Lines
  - Transformers
  - Loads



Power Injection Circuit (PIC)

- SubCkt #1: Acts as interface and measures current flows in to and voltage at bus
- SubCkt #2: Calculate the bus power flows (S_e).
- SubCkt #3: Integrate the difference between S_L and S_e as shown in (2) and (3).
  - Update voltage at bus to form closed loop.
  - For PV operation only one integrator is utilized.



Power Injection Circuit

Accomplishments to Date

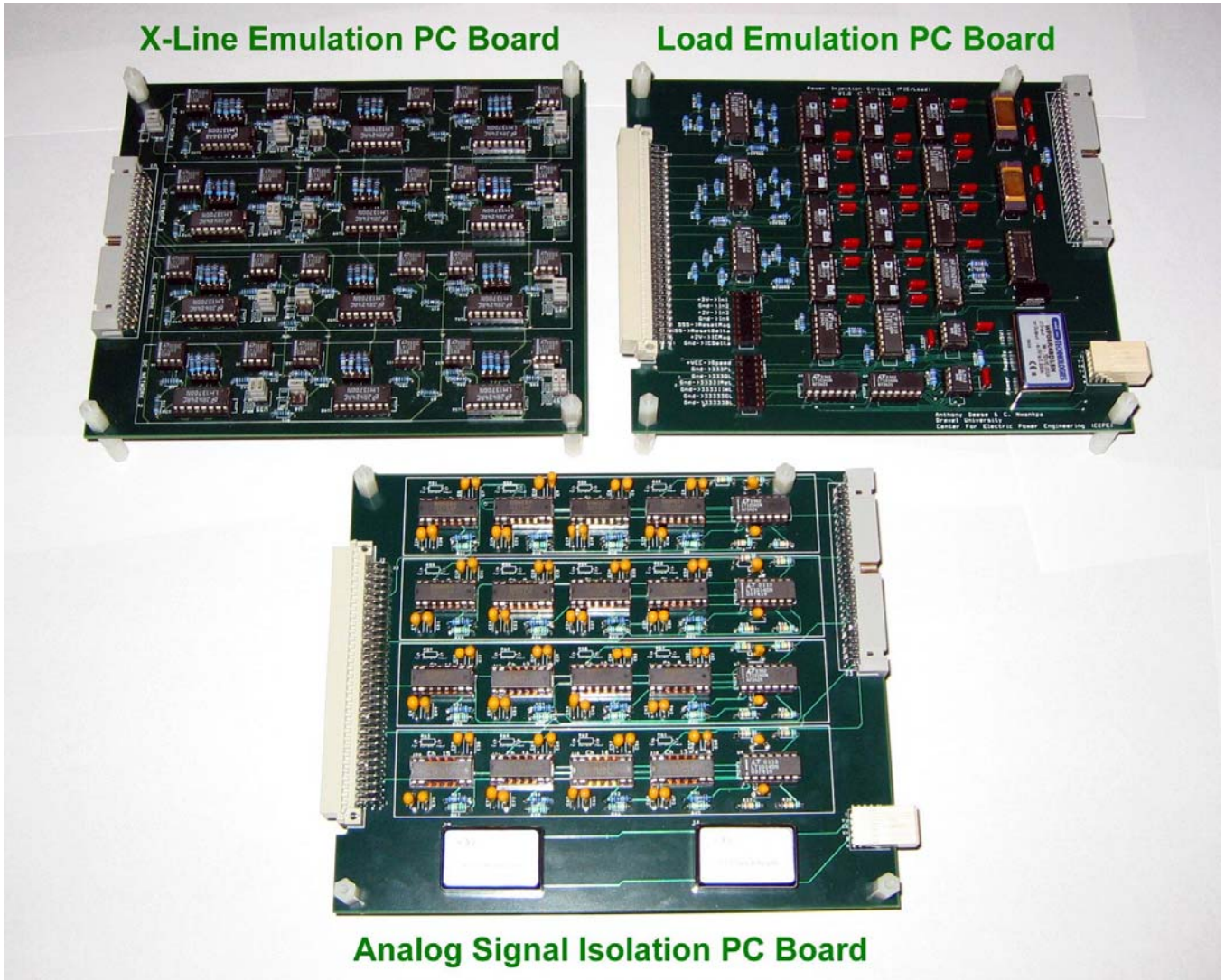
All Analog Track:

- Developed OTA Characterization for PSoC Analog Emulation Purposes
- Developed Analog Generator Module on Prototype Circuit Board
- Developed Analog Transmission Network Module on Prototype Circuit Board
- Developed Analog Transformer Module on Prototype Circuit Board (mixed signal tap changer)
- Developed Analog Load Module on Prototype Circuit Board

PC Board Modeling

- Problem Description
  - Translate ABM models of Power System components into Analog Circuit Form
- Issues:
  - Energy Consumption, Heat Dissipation, Data Acquisition, System Configuration/Actuation, Noise and Accuracy
- Solution
  - Custom Boards Developed for National Instruments SCXI Chassis
  - National Instruments Data Acquisition and Analog Output Cards
  - LabView software Interface to emulator

Realization of PC Boards



Project Remaining Timeline

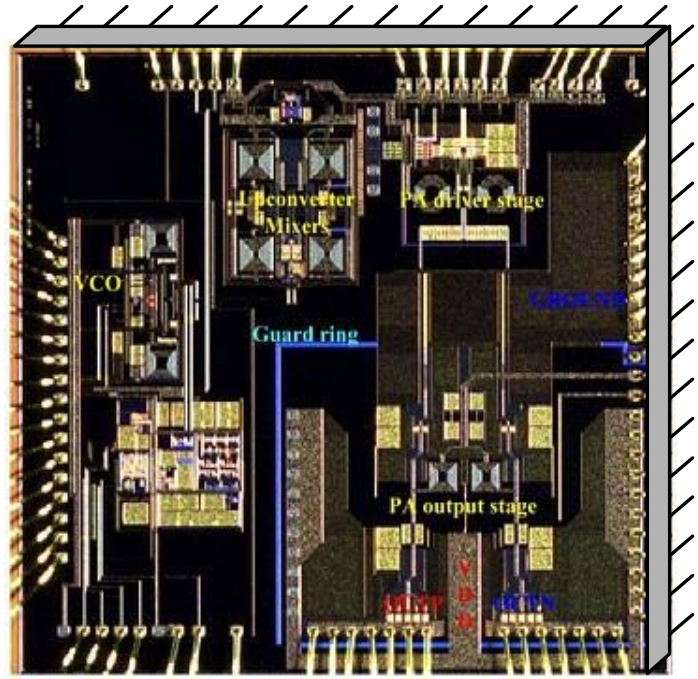
All Analog Track:

- Develop appropriate signal conditioning and data acquisition for modules
- Develop PSoC analog emulation modules for PC-Board Implementation
- With the help of MOSIS (inexpensive internet-based VLSI foundry service) develop a prototype VLSI design of our approach*

* - With possible collaboration of Sandia National Labs

VLSI Device Design and Development

- Problem Description
  - Translate PC Board HW models of Power System components into VLSI Device Form



- Issues:
  - Energy Consumption, Heat Dissipation, Data Acquisition, System Configuration/Actuation, Noise and Accuracy

- Path to Solution
  - Determine detail/sizes to be appropriately represented on a given wafer
  - Use of MOSIS or equivalent foundry service to develop a prototype VLSI design of our approach

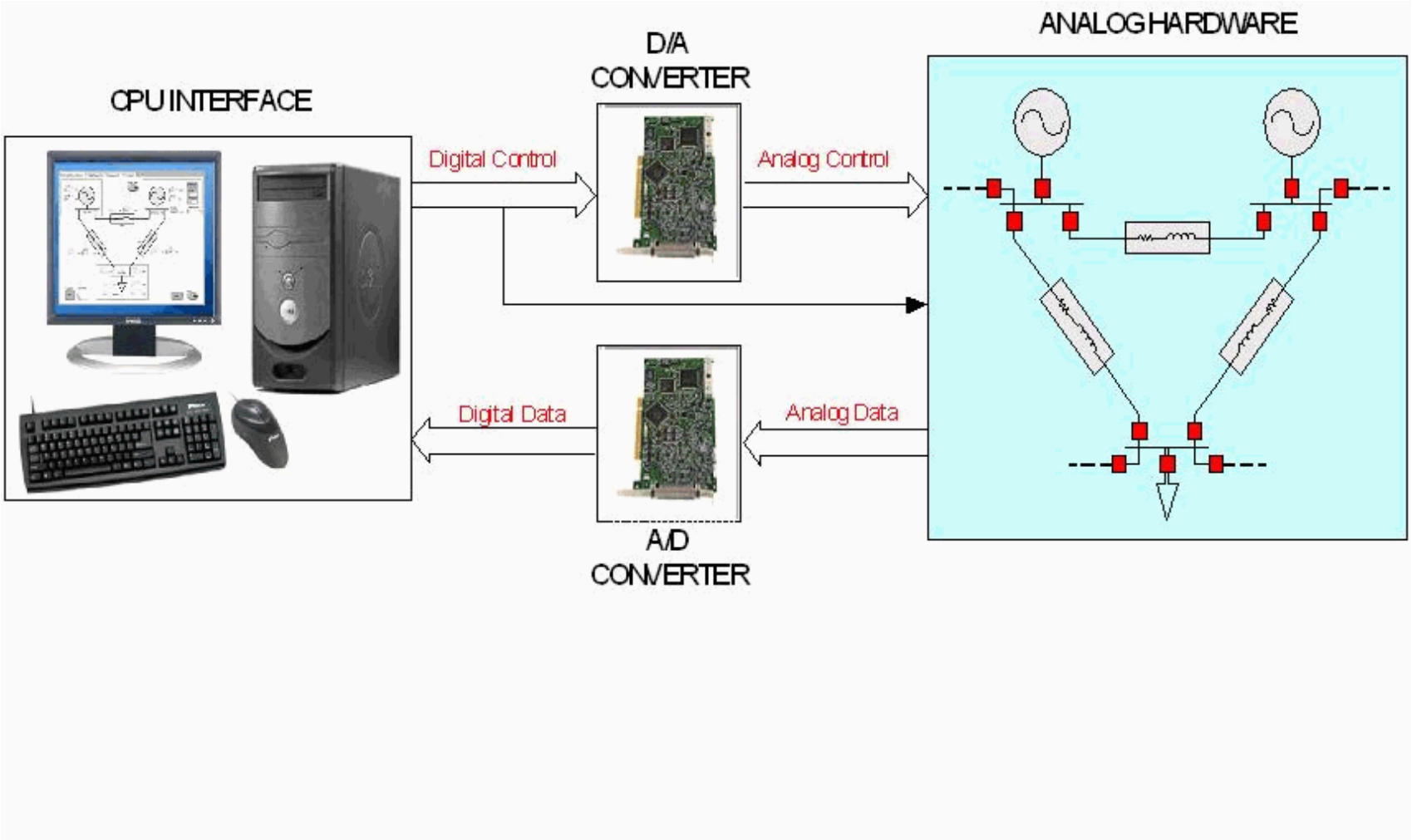
DEMO of
All-Analog Approach:

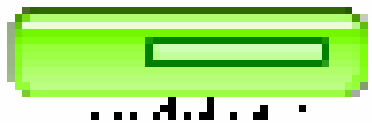
Two Examples:

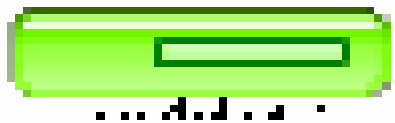
- Load Flow
- Transient Stability

Test Setup

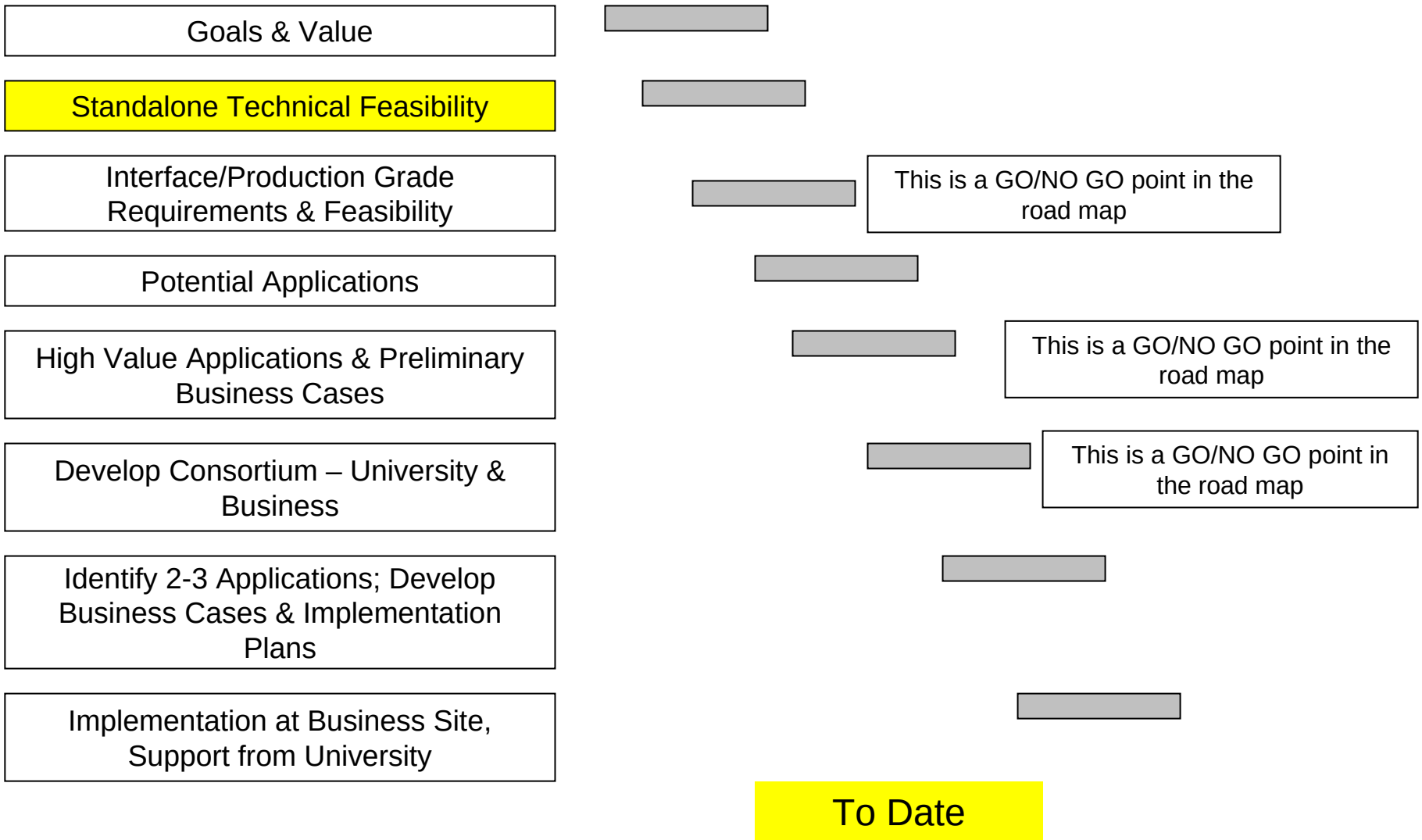
- Three Bus Analog Emulator:







PowerGrid Road Map*



* Developed in conjunction with PJM

Potential Applications

Appl / User	Power Flow	TSA VSA	SA LMP TLC	SE UDS ATC	Real Time Simulation	Real Time Look Ahead	System Restoration	Monte-Carlo Simulation	More ….
TO	X	X						X	
GO									
Utility	X	X	X					X	
ISO, RTO	X	X	X	X	X	X	X	X	

Conclusion and Future Work

In Summary:

- FPGA Work – Industrial Testing
- Analog PSoC – VLSI Feasibility
- Mixed Signal Reconfigurable Computation

National Inst
PCI Cards ar

Computer for Control and Data Acquisition

National Instruments SCXI Chassis