AN OVERVIEW OF CCD DEVELOPMENT AT LAWRENCE BERKELEY NATIONAL LABORATORY

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Abstract: Fully depleted, back-illuminated charge-coupled devices fabricated at Lawrence Berkeley National Laboratory on high-resistivity silicon are described. Device operation and technology are discussed, as well as results on telescopes and future plans.

Key words: charge-coupled device, fully depleted, back illuminated, high-resistivity silicon

1. INTRODUCTION

A new type of scientific charge-coupled device (CCD) has been developed at Lawrence Berkeley National Laboratory (LBNL) [1]. The work was motivated by the LBNL Supernova Cosmology Project (SCP), which studies cosmology via distant, red-shifted supernovae [2]. Conventional thinned, back-illuminated CCD's typically have poor red response and fringing at the near-infrared wavelengths of interest to SCP, while the device described here has much improved red response and negligible fringing by virtue of a thick depleted region.

The CCD's described in this work have been fabricated at the LBNL Microsystems Laboratory, a Class 10 clean room facility that emphasizes fabrication of devices on high-resistivity silicon. More recently interest in volume production for the proposed Supernova/Acceleration Probe (SNAP) space-based imager has led us to begin a technology transfer effort with a commercial CCD manufacturer. Initial results of this effort are described as well as some results from the use of this type of CCD at the National Optical Astronomy Observatory (NOAO) and Lick Observatory.

1.1 Fully-depleted, back-illuminated CCD technology

Figure 1 (a) shows the cross-section of the CCD described in this work. A 3-phase CCD is fabricated on n-type high-resistivity silicon, typically 10-12 kΩ-cm. A backside bias voltage in combination with the extremely low substrate doping allows for full depletion of the substrate at reasonable operating voltages. The substrate doping is typically about 4 orders of magnitude lower than that in the channel. This results in a low sensitivity of the channel potential to the backside bias voltage since only a small fraction of the field lines in the channel terminate in the substrate. Hence to first order the backside bias voltage used to fully deplete the substrate is independent of the bias voltages on the CCD gate electrodes as opposed to deep-depletion CCD's where the depletion depth in the substrate is determined by the voltages on the gate electrodes.

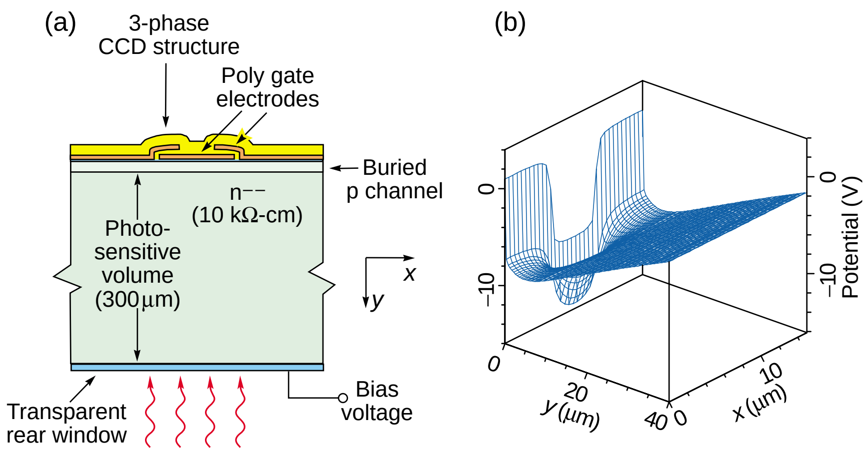

Figure -1(a). Cross section of a fully–depleted, back-illuminated CCD fabricated on high resistivity silicon. *(b).* A two-dimensional simulation showing the potential in the fully-depleted substrate that directs the photo-generated holes to the conventional potential wells generated by the voltages on the CCD gate electrodes.

As a practical matter is it not convenient to make a physical contact to the backside of the CCD as shown in Figure 1. In the actual implementation the contact is made on the front side [3-4]. An n^+ substrate contact surrounds a series of floating p^+ guard rings that terminate on a grounded p^+ guard ring.

The function of the floating p^+ guard rings is to gradually drop the substrate bias voltage between the n^+ contact and the grounded p^+ guard ring. The n^+ contact is located beyond the depletion edge in the quasi-neutral n-type substrate. For low-level light applications the photocurrent-generated voltage drop across the high-resistivity substrate is negligible, and hence the CCD can be fully depleted from the circuit side.

Figure 2 shows a photograph of a 100 mm diameter CCD wafer fabricated at LBNL. The wafer contains 2048 x 2048 $(15\ \mu m)^2$ CCD's as well as smaller format devices. The substrate resistivity is 10-12 kΩ-cm, which results in full depletion of 300 µm thick substrates at bias voltages of 20-25V.

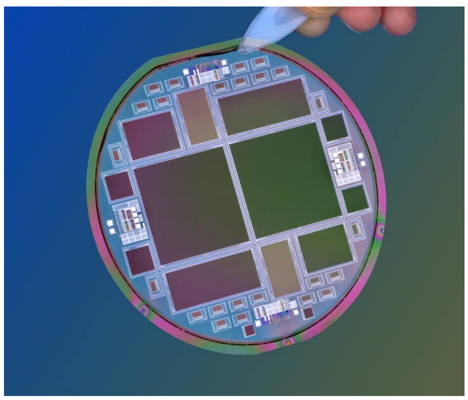

Figure -2. Photograph of a 100 mm diameter CCD wafer fabricated at LBNL.

Performance results measured at Lick Observatory on CCD's from this processing run include a quantum efficiency of 60% at 1 µm wavelength (Figure 3), noise of 4-6 e^- rms at 8 µs sample time each for reset and signal, and CTE exceeding 0.999995. Newer amplifiers have noise levels of approximately 2 e^- rms. Dark currents of less than 10 e^-/pixel-hour at –120C have been demonstrated [4]. The latter is achieved by inverting the CCD channel surface with electrons between frames and taking advantage of the long time constant for electrons trapped at interface states at cryogenic temperatures [6-7].

CCD's from this processing run have been installed on telescopes. Figure 4 shows a near-infrared spectrum of NG7662 taken at the NOAO 4-m telescope with a 1980 x 800 $(15\ \mu m)^2$ CCD on the RC spectrograph [8]. The lack of fringing and high near-infrared quantum efficiency is evident in the

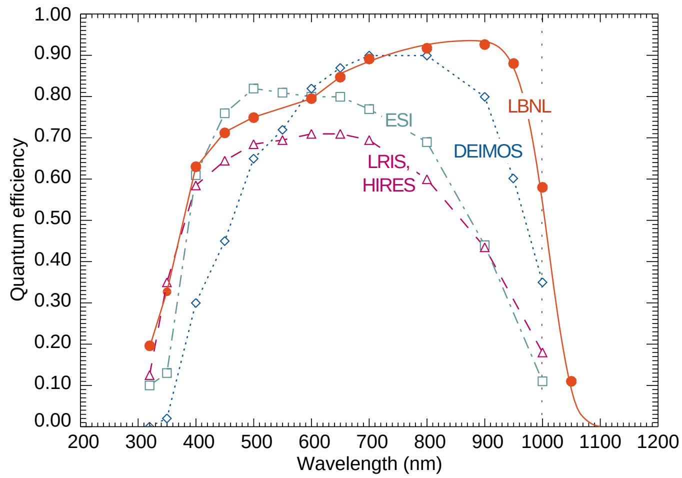

Figure -3. Measured quantum efficiencies comparing a 300 µm thick, fully depleted LBNL CCD versus CCD's in use at the Keck Telescope. The ESI and DEIMOS CCD's were fabricated at MIT Lincoln Laboratory [5], and the HIRES/LRIS CCD's were fabricated at Scientific Imaging Technologies.

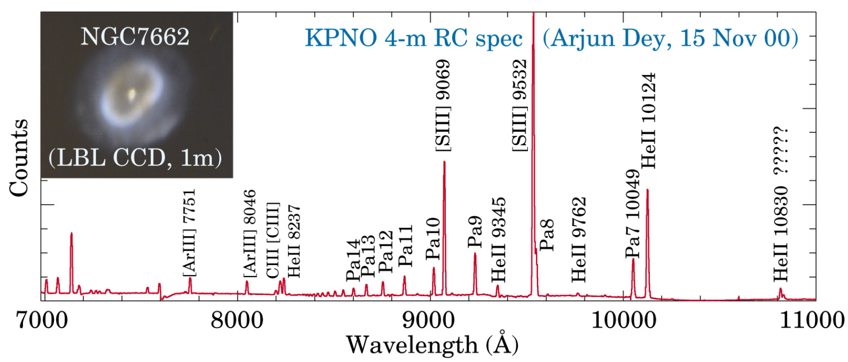

Figure -4. Near-infrared spectrum of NGC7662 taken with a 1980 x 800 (15 µm)^2 LBNL CCD at the NOAO RC spectrograph. Courtesy of Arjun Dey of NOAO.

good resolution of spectral lines at wavelengths above 8000 Å. The image of NGC7662 shown in inset of Figure 4 was taken at the Lick Observatory 1-m telescope on an early 200 x 200 prototype high-resistivity CCD. LBNL CCD's are also in use at the NOAO Multiple-Aperture Red Spectrometer and the Lick Observatory Hamilton Spectrograph.

1.2 Work in progress and future plans

The LBNL SCP group and others have proposed a space-based project (SNAP) to study large numbers of supernovae. A Gpixel imager containing CCD's and infrared detectors is envisioned, requiring significant quantities of both. As a result, we have begun a technology transfer effort with DALSA Semiconductor. Figure 5 shows a 150 mm diameter high-resistivity wafer processed at DALSA Semiconductor. CCD's on this wafer include 2048 x 4096 (15 μm)^2 devices for ground-based astronomy, prototype 12 μm and 10.5 μm pixel SNAP CCD's, as well as other experimental devices. High-quality front-illuminated CCD's have been produced, and initial efforts at the technology transfer of the LBNL back-illumination technology have begun. Figure 6 shows results from a back-illuminated, 300 μm thick, fully-depleted CCD fabricated at DALSA Semiconductor. The only processing step performed at LBNL was the deposition of anti-reflection coatings on the backside of the wafer. Although substantial technology development remains, this is an encouraging and significant result.

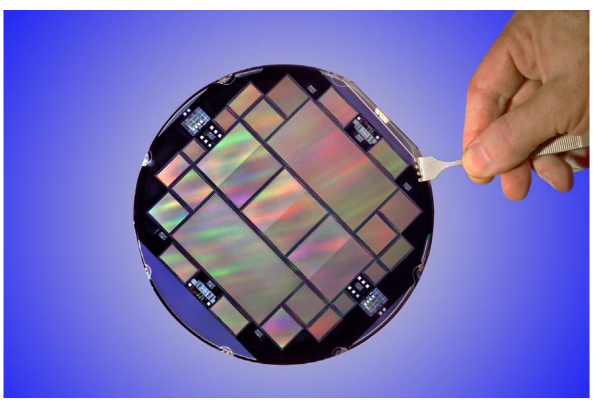

Figure -5. Photograph of a 150 mm diameter, high-resistivity CCD wafer fabricated at DALSA Semiconductor (Bromont, Quebec, Canada).

In addition to the manufacturing challenges for SNAP, small pixels are also desired for the wide-field CCD imager. In order to take advantage of smaller pixel size the point spread function of the CCD imager must be consistent with the smaller pixel size. In a fully-depleted CCD the point spread function (PSF) is determined by lateral diffusion of the photogenerated holes during their transit to the potential wells [9-10] while in a conventional thinned CCD the field-free region at the back surface of the CCD typically dominates.

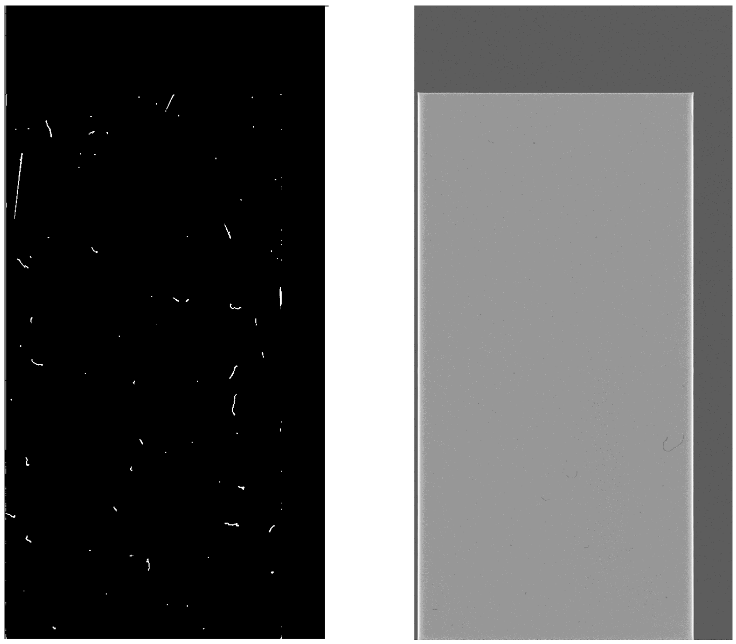

Figure -6. Dark current (left) and 500 nm flat field (right) images taken on a 1024 x 512 (15 µm)^2 fully-depleted, back-illuminated CCD fabricated at DALSA Semiconductor. The dark current at –150C was 3e$^-$/pixel-hour. The CCD was operated overdepleted (substrate bias voltage of 80V).

For the overdepleted case the width σ of the resulting Gaussian charge distribution at the CCD potential wells approaches the constant field limit given by

$$\sigma = \sqrt{2\frac{kT}{q}\frac{{z_{sub}}^2}{(V_{sub} - V_J)}} \qquad (1)$$

where z_{sub} is the substrate thickness, V_{sub} is the substrate bias voltage, V_J is an average potential near the CCD potential wells generated by the applied gate voltages, and kT/q is the thermal voltage. Hence the PSF can be improved by decreasing the substrate thickness and/or increasing the substrate bias voltage. A target CCD thickness for SNAP is 200 µm. This thickness is also advantageous in terms of reducing loss of pixels to cosmic ray hits although the long wavelength quantum efficiency is degraded slightly. Reliable operation of CCD's at substrate bias voltages compatible with the desired SNAP PSF will be the subject of major study during the R&D phase of detector development for SNAP.

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