November 1998 • NREL/SR-520-25941

# Advanced Processing of CdTe- and $CuIn_xGa_{1-x}Se_2$-Based Solar Cells

# Final Report
# 18 April 1995 - 31 May 1998

D.L. Morel, C.S. Ferekides, R. Bhatt,
A. Jayapalan, V. Komin, H. Lin, D. Marinskiy,
S. Marinskaya, R. Narayanaswamy, U. Poosarla,
R. Prabhakaran, H. Sankaranarayanan, B. Tetali,
V. Viswanathan, and S. Zafar
*Department of Electrical Engineering*
*The University of South Florida*
*Tampa, Florida*


National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

NREL/SR-520-25941

# Advanced Processing of CdTe- and $CuIn_xGa_{1-x}Se_2$-Based Solar Cells

# Final Report
# 18 April 1995 - 31 May 1998

D.L. Morel, C.S. Ferekides, R. Bhatt,
A. Jayapalan, V. Komin, H. Lin, D. Marinskiy,
S. Marinskaya, R. Narayanaswamy, U. Poosarla,
R. Prabhakaran, H. Sankaranarayanan, B. Tetali,
V. Viswanathan, and S. Zafar
*Department of Electrical Engineering*
*The University of South Florida*
*Tampa, Florida*

NREL technical monitor: B. von Roedern

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZAF-5-14142-09

November 1998

**NOTICE**



Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (423) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 605-6000 or (800) 553-6847
or
DOE Information Bridge
http://www.doe.gov/bridge/home.html


Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

## TABLE OF CONTENTS

**PART I: CdTe**



**PART II: CIGS**

## LIST OF FIGURES

## LIST OF TABLES

**PART I: CdTe**

## INTRODUCTION

The primary objectives of this project deal with the development of high efficiency thin film CdTe solar cells using fabrication techniques that are suitable for manufacturing environments. The process being developed for the deposition of the semiconductors is the close spaced sublimation (CSS); the CSS has demonstrated high throughput and efficient material utilization. Alternative window materials, TCO's, and back contact schemes are also being investigated.

The close spaced sublimation is being developed for the deposition of CdTe and CdS. The main objective is to deposit both films at temperatures below 550°C, and transfer the process to soda lime glass substrates. During the first two years of this project the low temperature baseline process has been successfully transferred to soda lime glass substrates (tin oxide coated glass purchased from Libbey Owens Ford - LOF). During phase I a 13.9% efficiency was demonstrated for a CdTe(low T-CSS)/CdS(CBD) solar cell. During phase II an all-CSS device fabricated on LOF substrate exhibited a 14.3% efficiency. In all cases the solar cells exhibit state of the art $V_{OC}$'s (840 –860 mV) and ff's (74-76%), while $J_{SC}$'s are in the 21-24 mA/cm$^2$ range, depending on the type of glass substrate. In order to further advance the efficiencies of these devices emphasis is placed on using thin CdS films, a rather straightforward yet very challenging approach, since CdTe cells fabricated on thin CdS exhibit lower efficiencies due to lower $V_{OC}$'s and ff's.

Alternative transparent conducting oxides (TCO's) and window materials being studied under this project include zinc oxide (ZnO) and zinc selenide (ZnSe). Although tin oxide ($SnO_2$) has been the most commonly used TCO for CdTe solar cells, ZnO has exhibited better electro-optical properties. A process for the deposition of ZnO by reactive sputtering has been under development as part of the CIGS component of this project. However, at this stage of the CdTe work, ZnO films being used for the fabrication of CdTe solar cells are deposited by rf sputtering of a ZnO target. Currently, the efficiencies of solar cells fabricated on ZnO/glass substrates are limited by the high series resistance of these devices, which leads to low fill factors. The source of the series resistance is the ZnO, which appears to be unstable under certain processing conditions. Considerable progress has been made in the performance of CdTe/ZnSe junctions and solar cells, however, the ZnSe/CdTe interface is still very difficult to control. During this phase of the project the efficiency of these devices has been advanced to 11.3%.

Back contact electrodes are also being developed as an alternative to the baseline back contact, which currently is doped graphite paste. Emphasis is placed on developing a vacuum deposited electrode, since vacuum processing is favored for manufacturing.

Finally, since the major objective is the development of manufacturable technologies, CdTe solar cells heat treated with $CdCl_2$ vapor, instead of the typical methanol/$CdCl_2$ wet process, are also being fabricated. Although this work is at its early stages it has produced some encouraging results.

## SOLAR CELL FABRICATION PROCEDURES

This section provides an overview of the various processes and fabrication procedures used for the fabrication of the CdTe solar cells, which are of the superstrate configuration. The two types of glass being used are Corning 7059 and LOF ($SnO_2$ coated soda lime) glass.

*TCO's*

The baseline TCO is a bi-layer $SnO_2$ ($SnO_2$:F/$SnO_2$) prepared by chemical vapor deposition (CVD). Aluminum doped ZnO is deposited by rf sputtering, and during this phase of the project it has been deposited onto Corning 7059 glass. The sheet resistance ($R_{SH}$) for both TCO's is typically less than 10 Ω/ (in some cases up to 15 Ω/ ).

*Window Layers*

CSS is the main process being used for the deposition of the window layers (CdS, ZnSe). However, CdS films prepared by the chemical bath deposition (CBD) and occasionally by rf sputtering are also being used for solar cell fabrication.

The window layer is typically heat treated prior to the deposition of the CdTe. The heat treatment is carried out in $H_2$, He, $O_2$, or in the presence of $CdCl_2$. Typical temperatures are in the 300-550°C range.

*CdTe*

All CdTe films are deposited by CSS. During the first phase of this project the CSS CdTe films were grouped into two categories: (a) high temperature (HT) 580-625°C, and (b) low temperature (LT) 500-550°C. During the second phase an additional small area CSS reactor was constructed, which is dedicated to the deposition of CdTe films at temperatures below 500°C. These films will be referred to as CdTe-LTII.

*Post Deposition Heat Treatment*

All CdTe/window/TCO/glass structures are subjected to the typical $CdCl_2$ heat treatment. The $CdCl_2$ can be applied to the surface of the CdTe structures by dipping in a methanol/$CdCl_2$ solution or by evaporation. Some structures have been heat treated in the presence of $CdCl_2$ vapor, in a 2-zone annealing chamber specifically constructed for this purpose.

*Back Contact*

Doped graphite paste (HgTe:Cu) is the baseline electrode used for the fabrication of the CdTe solar cells. Vacuum deposited electrodes ($Cu_xTe$ and ZnTe) are also under development. In both cases, the contact is completed by the application of a second (more conductive) layer, silver paste for the graphite paste and molybdenum for the vacuum deposited contacts. Prior to the formation of the back contact, the CdTe surface is always rinsed to remove the excess $CdCl_2$, and etched using a bromine/methanol or a phosphoric/nitric solution.

## ALTERNATIVE WINDOWS AND TRANSPARENT CONDUCTING OXIDES

### Zinc Oxide

Most of the emphasis in increasing $J_{SC}$ has been placed on thinning the CdS films. However, replacing $SnO_2$, the most commonly used TCO for CdTe cells, with ZnO could also help boost $J_{SC,}$ since ZnO has demonstrated better electro-optical properties [1]. Zinc oxide is prepared by rf sputtering from a ceramic target. It has been previously reported that solar cells fabricated on glass/ZnO substrates exhibited low ff's primarily due to their high series resistance [2]. This was believed to be due to an increase in the resistivity of the as-deposited ZnO films during one of the cell fabrication steps. The following sections review the work performed in this area during this phase of the project. Most ZnO films and solar cells were fabricated on borosilicate glass substrates. Solar cells were fabricated utilizing CdS films deposited by CSS or rf sputtering. The CBD process was not used for the deposition of the CdS films on ZnO/glass substrates, since ZnO is soluble in alkali solutions.

The ZnO films have been deposited by rf sputtering from a 99.999% pure ZnO target. Doping of the films was accomplished by placing alumina pieces on the ZnO target during the sputtering process. The position and number of alumina pieces determined the amount of dopant incorporated into the ZnO films. Typically four (3 x 3 cm) samples were mounted onto a graphite block using a stainless steel holder. The graphite was heated using a 2 kW tungsten halogen lamp. The table shown below provides a summary of the ZnO deposition parameters.

**Table 1. Summary of ZnO deposition conditions.**

| | |
|---|---|
| Base Pressure, (torr) | $1 - 4 \times 10^{-6}$ |
| Deposition Pressure, (torr) | $1 - 4 \times 10^{-3}$ |
| Sputtering Gas | Argon (UHP) |
| Substrate Temperature, (°C) | Room temp. – 500 |
| Power Density, ($W/in^2$) | 10-15 |
| Substrate – Target Distance, (cm) | 5 – 8 |

As previously reported from work carried out on reactively sputtered ZnO films, the substrate – target geometry has an effect on the film properties [3]. The same was true for the ZnO:Al films of this study. It was found that the films located closer to the target (directly above) exhibited higher resistivity, possibly due to high-energy ion bombardment. A thickness variation was also observed, but this was limited within 7-10% across the entire deposition area. The "damage" observed for the samples positioned directly above the target was more pronounced at low deposition temperatures. After a preliminary study of the basic properties of the ZnO films two substrate temperatures, 300 and 500°C, were selected for their deposition. It should be noted that these are the temperatures measured inside the graphite block, and that the actual substrate temperatures may be lower.

As mentioned above, devices fabricated on glass/ZnO:Al substrates exhibited high series resistance. Even though the starting sheet resistance ($R_{SH}$) of the ZnO films was typically less than 15 Ω/ , it was found to be considerably higher after the cells were completed (in some cases more than one order of magnitude higher). In order to identify the processing steps that mostly influence the properties of the ZnO films a series of annealing experiments were carried out. Since, both the CdS and CdTe depositions are carried out in inert or oxygen containing ambient, most annealing experiments were carried out in He or $He/O_2$ atmospheres. The duration of the heat treatments was typically 15 minutes, and the temperature was varied from 300-600°C, in order to cover the entire range of temperatures utilized for cell fabrication. A number of annealing experiments was carried out in a tube furnace, but most films were annealed in the CSS reactor used for the deposition of the CdS films. The ZnO films subjected to the heat treatments were doped with aluminum and the as-deposited $R_{SH}$ was in the 8-15 Ω/ range.

*Annealing in Helium Ambient*

The first set of samples were annealed in inert ambient (He) in order to understand the effect of high temperature processing on the ZnO films. Figure 1 shows the ratio of the sheet resistance of several ZnO:Al films before and after annealing (i.e. $R_{SH}$[as deposited]/$R_{SH}$[annealed]). The two sets of data points represent ZnO films deposited at 300 and 500°C respectively. As this figure suggests, the change in $R_{SH}$ is within 25-30% of the as deposited value, even for temperatures as high as 600°C. For the films deposited at 500°C, the change in $R_{SH}$ was smaller, suggesting that the stability of the ZnO films improves when these are deposited at relatively high temperatures. The data points corresponding to the 400 and 500°C annealing temperatures, for the ZnO film deposited at 500°C, are actually greater than 1.0. Although, this is within experimental error (5-10%), a slight decrease in $R_{SH}$ after annealing at low temperatures (300-500°C) was observed on several occasions.

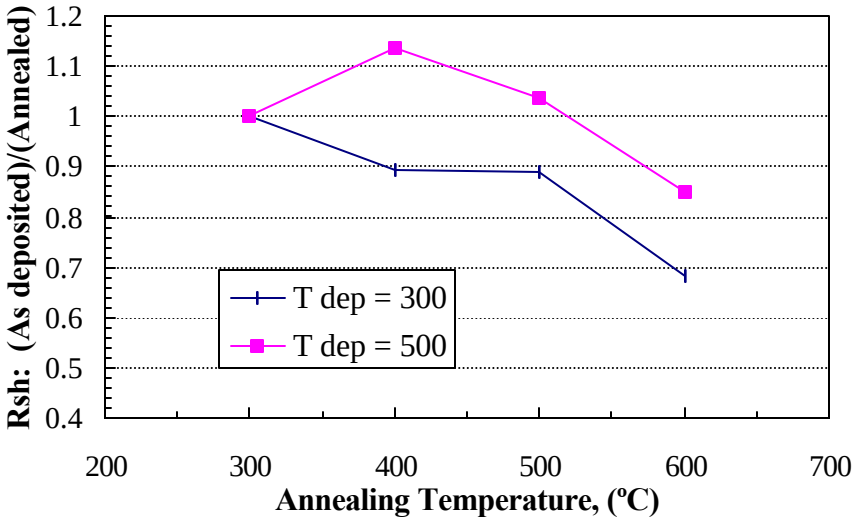



**Figure 1. The effect of annealing on the sheet resistance of ZnO:Al films.**

Hall measurements were performed to measure the carrier concentration and mobility of the ZnO:Al films. These results are shown in figs 2 and 3 ($T_{dep}$=300°C). Although, the data in fig. 1 suggest a rather small change in the as-deposited resistivity of the ZnO films, figs. 2 and 3 show a considerable increase in mobility, which is compensated by a decrease in the carrier concentration. Similar behavior was observed by others [4]; in that case this type of behavior was attributed to oxygen chemisorption. The resistivity of the ZnO:Al films calculated from Hall measurements was in very good agreement with four point probe measurements as shown in table 2.

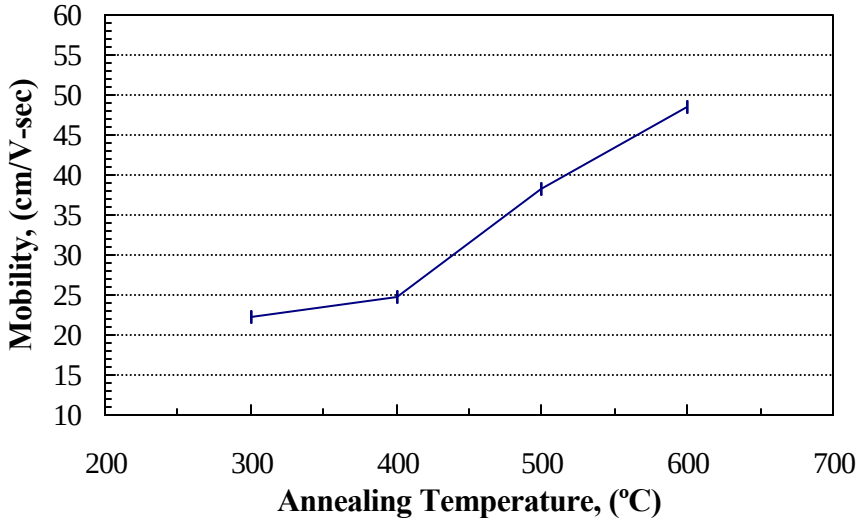



**Figure 2. The effect of annealing temperature on the mobility of ZnO:Al films.**

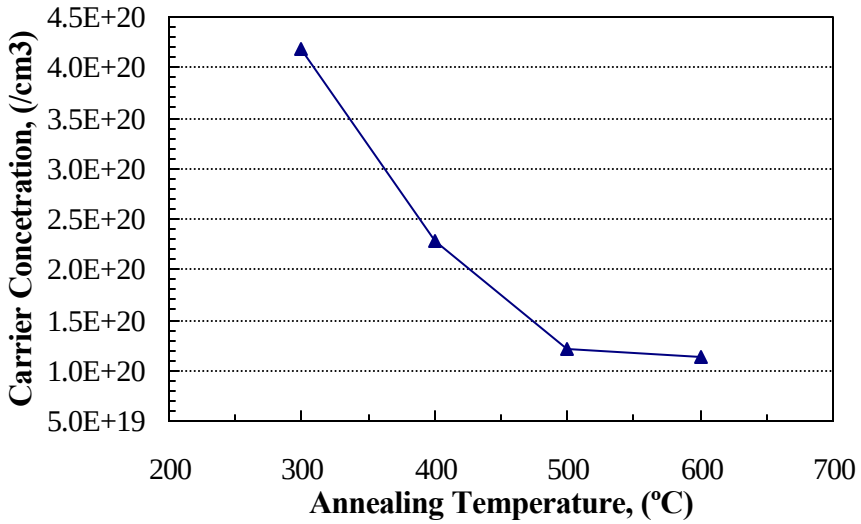



**Figure 3. The effect of annealing temperature on the carrier concentration of ZnO:Al films.**

**Table 2. ZnO:Al resistivity after annealing in He ambient.**

| Annealing Temperature, (°C) | $\rho_{Hall}$, (Ω-cm) | $\rho_{4\text{-}pp}$, (Ω-cm) |
|---|---|---|
| 300 | $6.070 \times 10^{-4}$ | $6.69 \times 10^{-4}$ |
| 400 | $0.960 \times 10^{-3}$ | $1.08 \times 10^{-3}$ |
| 500 | $1.107 \times 10^{-3}$ | $1.33 \times 10^{-3}$ |

Based on the rather small change in resistivity for the set of samples described above, it was concluded that the much larger change in $R_{SH}$ observed in finished devices was due to the fact that $O_2$ was present during the deposition of the CSS-CdS films. As previously reported, CSS CdS films prepared in the presence of $O_2$ have yielded considerably higher efficiencies, and these types of films are the ones used routinely for the fabrication of CdTe solar cells [2].

*Annealing in Oxygen Ambient*

In order to determine the effect of $O_2$ on the properties of the ZnO films, a series of annealing experiments were carried out in He/$O_2$ ambient. The amount of $O_2$ was varied from 10 to 100%. The annealing temperatures were again varied from 300-600°C, but most experiments were carried out at 500-550°C, since this is the desirable temperature range for the fabrication of solar cells. The annealing time was kept constant at 15 minutes.

The ratio of the sheet resistance for several ZnO:Al films before and after annealing ($R_{SH}$[as deposited]/$R_{SH}$[annealed]) at 550°C is shown in fig. 4. In contrast to the results presented in fig. 1, this time a rather large increase in $R_{SH}$ is observed, even in the case where only 10% $O_2$ was used. ZnO films deposited at 500°C were affected less than those deposited at 300°C, as was the case for the films annealed in He.

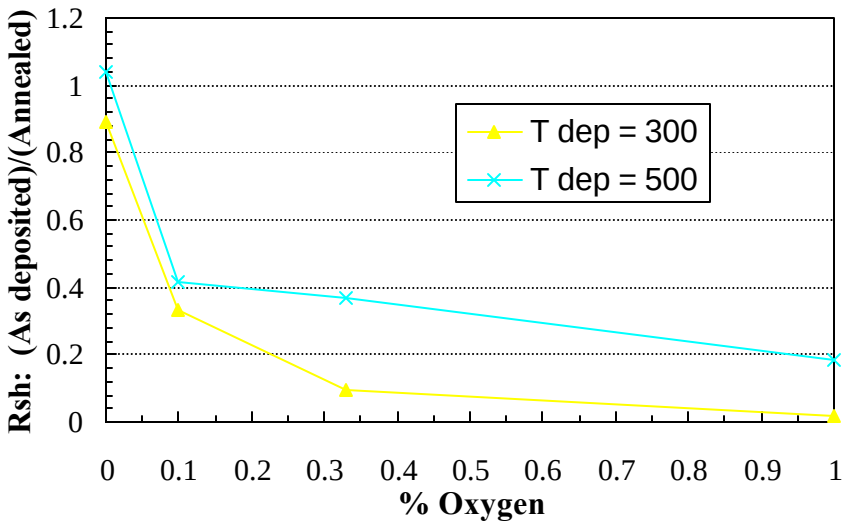



**Figure 4. The effect of annealing in He/$O_2$ ambient on the sheet resistance of ZnO:Al films.**

The mobility and carrier concentrations for the above films are shown in figs. 5 and 6. In this case both parameters have decreased as a result of the heat treatment in $O_2$. Others observed similar behavior, and it was suggested that the decrease in the carrier concentration was due to oxygen adsorbed at the grain boundaries where it acts as an electron trap. A limited number of XRD measurements were carried out, and these suggested that the crystallinity of the ZnO films annealed in He was superior to the ones annealed in oxygen. The annealing experiments verified that the observed increase in $R_{SH}$ was due to the fact that the ZnO films were subjected to high temperatures in the presence of oxygen. Nevertheless, solar cells were fabricated using both CSS-CdS films prepared in $O_2$ and inert ambient in order to determine whether the use of $O_2$ was the only processing parameter affecting the properties of ZnO,

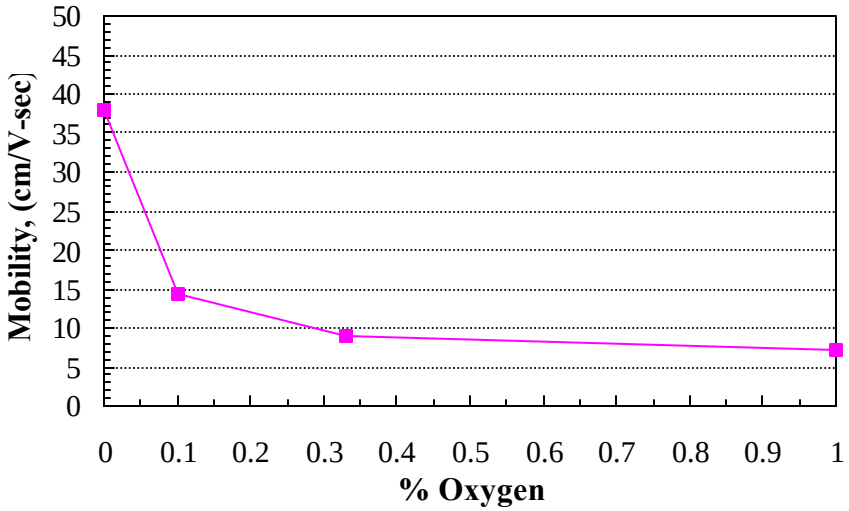



**Figure 5. The effect oxygen concentration during annealing on the mobility of ZnO:Al films.**

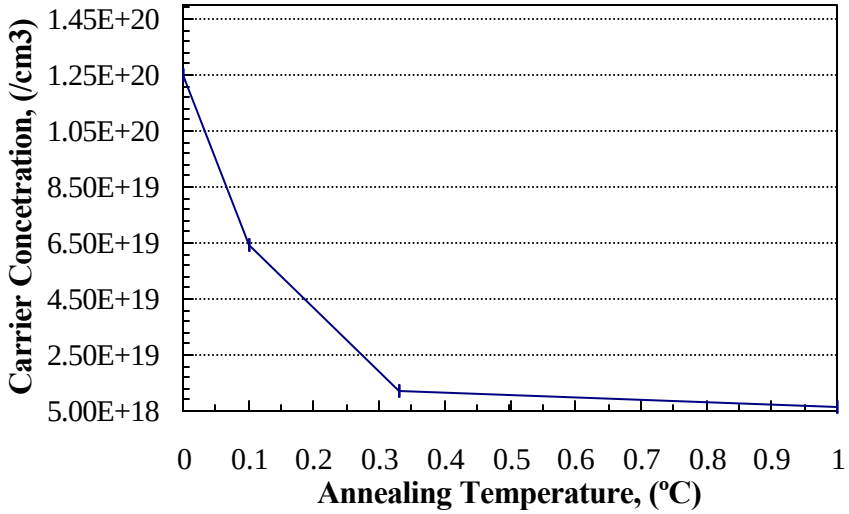



**Figure 6. The effect oxygen concentration during annealing on the carrier concentration of ZnO:Al films.**

*Solar Cell Results*

After completion of the above annealing experiments, ZnO:Al films were deposited on Corning 7059 and subsequently used for the fabrication of solar cells. The following variations in cell processing were used:

a) ZnO/CSS-CdS(He)/CSS-CdTe(LT,HT)
b) ZnO/CSS-CdS($O_2$))/CSS-CdTe(LT,HT)
c) ZnO/sputtered CdS/CSS-CdTe
d) ZnO/CdTe

The first sets of devices were fabricated with CSS-CdS deposited in He ambient. The thickness of the CSS-CdS for most of the devices discussed in this section was kept above 1000 Å. The sheet resistance of the ZnO films before and after the deposition of the CSS-CdS is shown in table 3. These results are in very good agreement with the annealing experiments described in the previous section. It is therefore suggested that if any interaction between the ZnO and CdS films took place during the CSS-CdS process, it did not have a measurable effect on the ZnO properties. Table 4 shows the performance of three solar cells (fabricated on ZnO substrates). It should be noted that the highest $V_{OC}$ obtained on $SnO_2$/glass substrates with CSS-CdS(He) films was also about 820 mV. It therefore appears that the use of ZnO as a TCO under this particular set of deposition conditions has no apparent detrimental effect on $V_{OC}$. The ff's are in the mid 60's similar to the performance obtained on $SnO_2$ substrates (see note at bottom of page for $J_{SC}$'s).

**Table 3. The sheet resistance of ZnO before and after the deposition of CSS-CdS(He).**

| ZnO Dep. Temp., (°C) | As deposited $R_{SH}$, (Ω/□) | $R_{SH}$ After CSS CdS Deposition, (Ω/□) | Ratio |
|---|---|---|---|
| 300 | 18.23 | 19.12 | 0.9534 |
| 300 | 15.62 | 16.20 | 0.8864 |
| 500 | 17.25 | 17.69 | 0.9850 |
| 500 | 16.42 | 16.20 | 1.010 |

**Table 4. Solar cell parameters for CdTe/CdS(He)/ZnO solar cells.**

| $V_{OC}$, (mV) | ff | $J_{SC}$, (mA/cm$^2$) | Efficiency, (%) |
|---|---|---|---|
| 820 | 0.663 | 18.67 | 10.80 |
| 814 | 0.671 | 18.09 | 9.88 |
| 810 | 0.621 | 18.53 | 9.22 |

Note: Scribing of the CdTe/CdS/ZnO structures and removal of the CdTe in order to define the cell areas was difficult, due to the strong adherence of the CdTe/CdS films to the substrate. This made it extremely difficult to measure the cell areas precisely, and the $J_{SC}$'s were in all cases underestimated. $J_{SC}$'s calculated from SR measurements were typically in the 21-23 mA/cm$^2$ range.

The SR of one of the above devices is shown in fig. 7. The sharp cut-off at 510 nm is what one should expect from solar cells fabricated with CSS-CdS deposited in He ambient [5]. The overall response was over 90%, suggesting that ZnO has the potential of replacing $SnO_2$ as the TCO for CdTe solar cells. No AR coating was used for the device shown in fig. 7.

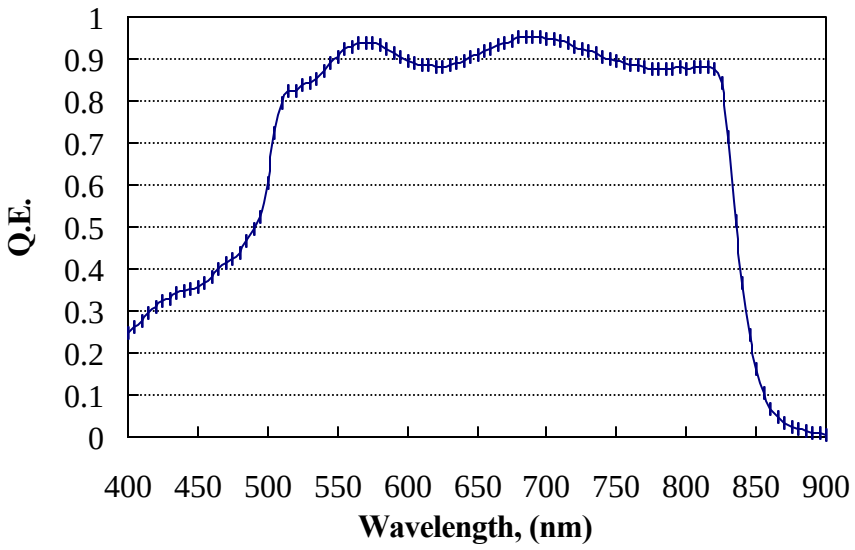



**Figure 7. The SR of a CdTe solar cell fabricated on a ZnO:Al/glass substrate.**

The deposition of CSS-CdS in the presence of $O_2$ has to date produced the best solar cell performance for all-CSS devices. However, as the previous annealing results suggested, these conditions cause the resistivity of ZnO to increase beyond what is acceptable for solar cell applications. Table 5 shows the change in the sheet resistance of ZnO:Al films after the deposition of CSS-CdS in 10% $O_2$. These results are consistent with the annealing experiments of the previous section.

The solar cell characteristics of devices fabricated using CSS-CdS deposited with 10 and 50% $O_2$ in the ambient are shown in table 6. The device fabricated with CSS-CdS(50% $O_2$) exhibited a considerably lower ff as expected. However, the $V_{OC}$'s for all cells are about 30-40 mV lower than what one should expect from CdS($O_2$) devices. It is not clear at this time whether this is related to the ZnO substrate.

**Table 5. The sheet resistance of ZnO before and after the deposition of CSS-CdS($O_2$).**

| ZnO Deposition Temp., (°C) | As-deposited $R_{SH}$ | $R_{SH}$ after CSS-CdS | Ratio |
|---|---|---|---|
| 500 | 7.61 | 87.80 | 0.125 |
| 500 | 15.70 | 60.40 | 0.325 |

**Table 6. Solar cell parameters for CdTe/CdS($O_2$)/ZnO solar cells.**

| % $O_2$ | $V_{OC}$, (mV) | ff |
|---|---|---|
| 10 | 803 | 0.66 |
| 10 | 815 | 0.57 |
| 50 | 820 | 0.40 |
| 50 | 818 | 0.41 |

**Zinc Zelenide**

A considerable effort has been dedicated to the study of CdTe solar cells fabricated with thin CdS layers in order to improve the short-circuit current of` these devices (this has been one of the early main objectives of the CdTe National Team). Although CdS has to date been the most successful n-type window layer for CdTe solar cells, other options that could possibly yield better results should be considered. Zinc selenide has a bandgap of 2.67 eV; therefore, replacing CdS with ZnSe would result in a ~50 nm shift (from 510 to 465 nm) in the blue response of CdTe solar cells. The use of ZnSe can lead to higher photocurrents due to the fact that a larger fraction of the blue photons will reach the CdTe layer. However, the difference in the electron affinities for CdTe and ZnSe leads to a discontinuity (positive) in the conduction band which impedes the transport of photo-generated carriers (electrons from the CdTe). It has also been suggested that interdiffusion at the metallurgical interface of a heterojunction can "smear out" and lower this discontinuity. It was expected, and indeed we found out, that interdiffusion at the CdTe/ZnSe interface would take place, which should alleviate the problem that arises from the differences in the electron affinities of the two materials [6,7].

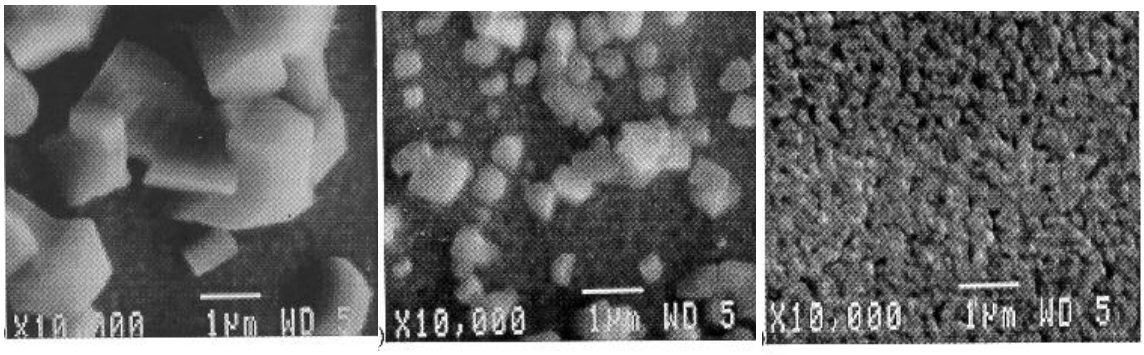
Understanding and controlling the formation of the CdTe/ZnSe junctions proved to be a challenging task. Reproducibility problems have hindered efforts to obtain a better understanding of the junction formation process and considerably advance the performance of these devices. During phase II, a number of processing parameters were identified as critical in achieving reproducible results for CdTe/ZnSe junctions.

*Deposition Process*

The ZnSe films are being deposited by CSS; the reactor for the deposition of the films is identical to those used for CdTe and CdS. The source material is 99.999% pure ZnSe powder, or 99.995% ZnSe pieces up to 10 mm in diameter. Early efforts to directly sublime the powder or the 5-10 mm pieces were unsuccessful due to considerable variation in film thickness, and in the case of the powder source, due to injection of small ZnSe particles onto the substrate. Instead, a thick layer of ZnSe was sublimed onto an $Al_2O_3$ plate and subsequently used as the source material. The ZnSe films are being deposited in inert ambient (1-300 torr of He), and the source and substrate temperature ranges are 700-780 and 560-680°C respectively.

As previously mentioned, it has been difficult to reproduce the performance of CdTe/ZnSe junctions. After a few experiments aimed at controlling the microstructure of the CSS-ZnSe films, it was found that the deposition process itself was dynamic in

nature. The deposition rate decreased during the first few depositions and eventually saturated to a constant value. This had a significant effect on the microstructure of the films. Figure 8 shows the SEM micrographs for ZnSe films deposited under identical conditions. As the data suggests, the first few depositions (faster growth rates) result in very large grains and discontinuous films. After a few depositions (when the growth rate stabilizes) the ZnSe films have smaller grains and are continuous. Although, this is believed to be one of the major reasons affecting the non-reproducibility of the CdTe/ZnSe junctions, it was found that it was not the only one. Even after using films prepared with the same "deposition rate" conditions, considerable variation in performance was still present (even on the same substrate). Figure 9 shows the SR of two CdTe/ZnSe solar cells fabricated on the same substrate; the $V_{OC}$ for these cells varied from 470 to 720 mV. Variations in the thickness of the ZnSe were ruled out, since this layer was found to be uniform within 2-5% over the entire substrate area. In order to determine whether this behavior was due to compositional variations in the ZnSe films, EDS measurements were performed using single crystalline ZnSe for reference. The composition of two CSS films and the single crystal ZnSe sample, shown in table 7, suggest that the deposited films were stoichiometric.




(a) (b) (c)

**Figure 8: SEM micrographs of ZnSe films; (a) 2nd deposition, (b) 5th deposition, and (c) 13th deposition.**

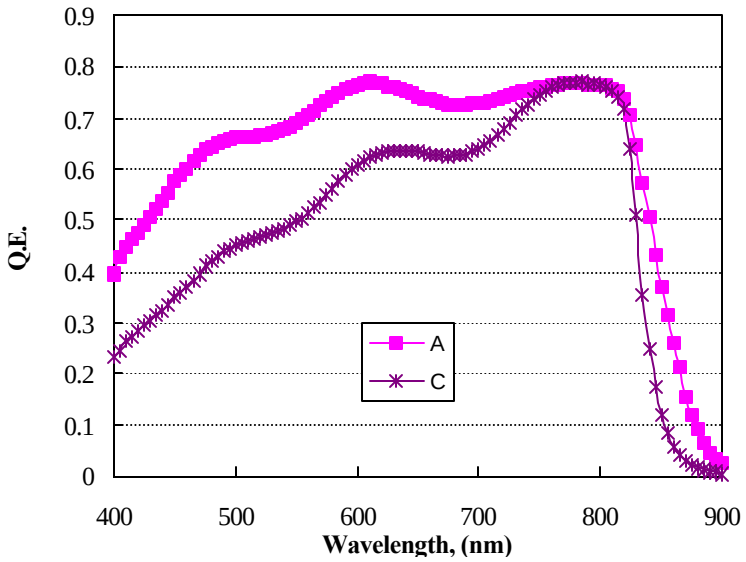



**Figure 9. The SR of two CdTe/ZnSe cells fabricated on the same substrate.**

**Table 7. Composition of CSS-ZnSe films.**

| Sample # | Zn, (atomic %) | Se, (atomic %) |
|---|---|---|
| Single Crystal | 56 | 44 |
| N 9-13-1C | 56 | 44 |
| N 9-4-1D | 55 | 45 |

*$CdCl_2$ Heat Treatment*

Attention was then focused on the $CdCl_2$ heat treatment, since this is believed to be one of the processing steps affecting the degree of interdiffusion between the semiconductors. Several experiments were carried out to determine its effect on solar cell performance. Application of $CdCl_2$ using a $CdCl_2$/methanol solution results in non-uniform $CdCl_2$ films on the CdTe surface. This does not appear to be significant for CdTe/CdS solar cells; however, to better control the amount of $CdCl_2$ on CdTe/ZnSe structures, evaporation was used instead. CdTe/ZnSe structures were coated with $CdCl_2$ to a thickness of 3-6 and 10-15 kÅ, and subsequently heat-treated in a tube furnace. Each sample used in this study was cut in half, and each half was coated with $CdCl_2$ of a different thickness. Variation of the $CdCl_2$ thickness in the 3-6 kÅ range did not seem to have a significant effect on $V_{OC}$. However, on average, the $V_{OC}$ of devices treated with a 3-6 kÅ thick $CdCl_2$ layer was higher than those treated with a 10-15 kÅ thick layer. This trend is shown in figure 10 where the difference in $V_{OC}$ is shown for eleven devices.

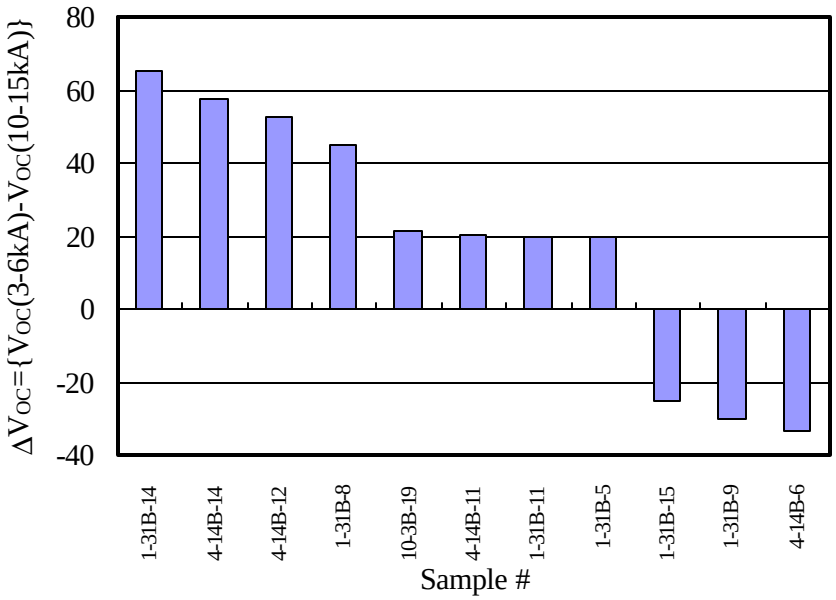



**Figure 10. The difference in $V_{OC}$ for CdTe/ZnSe junctions treated with $CdCl_2$ of different thicknesses.**

*Spectral Response*

Spectral response measurements were used as a tool to better understand the influence of processing on the properties of the CdTe/ZnSe junctions. Figure 11 shows typical CdTe/ZnSe SR's labeled type I, II, and III, along with the SR of a CdTe/CdS solar cell. These CdTe/ZnSe data exemplify the complexity of these junctions. The performance data for these devices are shown in table 8.

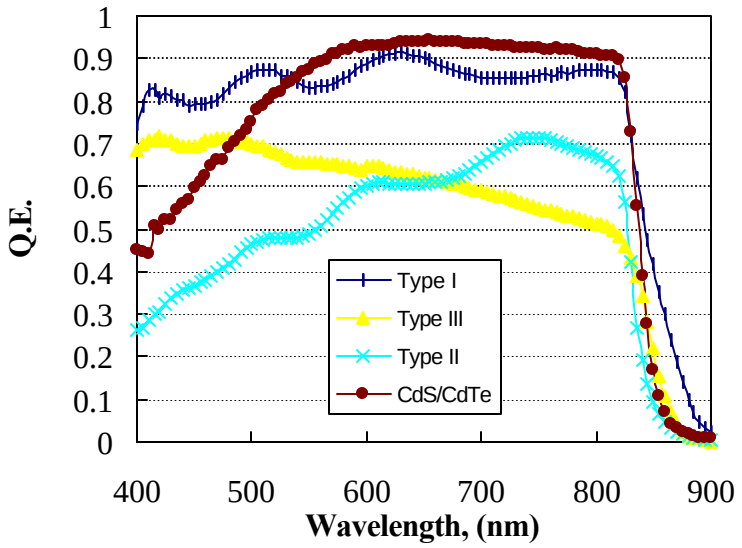



**Figure 11. Typical SR behavior of CdTe/ZnSe junctions.**

**Table 8. Solar cell characteristics of the devices of figure 11.**

| SR Type | $V_{OC}$, (mV) | $J_{SC}$, (mA/cm$^2$) | ff, (%) | Eff., (%) | $R_{sh}$, (W-cm$^2$) | $R_s$ |
|---|---|---|---|---|---|---|
| CdTe/CdS | 840 | 23.0 | 68 | 13.1 | 900 | 1.5 |
| I | 724 | 24.8 | 63 | 11.3 | 1185 | 1.9 |
| II | 560 | 17.0 | 59 | 5.6 | 780 | 2.5 |
| III | 550 | 9.8 | 33 | 1.8 | 54 | 1 |

Devices with SR labeled type II and III exhibited poor solar cell characteristics. Solar cells with SR type I exhibited the best performance. The blue region of the type I response suggests that no ZnSe is present in the front of the device, even though the starting ZnSe thickness was about 800 Å. This response also exhibits a slight shift near the CdTe absorption edge. This suggests that the bandgap of CdTe has decreased most likely as a result of selenium (and Zn) diffusion into this layer. Figure 12 shows the energy gap contours for the $Zn_{1-x}Cd_xSe_{1-y}Te_y$ alloy [8]. No distinct cut-off (corresponding to the ZnSe absorption edge) is present in the blue response of the type II device. It is believed that for the type II device, a compound (the exact composition of

which is unknown) is formed at the front of the cell as a result of interdiffusion between the CdTe and ZnSe layers. This layer, which was visible after removal of the CdTe, does not contribute to the photocurrent of the devices (i.e. electrically inactive). Transmission measurements of this film "matched" the SR trend observed in figure 11. For the other two devices (types I and III), it appears that the ZnSe has been completely consumed by diffusing into the CdTe, and the main difference between type I and type III cells is that the type III device suffers from poor collection. Additional work is underway to further understand the behavior of these devices.

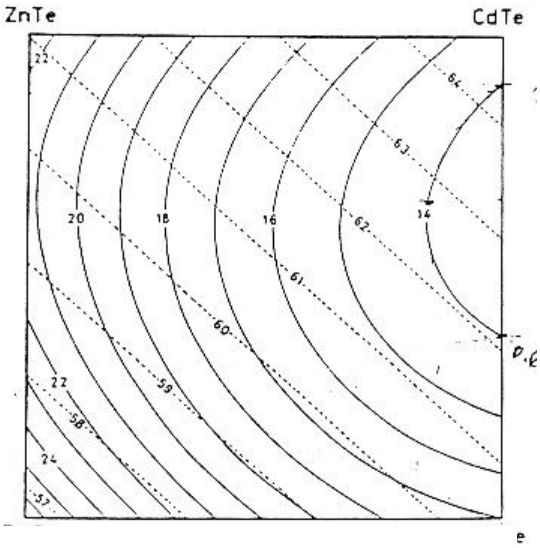



**Figure 12. Energy gap contours of the $Zn_{1-x}Cd_xSe_{1-y}Te_y$ system [8].**

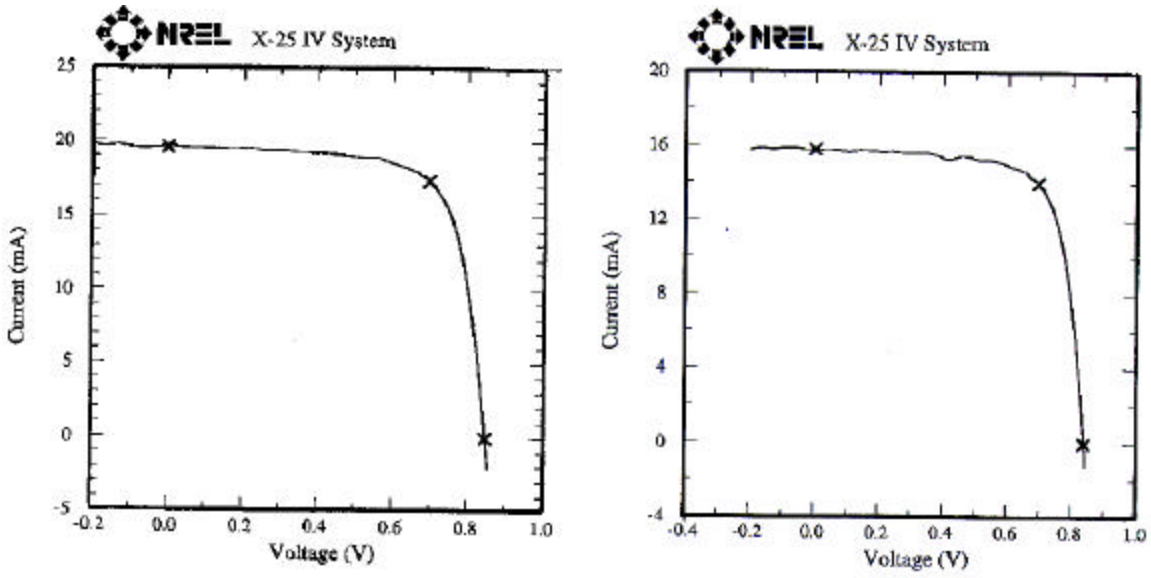
## CSS CADMIUM SULFIDE

### All-CSS CdTe/CdS Solar Cells

The close spaced sublimation is currently used for the deposition of both semiconductors, and all-CSS devices (Corning 7059) with 14.2% efficiencies were reported during phase I. During phase II, all-CSS devices have reached efficiencies of 15.0% on Corning 7059 glass substrates. The process was transferred to LOF substrates and an efficiency of 14.3% was demonstrated. The light I-V and SR of the two devices are shown in figures 10 and 11 respectively. The solar cell characteristics for these two cells are listed in table 9.

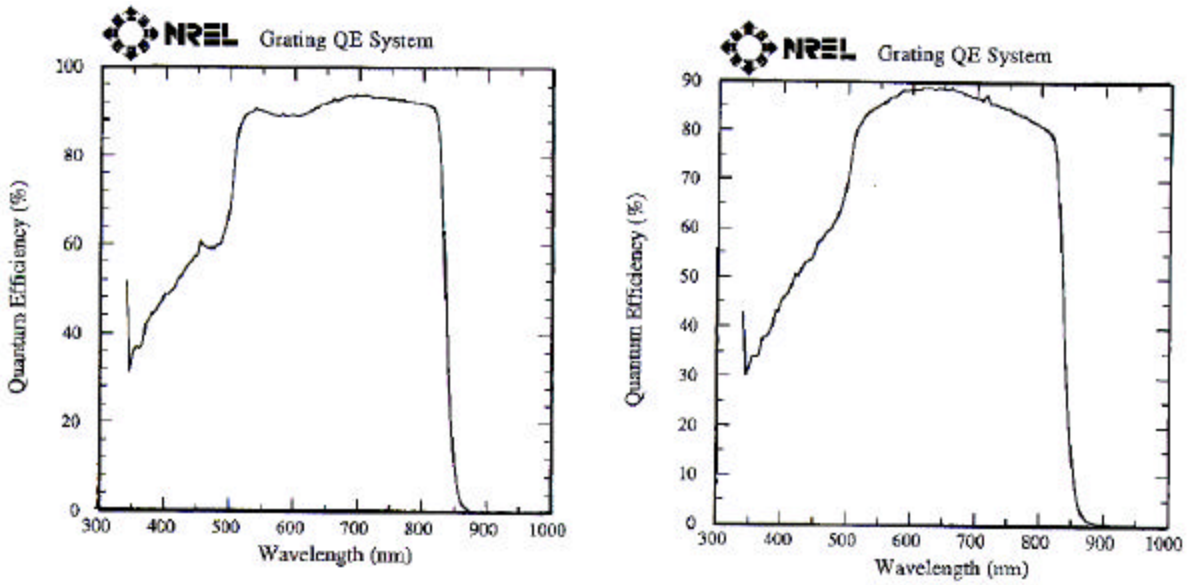
**Table 9. Solar cell characteristics of the devices shown in figure 13.**

| Glass Substrate | $V_{OC}$, (mV) | $J_{SC}$, (mA/cm$^2$) | ff | Efficiency, (%) |
|---|---|---|---|---|
| Corning 7059 | 848 | 24.16 | 73.1 | 15.0 |
| LOF | 839 | 23.11 | 73.5 | 14.3 |




(a) (b)

**Figure 13. Light I-V of all-CSS CdTe/CdS solar cells fabricated on (a) borosilcate and (b) LOF glass substrates.**




(a) (b)

**Figure 14. SR of the CdTe cells shown in figure 13.**

The main difference in the two devices lies in their SR. The SR of the device fabricated on the borosilicate glass substrate exceeds 90% for all wavelengths below the CdS bandgap. The SR of the LOF device is limited below 90%, and shows a gradual decrease toward longer wavelengths; this behavior is related to the optical properties of the LOF

substrate. In both cases the cut-off at 510 nm is sharp suggesting that interdiffusion between the CdTe and CdS is negligible.

**Photoluminescence Measurements**

During phase I the focus was on understanding the deposition process itself and optimizing it for optimum solar cell performance. During phase II a study of the CSS CdS films after heat treatments was undertaken, in order to understand the changes undergone by these films under various annealing conditions. CSS-CdS films were annealed in inert ambient (He), in $H_2$, or in the presence of $CdCl_2$ vapor. The PL spectra of several CSS-CdS films annealed in the presence of $CdCl_2$ vapor is shown in figure 15. As a result of the heat treatment, the intensity of the band located at 620 nm, and which has been previously attributed to sulfur vacancies, increases as the annealing temperature increases. These results appear to be in good agreement with previous work that suggested that 470°C is a critical temperature above which thermal creation of sulfur vacancies takes place [9].

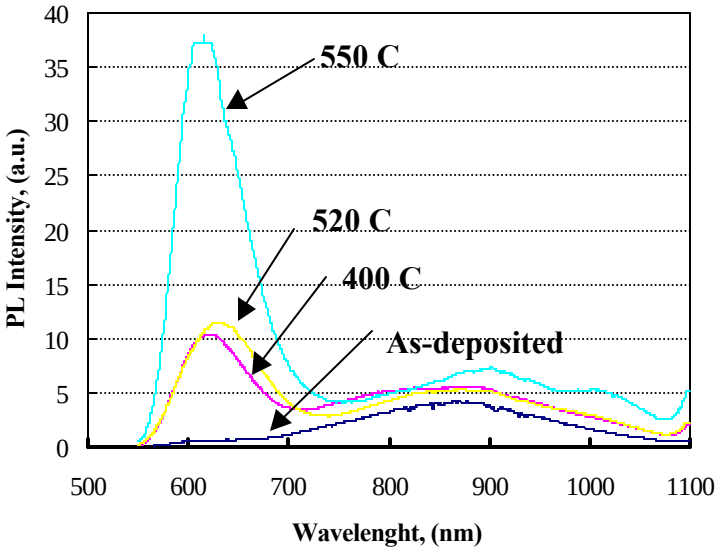



**Figure 15. The PL spectra of CdS(He) films annealed in $CdCl_2$ vapor.**

PL measurements of CdS($O_2$) films included in the phase I report, showed a *decrease* in the intensity of the sulfur vacancy band suggesting a reduction in the concentration of sulfur vacancies [10]. At that time this was believed to be a possible reason for the better solar cell performance obtained with CdS($O_2$) vs. CdS(He) films. The above annealing experiments suggest that heat treatment of the CdS(He) films leads to an *increase* in the intensity of the same PL band. Yet state-of-the-art performance has been demonstrated with devices fabricated with CdS($O_2$) films and with CdS(He) films subsequently annealed in $CdCl_2$. Therefore the current results suggest that the above defects have no significant effect on solar cell performance. It is most likely that the changes undergone

by the CdS films during the cell fabrication process are overshadowing their pre-fabrication properties. Additional studies are underway in this area in order to identify those properties of the CSS-CdS films that are critical to obtaining the desired solar cell performance.

## LOW TEMPERATURE CSS CDTE (LTII) - VAPOR $CDCL_2$ HEAT TREATMENT

Although, under the current program's requirements the deposition temperatures need only be lowered to 550°C, the results obtained from phase I suggested that the CSS-CdTe temperature could be further lowered without considerable loss in performance. During phase II a small area CSS reactor was constructed for the deposition of CdTe films at temperatures below 500°C (CdTe-LTII); the lowest CSS-CdTe temperature used to date is 420°C. The rest of the deposition parameters have been adjusted to yield deposition rates about twice as fast as those used for the typical baseline process. A two zone annealing chamber was also constructed for annealing CdTe/CdS structures in $CdCl_2$ vapor. The CdTe-LTII films are typically heat-treated using either the typical (wet) $CdCl_2$ heat treatment, or the under development vapor treatment. These cells are fabricated using CBD CdS films. Although only a limited number of devices have been processed using the above processing conditions, early results are very encouraging. The characteristics of the two best devices fabricated to date are listed below:

- CdTe(LTII) $T_{SUB}$=480°C/wet chloride treatment:
  $V_{OC}$=835 mV, $J_{SC}$=20.22 mA/cm$^2$, ff=66.0%

- CdTe(LTII) $T_{SUB}$=480°C/vapor chloride treatment:
  $V_{OC}$=790 mV, $J_{SC}$=20.20 mA/cm$^2$, ff=62.2%

It is believed that the above solar cell performance can be improved with further development of the vapor chloride treatment and the CdTe-LTII process.

## CONCLUSION

The efficiencies of all-CSS devices have been advanced for both borosilcate and LOF glass substrates. A disadvantage for all-CSS solar cells vs. those fabricated with CBD CdS remains the fact that it has not yet been possible to utilize the same small thicknesses for the CSS-CdS; the typical reduction in $V_{OC}$ and ff occurs at larger thicknesses when CSS-CdS films are used. Devices fabricated with CSS-CdS(He) films that have been heat treated in the presence of $CdCl_2$ vapor have exhibited the same performance previously achieved with CSS-CdS($O_2$) films. However, the PL behavior of these two types of CSS CdS films is considerably different. Films deposited in $O_2$ have shown a reduction in the concentration of sulfur vacancies, while films deposited in He and annealed in $CdCl_2$ have shown an increase in the concentration of sulfur vacancies.

Further work is underway to better understand whether sulfur vacancies in CdS have a significant impact on device performance.

Zinc oxide films doped with aluminum have been used for the fabrication of solar cells. Results obtained to date have suggested that the current "optimum" solar cell fabrication processes are incompatible with these films; the presence of $O_2$ during the deposition of the CdS films leads to a large increase in the resistivity of the ZnO films. SR measurements have indicated that CdTe/CdS/ZnO cells can achieve 90+% quantum efficiencies (without AR coating). Most work described in this report has focused on the influence of the CdS deposition on the properties of the ZnO films. It is possible that the CdTe deposition process, which in some cases is done in oxygen, can also influence the properties of the ZnO films. Since the CdS films used for the ZnO cells were at least 1000Å, they may have protected the ZnO films from any effects that the CdTe deposition process could have on them. Based on the device performance obtained on ZnO:Al/glass substrates, it is believed that low temperature and "oxygen free" processes, such as sputtering and physical vapor deposition, could successfully incorporate ZnO as the TCO for CdTe solar cells. Since most of the processing options currently being developed emphasize low temperatures, and do not utilize oxygen, it is believed that when these are optimized ZnO can be successfully used for the fabrication of high efficiency CdTe solar cells.

A vapor $CdCl_2$ treatment has been implemented and has produced encouraging results for CSS-CdTe deposited at temperatures below 500C. This process is not yet optimized, and additional work is underway to improve the performance of these devices.

## REFERENCES


1. R. Gordon, "Deposition of Transparent Conducting Oxides for Solar Cells", 14th NREL/SNL PV Program Review, AIP Conference Proceedings 394, pg. 39.

2. D. L. Morel and C. S. Ferekides, "Advanced Processing of CdTe- and $CuInGaSe_2$-Based Solar Cells", Annual Report, NREL Subcontract No. XAF-5-14142-09 (1996).

3. S. Zafar, C. S. Ferekides, and D. L. Morel, J. Vac. Sci. Technol. A 13 (4), (1995)

4. T. Minami, S. Takata, Japanese J. Appl. Phys., 30, 814, (1991).

5. C. S. Ferekides, D. Marinskiy, S. Marinskaya, B. Tetali, D. Oman, and D. L. Morel, "CdS Films Prepared by the Close Spaced Sublimation and their Influence on Solar Cell Performance", Proc. 25th IEEE Photovoltaic Specialists Conf., pp. 751-756, (1996).

6. D. Cheung, Ph.D. Thesis, Stanford Univ., (1975)

7. W. G. Oldham, and A. G. Milnes, Solid State Electron., 6, p. 121, (1963)

8. I. Toshiyuki, J. of Electronic Materials, vol. 9, 5, (1980).

9. J. Nishimura, J. Appl. Phys., 30, 537, (1991).

10. C. S. Ferekides, D. Marinskiy, and D. L. Morel, "CdS: Characterization and Recent Progress in CdTe Solar Cell Performance", Proc. 26th IEEE Photovoltaic Specialist Conf., pp. 349-352, (1997)

## LIST OF FIGURES

## LIST OF TABLES

**PART II: CIGS**

## INTRODUCTION

During Phase I of this project we accomplished a substantial advancement in performance as a result of the introduction of Ga into our manufacturing-friendly process. Although we made initial observations on the behavior of Ga, it was clear that there was much to be done to understand Ga's role and the optimization of its influence on performance. During Phase II of the project we focused specifically on this issue. More specifically we focused on developing a semiconductor which reliably and reproducibly produced high Jsc's. As will be discussed, this took us in directions in which Ga plays a subtler role than just opening the band gap. *In taking this approach we also were able to achieve what we consider to be a key objective: the ability to optimize bulk and surface properties independently of each other.* Having achieved this objective, we are able to manipulate the surface properties of the absorber while not adversely affecting what is basically a Jsc of 40 $mA/cm^2$. The surface properties are rich in mechanisms, and these mechanisms are very sensitive to process details. We report results on efforts to understand and control these mechanisms, but realize that we are just beginning to sort things out. Nevertheless, we have been able to boost Voc's above 500 mV's on these 40 $mA/cm^2$ base materials and achieve efficiencies of 13%. As will be discussed, these values of Jsc and Voc are approaching the expected limits for these low band gap devices, and the limiting parameter to higher efficiency is the FF.

We also continue our efforts to understand and improve the junction in these devices. We are certain that in our devices the interface that is formed among the absorber surface, CdS and ZnO is key to performance, and that we need to understand and control each of these. We have used a Shockley-Read-Hall recombination model to guide our thinking and continue to find it effective in "explaining" mechanisms. We have also made reactive ZnO junctions directly with CIGS as part of our national team activities. We also report results on the influence of substrates on the properties of ZnO that were also generated as a team activity.

## PROCESS DESCRIPTION

Details of our deposition process have been described previously(1,2). We provide a brief description here for convenience. Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by sputtering or evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 °C. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. Much of what is presented below is for process "PI". In this process the order of deposition of the precursors is Cu/Ga/(In + Se). In process "PII" the order is reversed: (In + Se)/Cu/Ga. ("PI" and "type I" are used interchangeably in the following.) Further details are provided below in the extended discussion. Formation of the semiconductor layer takes about one-

half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by high ρ/ low ρ ZnO.

## EFFECTS OF GA ON $J_{SC}$ GENERATION

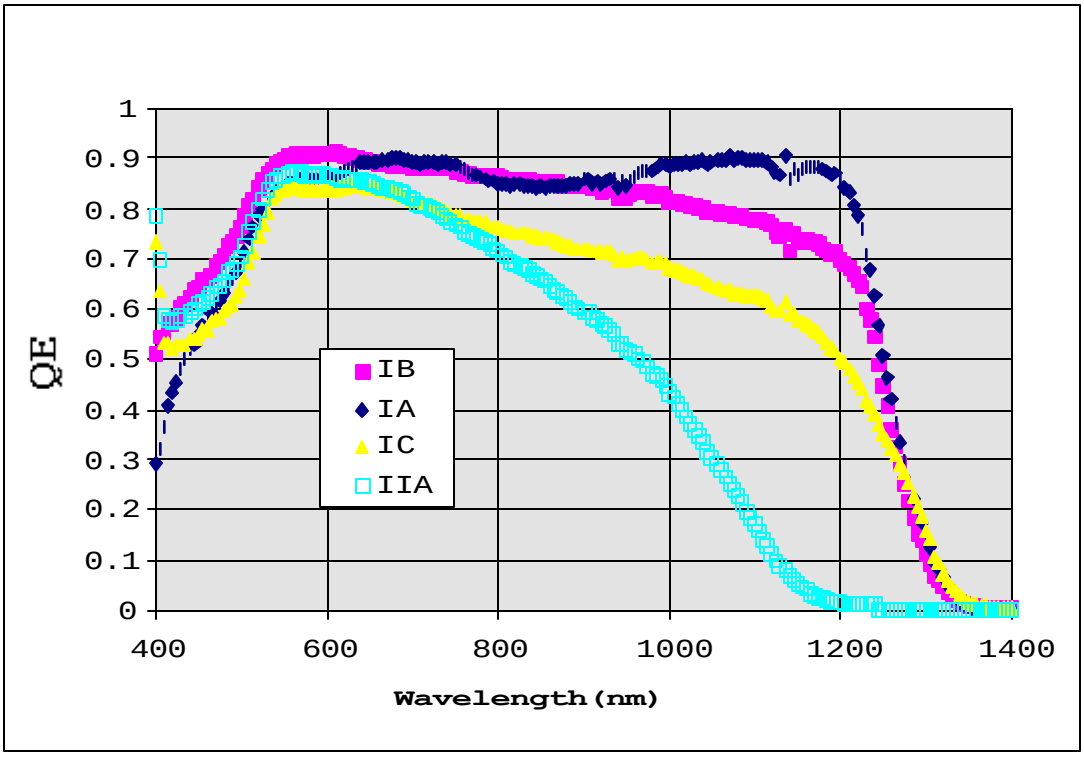



**Figure 1. Quantum efficiency spectra for Type I and Type II devices.**

In our Phase I Final Report we discussed the effect of increasing Ga levels on spectral response in general terms. Basically we reported that we could systematically shift the band gap with increasing Ga, but as the gap increased we observed a disproportionate loss in current. Since then we have concentrated our efforts primarily on understanding the effects of increasing Ga in PI structures in which the band gap is not changed. Representative spectral responses of several type I devices(and a type II) are shown in figure 1. Extrapolation of the absorption edge results in a band gap of .95 eV which is the same as our CIS devices whose spectral response is similar to device IC shown in figure 1. We note that these devices do not have AR coatings, and that the QE is calibrated with NREL calibrated Si and CIS reference cells. The integral of these responses results in the $J_{sc}$ values shown in table 1. The point to be made here is that the judicious incorporation of Ga has increased our current densities by about 5 mA/cm$^2$ over CIS. We offer two perspectives for the role played by Ga. Since the unchanged band gap suggests that it is not present at alloy levels(or at least not chemically bonded) in the space charge(SC) layer, it must be located between the Mo contact and the space charge layer. Assuming that it has chemically incorporated in this region, the resulting larger band gap would form the equivalent of a back surface field(BSF) which would aid the collection of minority carriers. To investigate this possibility we used a spectral response model to fit

the data of figure 1. The model is a straightforward adaptation of the standard formulas found in

| Device | $J_{sc}$ mA/cm$^2$ | Depletion Width(μm) | Diffusion Length(μm) |
|---|---|---|---|
| IA | 39.7 | 1.0 | 2.0 |
| IB | 39.2 | 0.4 | 0.8 |
| IC | 34.5 | 0.3 | 0.3 |

**Table 1.** Device and material properties for type I devices.

Sze(3) including the assumption that carriers generated in the SC region are collected. The biggest uncertainty in our procedures involved absorption constants. We used data from NREL and IEC which had differences between them, and the NREL data even demonstrated that the absorption properties, especially in the rise portion, were sensitive to Cu/ ( Cu + In) ratios. Within the limits of these uncertainties we were able to determine the values of SC width(W) and minority carrier diffusion lengths(L) shown in table 1. An example of a fit using the model is shown in figure 2. There is no attempt at this point to address the complexities of the blue region. We instead are focusing on the rise at the band gap that is sensitive to depletion width and diffusion length. The total curve(□'s) was fit to the data for device IA in figure 1. The ■ 's and ▲ 's show the space charge and

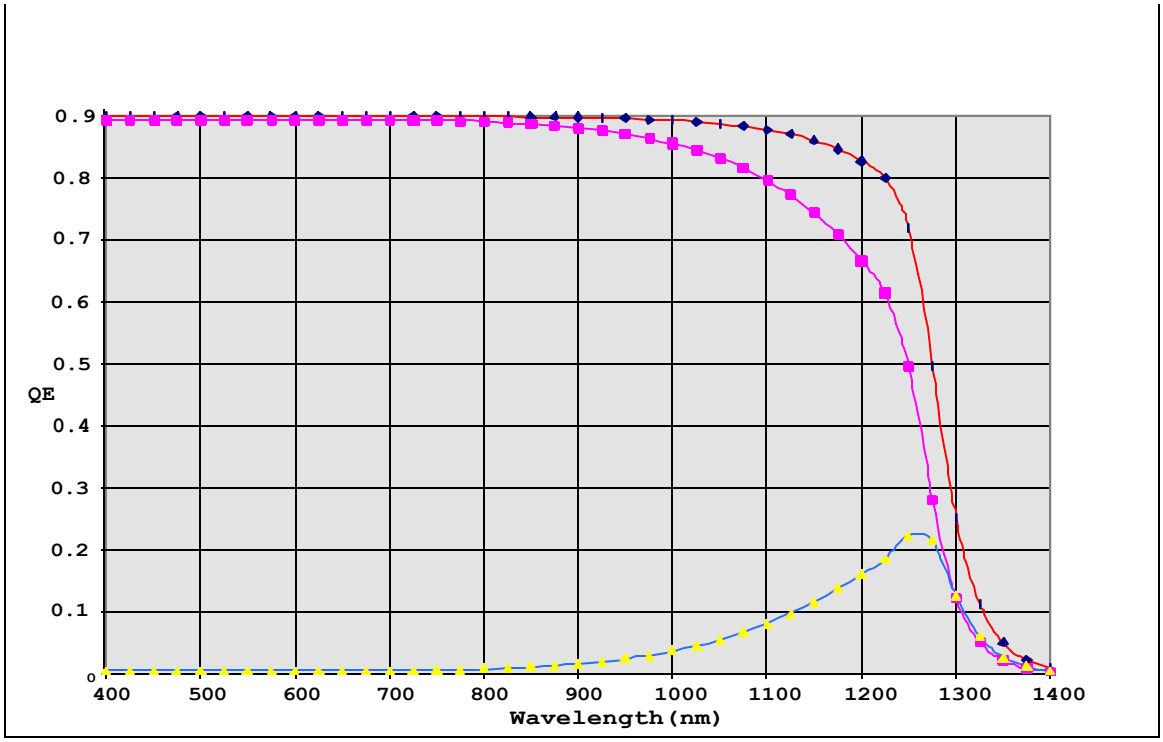



**Figure 2. Overall QE simulation (◆) and contributions from the space charge layer (■) and minority carrier diffusion (▲) for a PI device.**

diffusive contributions respectively. Because of the fast rise of the data at the band edge a large diffusive contribution was required resulting in the large diffusion length's in table 1. Overall collection in PII devices is significantly reduced relative to PI. Determining values of W and L is less precise for these, however, because of greater uncertainties in absorption constants.

We see that for these devices increases in $J_{sc}$ result from increases in both W and L. The increase in L we attribute at least in part to the proposed BSF(==> μE collection). The increase in W leads in to the other proposed role of Ga, that at trace levels it is able to favorably affect the point defect composition. The abrupt rise in QE at the absorption edge in device IA is testimony to the positive influence of Ga. The resulting overall collection length of 3 μm is remarkable in spite of the uncertainties imposed by absorption data, and the high values of $J_{sc}$ reflect that fact.

The range of performance exhibited in figure 1 is the result of variation in the Ga incorporation. We wish to note however, that the high-end performance of devices IA and IB is reproducible and consistent. The reproducibility of the process is demonstrated in Table 2. These results are for a sequence of runs that was conducted over a two-month

| Run | 19 | 20 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|
| Jsc($mA/cm^2$) | 39.2 | 39.0 | 40.0 | 40.5 | 40.1 | 38.6 | 39.7 | 40.3 | 40.5 | 40.7 |

**Table 2. Jsc data for a sequence of runs showing the consistency over a two-month period.**

period. Missing runs 21,22 and 30 were a different process recipe or were runs for which there was an equipment failure and are not part of the sequence. The devices do not have AR coatings. The consistently high Jsc's over this sequence of ten runs clearly demonstrates the heartiness of this process. We also note that in many of these runs process parameters at the end of the run were intentionally varied to improve Voc. The fact that the Jsc's consistently stayed in the same (high) range even though we varied the parameters at the end of the run not only demonstrates reproducibility, but also that the surface and bulk can be independently optimized.

This solid and reliable current generation thus provides a firm foundation for studying and advancing $V_{oc}$ and FF performance. Device IB had a FF of .66 and $V_{oc}$ of .463 resulting in an efficiency of 12.0%. These values of FF and $V_{oc}$ represent significant improvements over CIS as well. In this case we attribute the effect to reduction of recombination near the metallurgical junction. Thus trace levels of Ga are operative throughout the SC layer and are improving the microstructure. To examine this issue more closely we use the SRH model to fit $J_{sc}$- $V_{oc}$ data from a representative PI device as shown in figure 3. The two sets of data points are measurements going up and down in intensity to look for hysteresis caused by trapping. The parameters used in the calculations are from direct measurements and from representative literature values for

difficult parameters such as cross sections. While these limit the accuracy of the calculations, relative comparisons are meaningful.

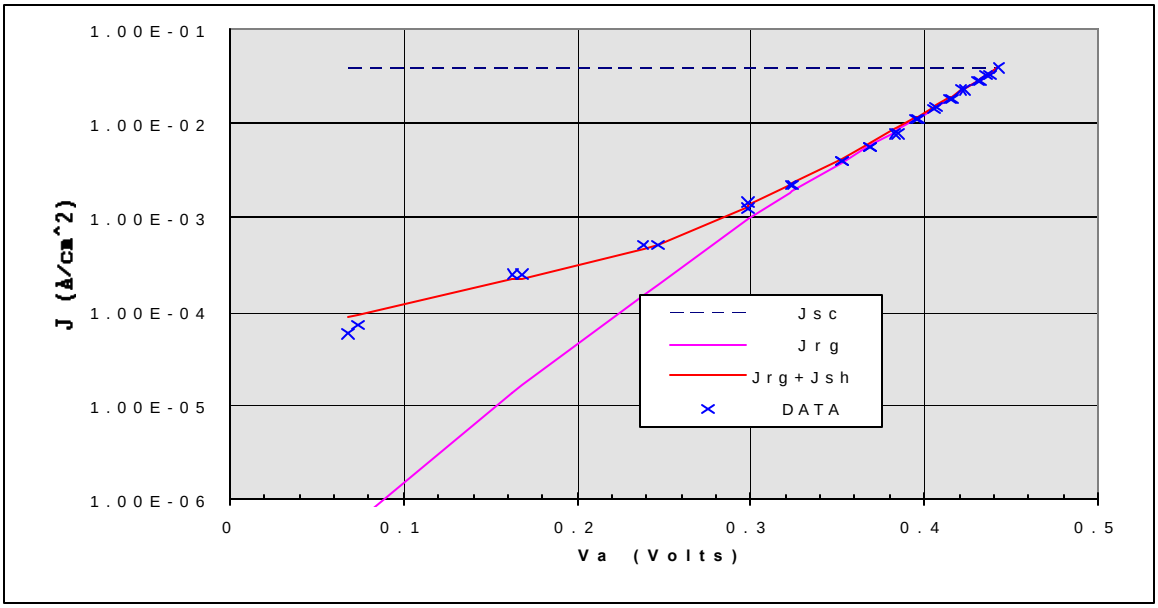



**Figure 3. Fit to Jsc-Voc data for a type I device. The dashed line is Jsc at one sun. The lower line is the modeling curve without including shunting. The line through all of the data points includes a shunt contribution to current.**

For example, the recombination lifetime for the device in figure 3 is found to be 7.1 x $10^{-9}$ s from the fit. This is in good agreement with direct measurements of lifetime in companion devices by the DBOM technique at UF Gainesville.

To help build our understanding of these complexities we have furthered the development and effectiveness of the SRH recombination(4) model under the auspices of another NREL -sponsored project. Application of the model from a series of samples reveals interesting information about the effect of run parameters. In figure 4 we show I-V curves from Jsc-Voc measurements for a PII run. This process results in more Ga incorporation in the space charge layer and a higher and more dynamic Voc. The four devices are from the same run and received increasing Se flux from left to right due to the intentional gradient. The difference in flux level from left to right was about 10%. The solid lines are from the model. The fit does not match the data at low voltages because shunting dominates behavior in that region. The region of importance is the high voltage region. Because Jsc-Voc eliminates Rs, the data represents actual diode behavior. Results of the analysis are summarized in Table 3. As can be seen, Voc increases systematically with

| | Increasing | Se | → | |
|---|---|---|---|---|
| τ (ns) | 0.42 | 0.71 | 2.0 | 2.8 |
| Voc(mV) | 430 | 455 | 505 | 520 |

**Table 3. Voc and lifetime dependence on Se flux for PII devices.**

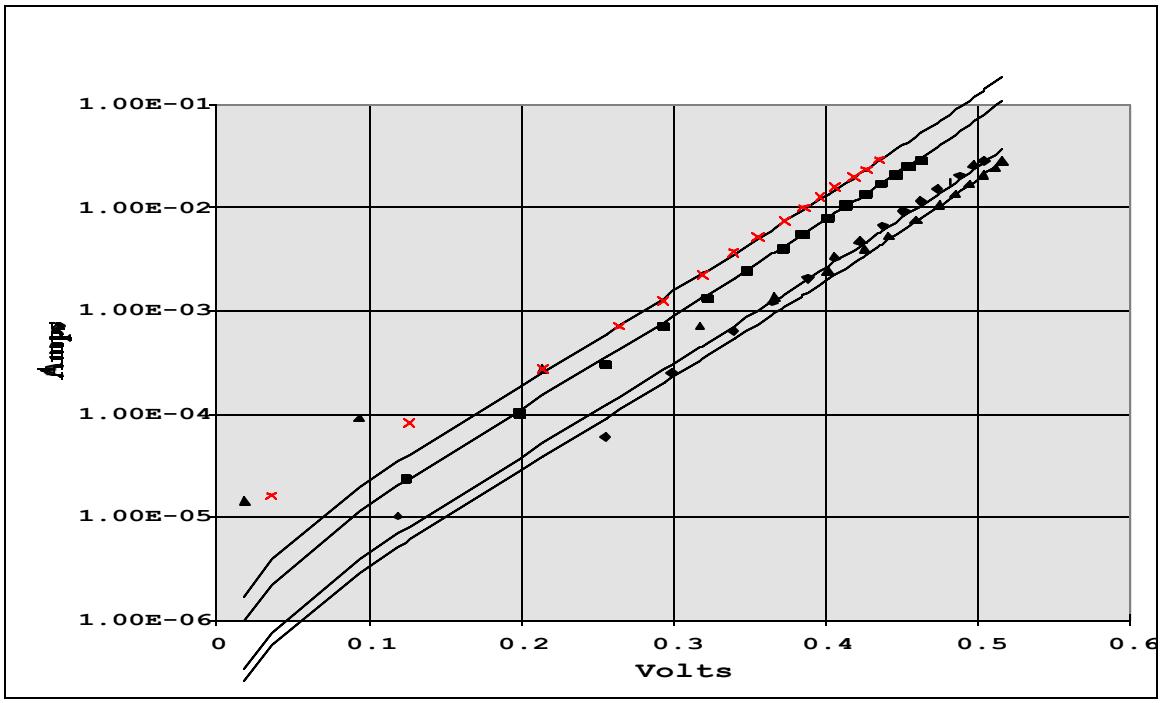



**Figure 4. Jsc-Voc for a PII device. Se flux is increasing from left to right.**

increasing Se flux, as does the primary fundamental variable determining Voc, the recombination lifetime. Additional analysis indicates that the recombination is taking place in the top of the space charge layer near the metallurgical junction. Thus the Se flux of importance for Voc in this case is that at the end of the growth which only affects the near surface region. The band gap and Jsc for these devices were 1.09 eV and 28 mA/cm$^2$ respectively and were independent of the Se flux confirming the separation of surface and bulk properties.

## EFFECTS OF PROCESSING ON GA INCORPORATION

In terms of theoretical efficiency it is clear that Ga should be used to increase the band gap to the 1.4 eV range, and the highest reported efficiencies are for CIGS with band gaps in the 1.1 - 1.2 eV range. As seen in figure 1, for type II devices we are able to shift our band gap into this range. This results from depositing Ga after In in our process sequence. General observations suggest that Ga migrates towards the back of the device and In towards the front. Thus in order to incorporate alloy levels of Ga in the SC region it is necessary to place the Ga in that vicinity during the critical formation stage of that region. In addition, the details of the processing conditions during Ga incorporation determine its bonding effectiveness. We feel that the downward slope in the spectral response for device IIA seen in figure 1 is due to incomplete Ga incorporation. That is, poorly or unbonded Ga is deteriorating transport properties. The corresponding slope in device IC may be due to the same effect. Although type I devices only have trace quantities of Ga in the SC layer, as these are increased toward the alloy level we see the onset of the downward slope prior to band gap changes. Since codeposition processing does not reveal as strong an effect on the slope as we observe, at least at Ga levels below about 20%, this is not a fundamental problem but a process-dependent problem. We have

recently made small modifications to our process and are observing improvements in these slopes.

To study the effects of increasing Ga incorporation on performance we find it useful to create Ga gradients in a single run so that we can be certain that uncontrolled run-to-run variables are not operative as is the case when comparisons among different runs are made. Nevertheless in such comparisons we have observed that Ga behavior can be strongly influenced by the overall environment. Under a given set of conditions we can desensitize the semiconductor formation to Ga levels and achieve uniform Jsc's across the entire substrate. This regime is also one in which we achieve the excellent run-to-run reproducibility indicated in Table 2. By adjusting the deposition conditions, however, we can make semiconductor formation very sensitive to Ga levels. This affords us an ideal situation for studying Ga incorporation phenomena.

The layout for our runs is shown in figure 5. The substrate is 2" x 2" , and we deposit a 5 x 5 array of ZnO dots across this area to allow evaluation of the effects of gradients. In order to sensitize semiconductor formation to Ga we have pushed the Cu/In ratio to 1 near the center. Thus to the left of center on the Cu side Cu/In > 1 which forces the admission of Ga into the matrix. The Cu/In ratio varies by 10 % across the 2" stretch of the substrate; Ga has a similar gradient, while that for Se is a bit larger. The range of band gaps resulting from this procedure is represented in figure 6 in the QE spectral response for several of the devices(note that AR coatings were not used). Two observations from the QE spectral response curves are that a range of slopes is observed for devices with the same Eg( about 0.97 eV, the same as CIS), and that those with a significant shift in Eg have a steeper slope. Previously we speculated that these slopes were due to improper

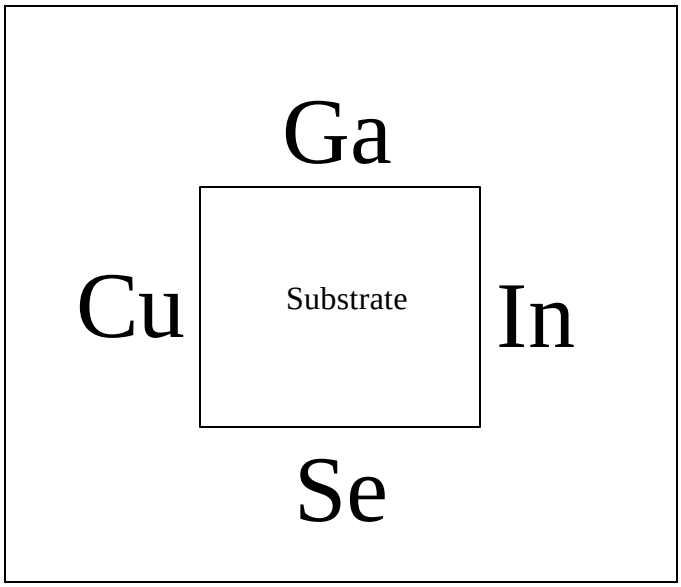



**Figure 5. Arrangement of sources around the 2" x 2" substrate.**

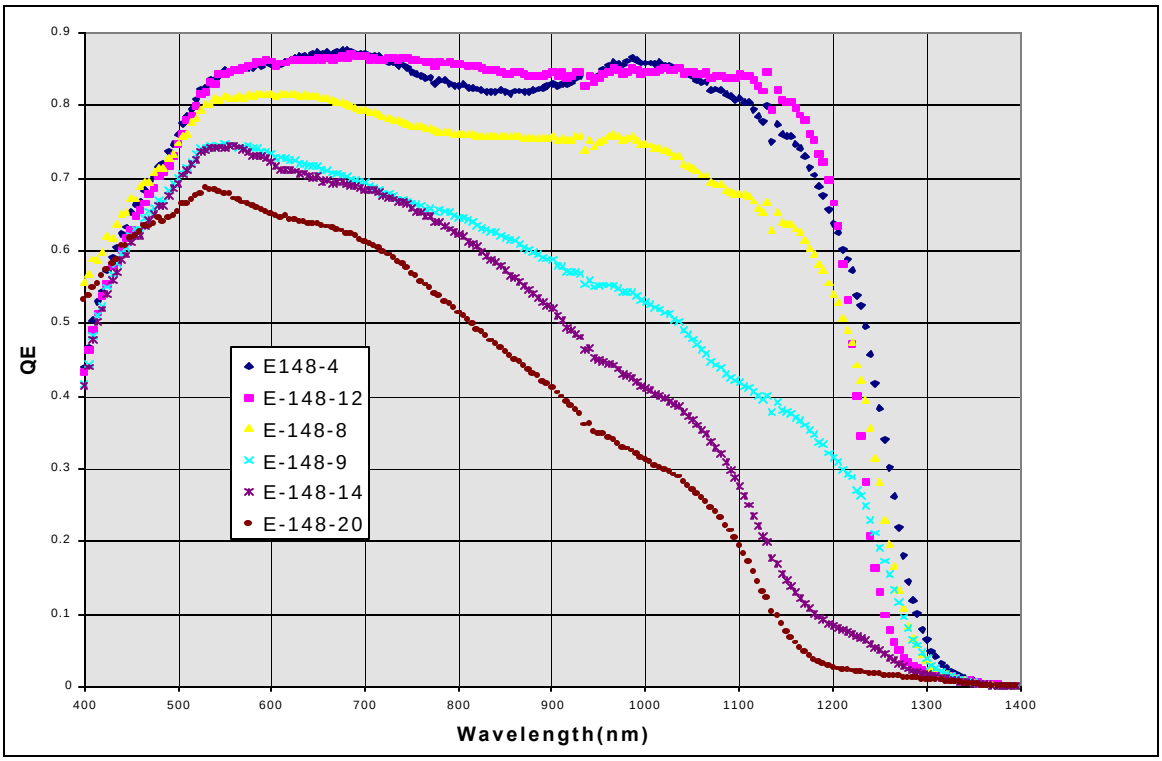



**Figure 6. QE spectral response for several devices from run 148.**

incorporation of Ga and a resulting adverse influence on transport properties. The fact that this data is all from the same run eliminates run to run uncertainties and allows a closer look at these phenomena. The effect of the gradients on the resulting band gap is shown in Fig. 7. As can be seen, the In - Ga corner(near 5,S5) has higher band gaps, while the

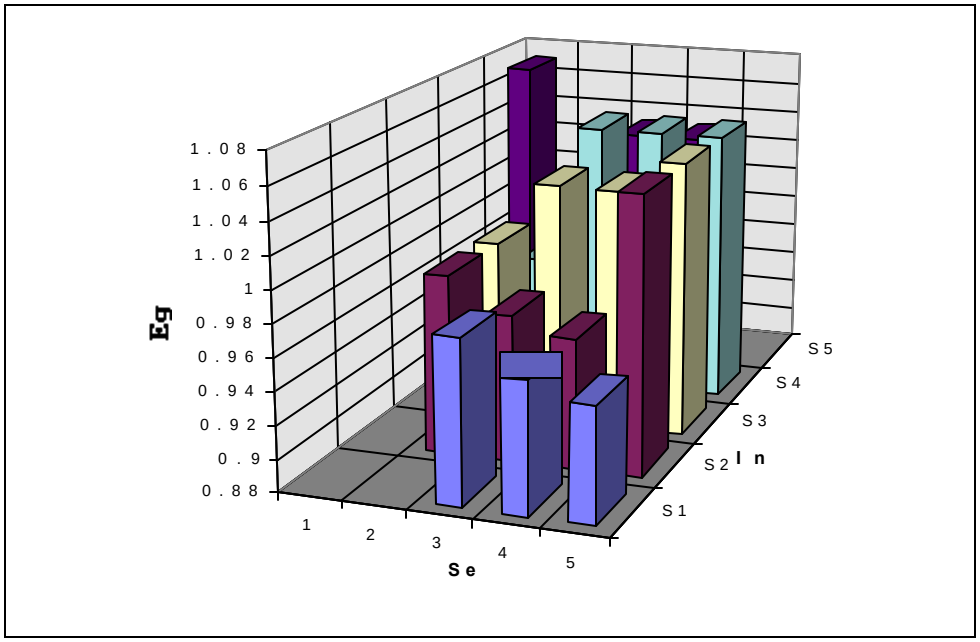



**Figure 7. Band gap profile for run 148.**

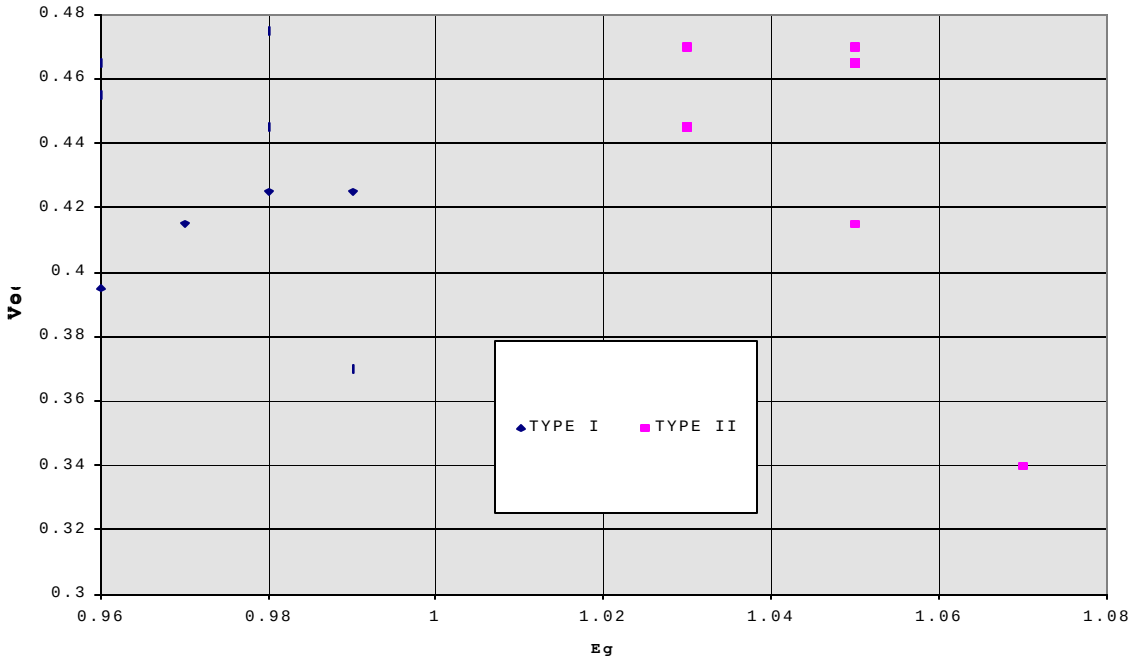



**Figure 8. Voc versus Eg for run 148.**

Cu- Se corner(near 1,S1) has the low CIS band gaps characteristic of Type I devices. If a diagonal is drawn from corner to corner(1,S5 to 5,S1), Type I devices with $0.96 \leq$ Eg $\leq$ 0.99 eV are found on one side, and devices with $1.03 \leq$ Eg $\leq$ 1.07(Type II) on the other. In rows 1 and 2 the absence of data is due to the high Cu level which resulted in shorted devices. As we proceed toward increasing In on the Se side of the diagonal we see typical Type I band gaps. Since the Cu/In ratio is basically constant along a Se - Ga row, we expect the influence of Ga to be more prevalent on the Ga side. While it is, it seems to influence Eg more near the In source than away from it. For example if we look at datum (4,S2) in Fig. 7, we might conclude that Eg is low because there is too little Ga available. However, datum (5, S2) has the same Ga level but exhibits the high Eg. This suggests that under these deposition conditions effective bonding of Ga is a function of the Cu/In ratio and the Se environment. These complex growth interrelationships must be understood if manufacturing- friendly, layered growth processing is to succeed.

The dependence of Voc and Jsc on Eg for these devices is shown in Figs. 8 and 9. Although Eg increases by up to 90 mV for the Type II devices, there is no net increase in Voc. Thus the increase expected from the larger Eg is compensated by other losses such as lower Jsc and increases in Jo. The behavior of Jsc in Fig. 9 is more revealing. The dashed line is a least squares fit to the Type I data points. As can be seen, Jsc appears to increase with Eg. The solid curve is a fit to the Type II data. In this case there is a negative dependence on Eg, and extrapolating the curve to the Type I region suggests a match up to that data as well. Needless to say, the observed drop in Jsc with increasing

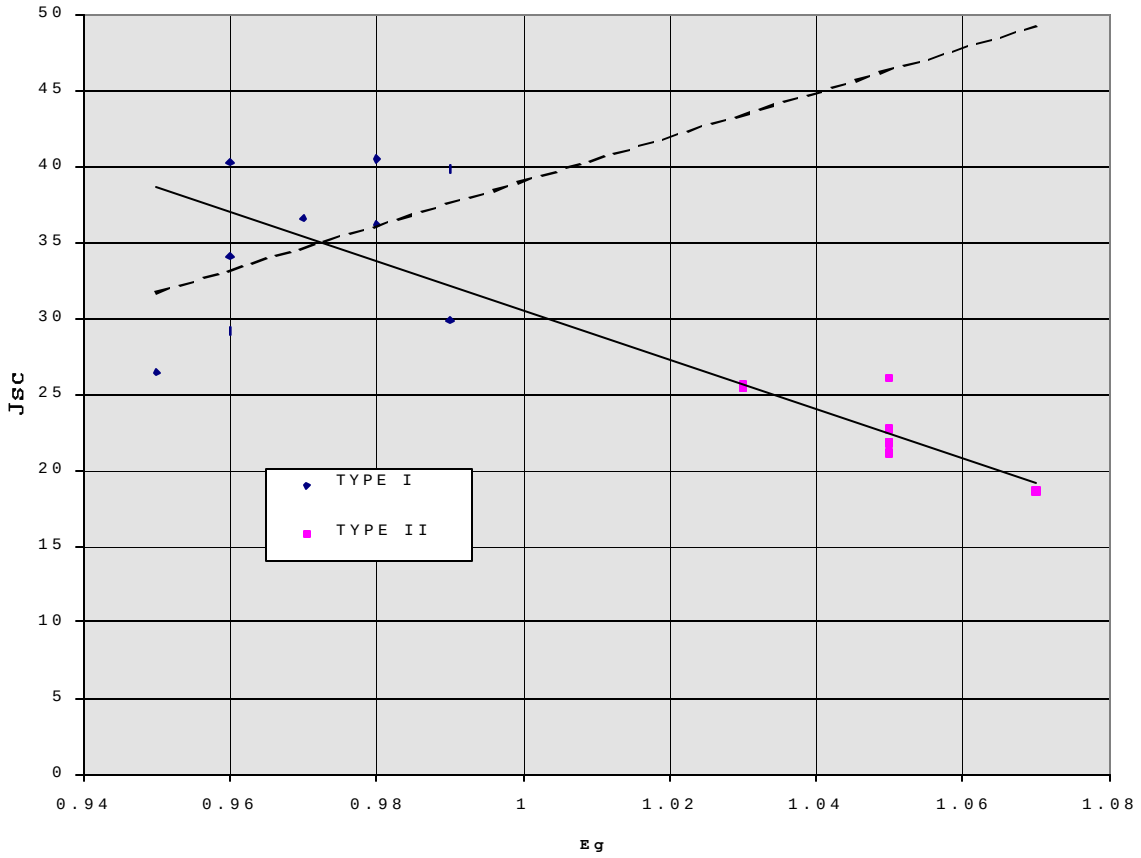



**Figure 9. Jsc versus Eg for run 148.**

Eg in crossing from Type I to Type II devices is much larger than that expected from band gap considerations alone.

At this point it is appropriate to refer to the gap of about 40 mV between the Type I and Type II data. This can be seen in Figs. 8 and 9 as the absence of data in the range 0.99 < Eg < 1.03 eV and is very noticeable along the diagonal in Fig. 7. In considering the reasons and implications for this gap we must remember that Eg is determined by measuring QE spectral response and is thus the effective Eg in the space charge layer. Nevertheless, it is no less remarkable that the effective Eg in the space charge layer jumps by a minimum of 40 mV as soon as some critical combination of Cu/In and Se environment is crossed as discussed above. This change occurs over a distance of 5 mm, the spacing between devices.

The range of Cu/Group III ratios exhibited in figure 7 goes from Cu- rich in the (1,S1) corner to stoichiometric along the (1,S5 - 5, S1) diagonal to Group III-rich across the diagonal. The abrupt rise in Eg in crossing the stoichiometric boundary toward the Group III-rich region suggests transition to new energy configurations associated with lattice structure and is reminiscent of the order/disorder behavior observed for CGS. The bottom line is that the 40+ mV upward shift in band gap results in poorer performance, primarily in Jsc. Because of the manner in which we have incorporated the Ga to accomplish the

band gap shift we strongly suspect that we have an inverted band profile with a low band gap(0.95 - 0.98 eV) region behind the front high gap(1.03 - 1.08 eV) region. This significantly diminishes minority carrier collection resulting in lower Jsc's.

Evidence for the hypothesized inverted bands is found by examining the QE responses in figure 6. Devices 4,12,8, and 9 are Type I devices whose absorption edges intersect the wavelength axis in the 1250-1300 nm. Devices 14 and 20 have absorption edges that are clearly shifted to the 1150 - 1200 nm range, however they also exhibit a tail that extends out to the 1250-1300 nm range. This tail range is most evident in device 14. The "bump" that is observed is interpreted as the presence of a low band gap ( 0.97 eV) region at the back of the space charge layer. The front of the space charge layer has an Eg $\cong$ 1.04 eV. This differential of 70 mV in the band gap that is in the wrong direction for minority carrier collection is felt to be largely responsible for the large drooping slope in the QE response for these devices and the resulting losses in Jsc.

While this region of the device is revealing, it is not a pathway to improved performance. However, there are additional affects associated with low level Ga incorporation on the "Type I" side of the device that are of interest. As seen in figure 6 devices 4,8,9 and 12 are all Type I in that they have a low band gap. It is apparent, however, that there are significant differences in QE behavior. Device 4 may be taken as the base case as it is safely within the Type I zone. Allowing for the interference fringes due to ZnO reflections it has a "square" QE response and resulting Jsc of about 40 mA/cm$^2$. Device 12 is on the energy gap transition border. It exhibits about a 30 mV increase in Eg while maintaining a square QE profile. This might be thought of in terms of a decreased Cu/In ratio as well as to incorporated Ga. Devices 8 and 9 are also on the border and have increasing downward sloping QE profiles suggestive of varying degrees of ineffective Ga incorporation. It is noteworthy that the slope of device 9 is comparable to that of its neighbor just across the border, device 14. Since there is no evidence for inverted bands in device 9, this strongly suggests that other factors are affecting minority carrier collection as well.

To better understand the behavior of Jsc with Eg exhibited in Fig. 9 we performed extensive capacitance measurements on the devices and combined these with modeling approaches. Given the complexities of these devices it is not straightforward to determine film and device properties from capacitance measurements. The influence of traps on the measurements is of particular concern(5). However, in cases as these where comparisons between devices can be made, useful results can be attained. A measure of the influence of traps on the space charge width is the change in width under illumination. This is shown in figure 10. All measurements were taken in the 500 - 1000 kHz range. As can be seen, the data is clustered in the range 1000 – 1500 Å in the dark with a corresponding range in the light of 40 - 1000 Å . These are primarily Type II devices. Type I devices go out to several thousand Å in the dark and up to 2500 Å at 1 sun. There is clearly a correlation between light and dark, and the least squares fit indicates an approximate ratio of about 2.5/1. Ahrenkiel(6) has proposed a qualitative relationship between C and performance, and these results are in general agreement with his findings. We also note that the depletion widths as presented are actually a lower limit. That is, as pointed out in

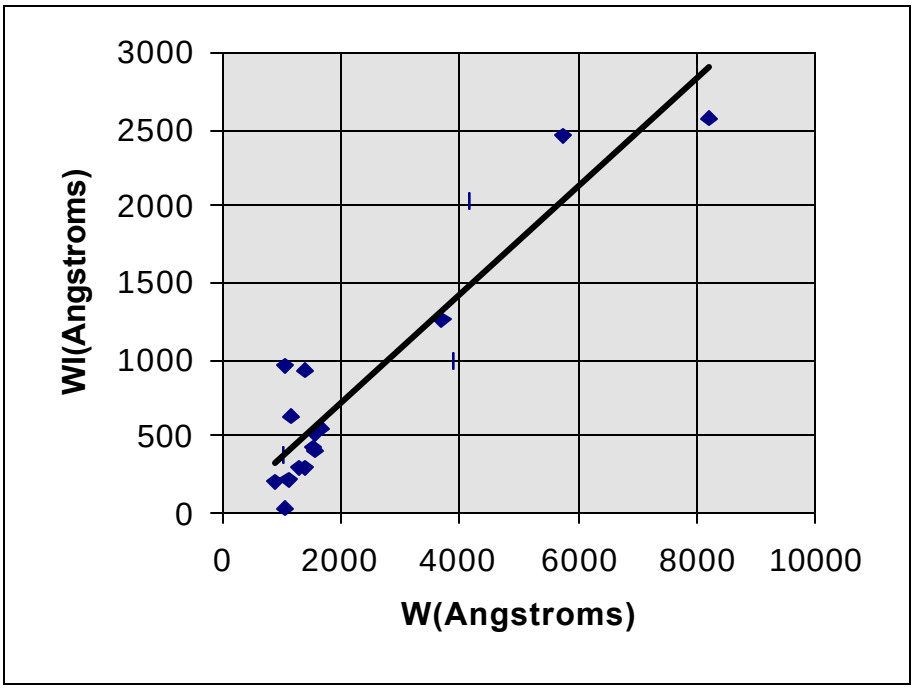



**Figure 10. Depletion width at 1 sun versus dark depletion width.**

reference(5) in thepresence of deep states capacitance measurements yield an effective width, which is a function of the number and location of traps. To provide further insight in Fig. 11 we show the dependence of depletion width and diffusion length from modeling on Eg. The dashed trend line is for the diffusion length and supports the observed Jsc rise with Eg for the low band gap devices as well as the drop as the 40 eV threshold is crossed. Depletion width is seen to follow a similar trend. This suggests that

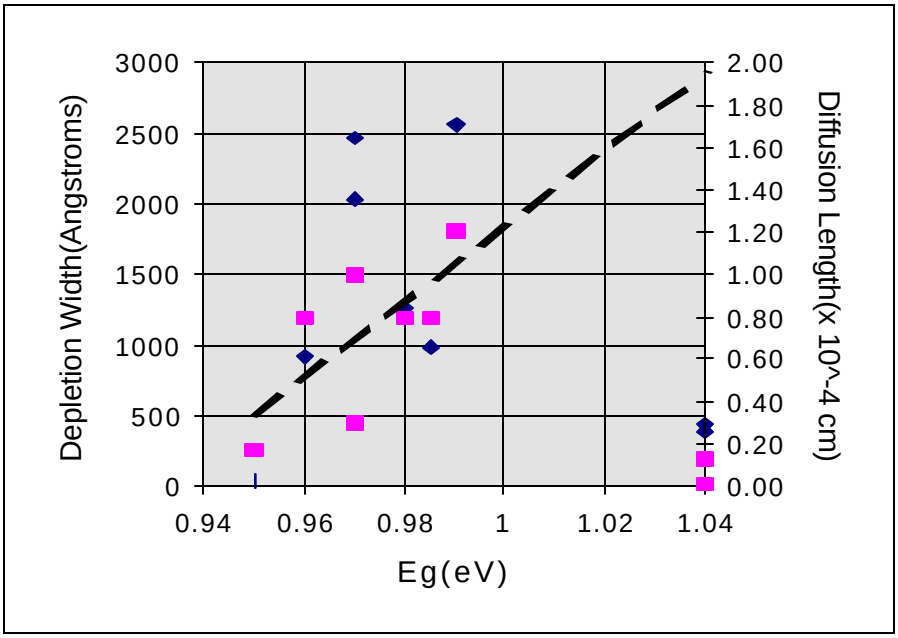



**Figure 11. Depletion width(◆)and diffusion length(■) versus Eg.**

the same defect is controlling both of these important fundamental parameters and that judicious incorporation of small quantities of Ga in the space charge layer is able to passivate the defect.

## PERFORMANCE PROJECTIONS

In Table 4 we show the parameters of our current best device and expectations for

| | Jsc(mA/cm$^2$) | Voc(mV) | FF | Efficiency |
|---|---|---|---|---|
| Current Best | 40 | 510 | 0.64 | 13 |
| Eliminate External losses | 41 | 510 | 0.72 | 15 |
| Optimize Junction | 41 | 520 | 0.75 | 16 |

**Table 4.** Projected efficiencies

improved performance. Improvements in FF will clearly dominate our efforts. We are presently in a data-taking mode to determine the origins of FF weakness. Our observations thus far suggest small contributions from a number of factors rather than one overriding mechanism. Since we have already achieved FF's up to 0.73 in other(Type II devices), we have an existence proof that our contacts can be efficient. The surface of the semiconductor in our Type II devices, however, is notably smoother than those of Type I devices. This suggests that shunting across the CdS/i-ZnO layer might be more prevalent in Type I devices. There are notable differences between the two at the Mo contact as well. In Type II devices the Mo is exposed to a higher level of Se flux than Type I. While this has generally resulted in adhesion problems, in our current Type II devices adhesion is superior to all other processes. We suspect that we have tuned the process parameters to a point where the reaction of Mo with Se flux is causing the formation of a favorable bonding arrangement. This may also reduce or eliminate contact resistance at the Mo interface.

As indicated above we routinely achieve Jsc's in the 40 mA/cm$^2$ range without AR coatings. The projected increase to 41 mA/cm$^2$ will result from minor tuning of the ZnO layer. Additional increases could result from use of an AR coating.

Elimination of externally caused shunts and series resistance will have the biggest effect on performance. Elimination of these will result in an improvement of FF's above the .70 level. As discussed above we expect to accomplish this in part by transferring techniques from our Type II process that contribute to low Rs and Rsh. These techniques involve aspects of the device outside of the junction region and are not expected to adversely affect junction performance.

Once these externalities are controlled we will concentrate our efforts on refinements to the junction region. In particular, we will focus our efforts on reduction of recombination in the interfacial region. Our experimental results to date indicate a complex interplay with these states by Ga, and this insight will guide our efforts. Effective control of recombination will reduce losses in the knee of the IV curve and allow FF's above 0.75.

In addition, small increases in Voc will follow. This will raise device efficiency to the 16% level. We believe this to be an achievable intermediate goal for our process. Given the manufacturing advantages that this process offers, we feel that achievement of this objective would provide a very favorable manufacturing option.

## REFERENCES


1. G. Attar, A. Muthaiah, H. Natarajan, D. Nierman, S. Karthikeyan, S. Zafar, C. S. Ferekides and D. L. Morel, "Development of Manufacturable CIS Processing", Proceedings of the First World Conference on Photovoltaic Energy Conversion, Hawaii, December, 1994, p. 182.

2. S. Zafar, H. Sankaranarayanan, A. Jayapalan, R. Narayanaswamy, C. S. Ferekides, and D. L. Morel, "The Use of Ga in Two-Step Processing to Optimize the Electronic Properties of CIGS Solar Cells", Proceedings of the 26th IEEE Photovoltaic Specialists Conference, Anaheim, September, 1997.(Also see Phase I Report for this project.)

3. S. M. Sze, Physics of Semiconductor Devices, 2nd Edition, Wiley-Interscience, New York, 1981.

4. W. Shockley and W. T. Read, Jr., Phys. Rev. B, **87,** no. 5, 835-842(1952), R. N. Hall, Phys. Rev., **83**, 228(1951) and **87**, 387(1952).

5. J. Shiau, A. Fahrenbruch, and R. Bube, J. Appl. Phys., **59(8)**, (1986), 2879.

6. R. Ahrenkiel, J. Appl. Phys., **59(1)**, (1986), 181.

# REPORT DOCUMENTATION PAGE

*Form Approved*
*OMB NO. 0704-0188*



| 1. AGENCY USE ONLY (Leave blank) | 2. REPORT DATE | 3. REPORT TYPE AND DATES COVERED |
|---|---|---|
| | November 1998 | Final Report, 18 April 1995–31 May 1998 |

**4. TITLE AND SUBTITLE**
Advanced Processing of CdTe- and $CuIn_xGa_{1-x}Se_2$-Based Solar Cells: Final Report, 18 April 1995–31 May 1998

**5. FUNDING NUMBERS**
C: XAF-5-14142-09
TA: PV905001

**6. AUTHOR(S)**
D.L. Morel, C.S. Ferekides, R. Bhatt, A. Jayapalan, V. Komin, H. Lin, D. Marinskiy, S. Marinskaya, R. Narayanaswamy, U. Poosarla, R. Prabhakaran, H. Sankaranarayanan, B. Tetali, V. Viswanathan, and S. Zafar

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
Department of Electrical Engineering
University of South Florida
4202 East Fowler Ave.
Tampa, FL 33620

**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**
SR-520-25941

**11. SUPPLEMENTARY NOTES**
NREL Technical Monitor: B. von Roedern

**12a. DISTRIBUTION/AVAILABILITY STATEMENT**
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

**12b. DISTRIBUTION CODE**

**13. ABSTRACT** *(Maximum 200 words)*
This report summarizes work performed by the University of South Florida Department of Electrical Engineering under this subcontract. The cadmium telluride (CdTe) portion of this project deals with the development of high-efficiency thin-film CdTe solar cells using fabrication techniques that are suitable for manufacturing environments. The process being developed for semiconductor deposition is close-spaced sublimation (CSS), which has demonstrated high throughput and efficient material utilization. During Phase II, an all-CSS device fabricated on Libbey-Owens-Ford substrate exhibited a 14.3% efficiency. Alternative transparent conducting oxides (TCOs) and window materials being studied under this project include zinc oxide (ZnO) and zinc selenide (ZnSe). The best efficiency obtained for a ZnSe/CdTe device was 11.3%. This work also included fabricating CdTe solar cells heat-treated with $CdCl_2$ vapor instead of the typical methanol/$CdCl_2$ wet process, which has produced some encouraging results. The copper indium gallium diselenide (CIGS) portion of the project focused on developing a semiconductor that reliably and reproducibly produced high Jsc values. A key objective was achieved: the ability to optimize bulk and surface properties independently of each other. Researchers were able to boost Voc values above 500 mV on 40 $mA/m^2$ base materials and achieve efficiencies of 13%.

**14. SUBJECT TERMS**
photovoltaics ; solar cells ; cadmium telluride ; close-spaced sublimation ; low band-gap devices ; copper indium gallium diselenide

**15. NUMBER OF PAGES**
43

**16. PRICE CODE**

| 17. SECURITY CLASSIFICATION OF REPORT | 18. SECURITY CLASSIFICATION OF THIS PAGE | 19. SECURITY CLASSIFICATION OF ABSTRACT | 20. LIMITATION OF ABSTRACT |
|---|---|---|---|
| Unclassified | Unclassified | Unclassified | UL |