Test Vectors (cont.)

10) set threshold thresh=1
11) set threshold thresh=2
12) set threshold thresh=3
13) test mode on
14) test mode on mode_sparse=1
15) test mode on mode_trig=1
16) test mode on mode_sparse=1 mde_trig=1
17) verify operation of sync, reset, and trigger on different clk4 phases
18) verify tdc timing
19) verify multiple readout of same buffer
20) half speed readout
21) check fadc hold-off

Test Vectors

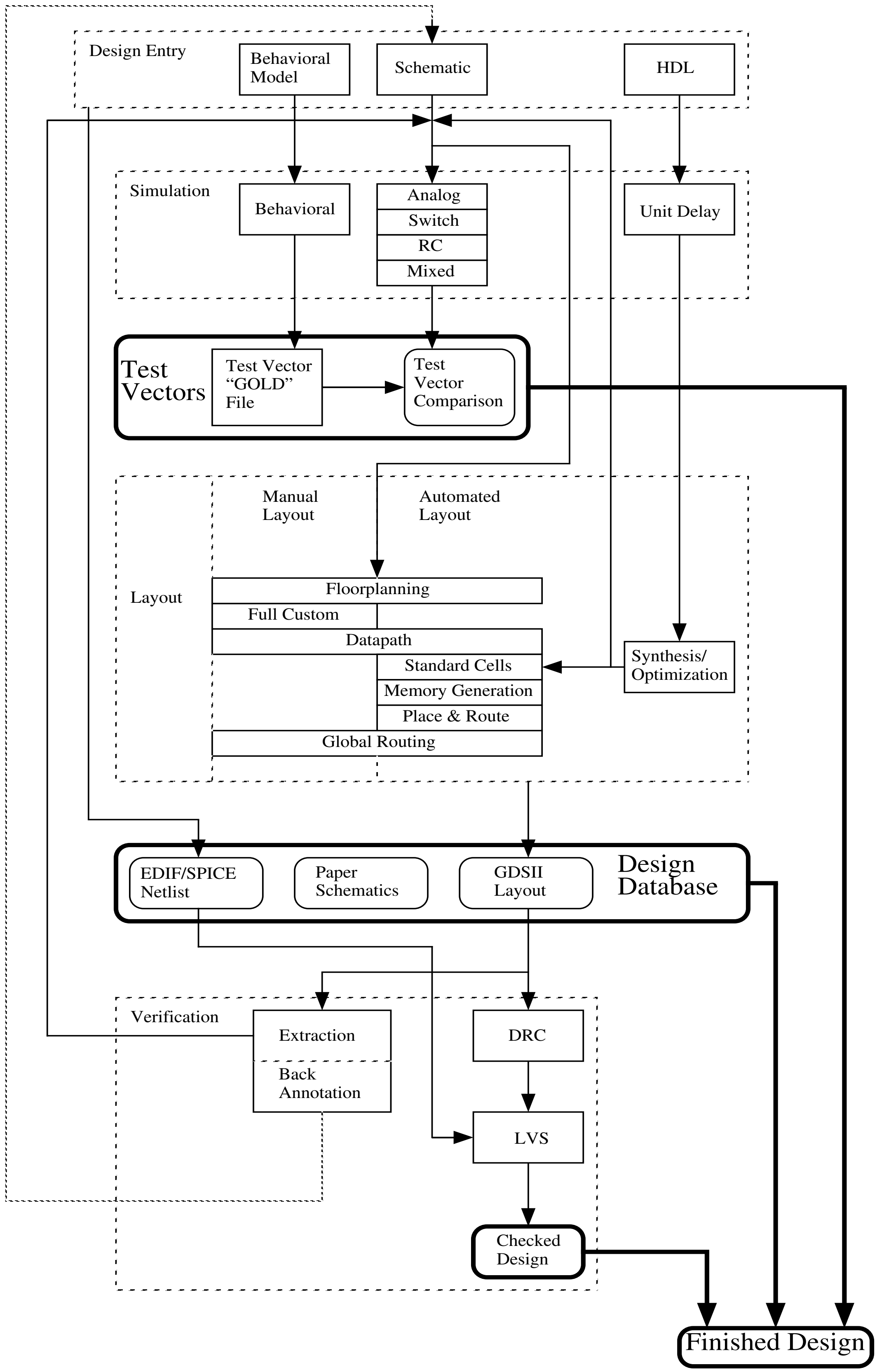
A complete test vector suite was developed for the Elefant Digitizer IC.

This suite was run on the pre-production model and accurately modeled the functionality of the IC

The test vector suite runs 21 sets of test vectors. These sets are summarized below:

1) standard readout
2) standard readout mode_sparse=1
3) standard readout mode_trig=1
4) standard readout mode_sparse=1 mode_trig=1
5) standard readout cycle fadc always
6) standard readout cycle fadc always mode_sparse=1
7) standard readout cycle fadc always mode_trig=1
8) standard readout cycle fadc always mode_sparse=1 mode_trig=1
9) set threshold thresh=0

Verification Procedure



Scott Dow

Actions Taken After The PDR (cont.)

5) COMPLETE CHIP, and “vicinity”: (cont.)

- In general, the chip should not show a destructive behavior or draw excessive current under any condition, such as the absence of a clock, power on, etc.

6) TESTING:

The committee perceived the need to rethink the testing of the IC. The production testing and detailed characterization seems to be in good hands at U of Montreal, although the team should think through and plan careful the burn-in and testing sequence. The functional testing, on the other hand, could be a major time sink and be critical for the successful development of the IC. It has to be planned ahead of time, test-boards and set-ups have to be build and a test program has to be developed. This requires manpower, resident at LBL, with thorough understanding of the design and the design tools. Given the fact that part of the present group will leave this project in the Fall, new team members should be added asap to make them familiar with the IC project.

Actions Taken After The PDR (cont.)

3) TDC:

- Check temperature and power supply sensitivity
- Investigate recovery time of the delay locked loop after a sync that is changing the phase of the sampling clock
- Verify that the absence of the clock does not damage the chip
- Investigate the condition of the TDC in the absence of a clock after a RESET

4) DRAM:

- Verify that the DRAM will survive operating at high temperature after is has received some radiation damage.

5) COMPLETE CHIP, and “vicinity”:

- The possibility of using complementary CMOS output buffers.
- On the control gate array, the run time control signals e.g. “trigger”, “clock”, etc. should also be complementary, even if the receiving end is single ended.

Actions Taken After The PDR

The Elefant Digitizer IC PDR was held on July 24, 1996.
The review committee suggested various actions.
This is a list of the changes due to the review committees suggestions.

1) ANALOG RECEIVERS:

- Perform Monte Carlo simulations to define bandwidth, accounting for the input characteristics of the FADC block
- Optimize gain-bandwidth-power trade-off.
- Check linearity at full 3 Volts output.
- Size of the analog receiver block (Layout)?
- ESD protection?

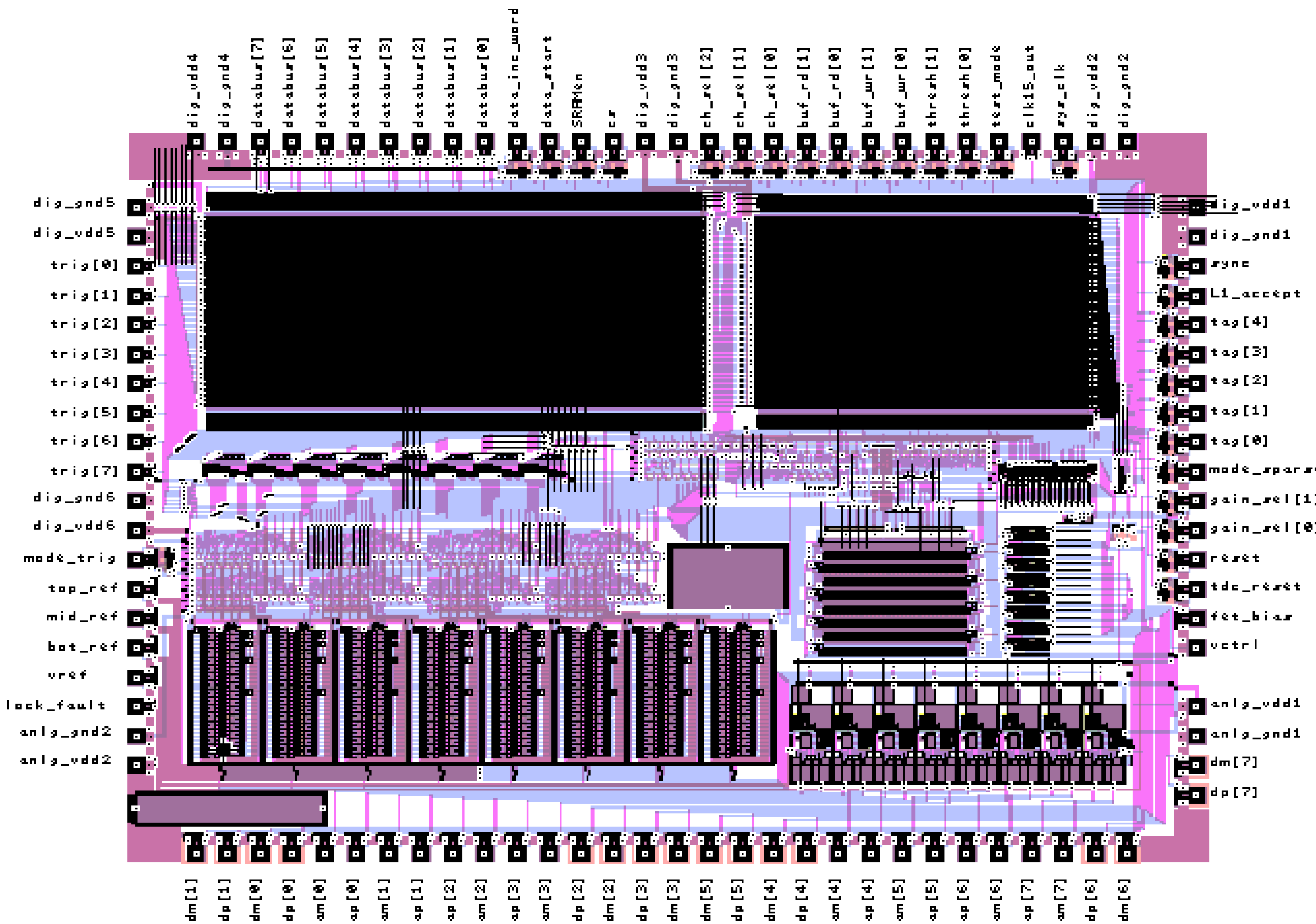
2) DIGITAL RECEIVERS:

- Check temperature sensitivity (time walk)
- Check power supply sensitivity
- Test for jitter (after fabrication)

Table 1: Elefant Digitizer IC Specifications

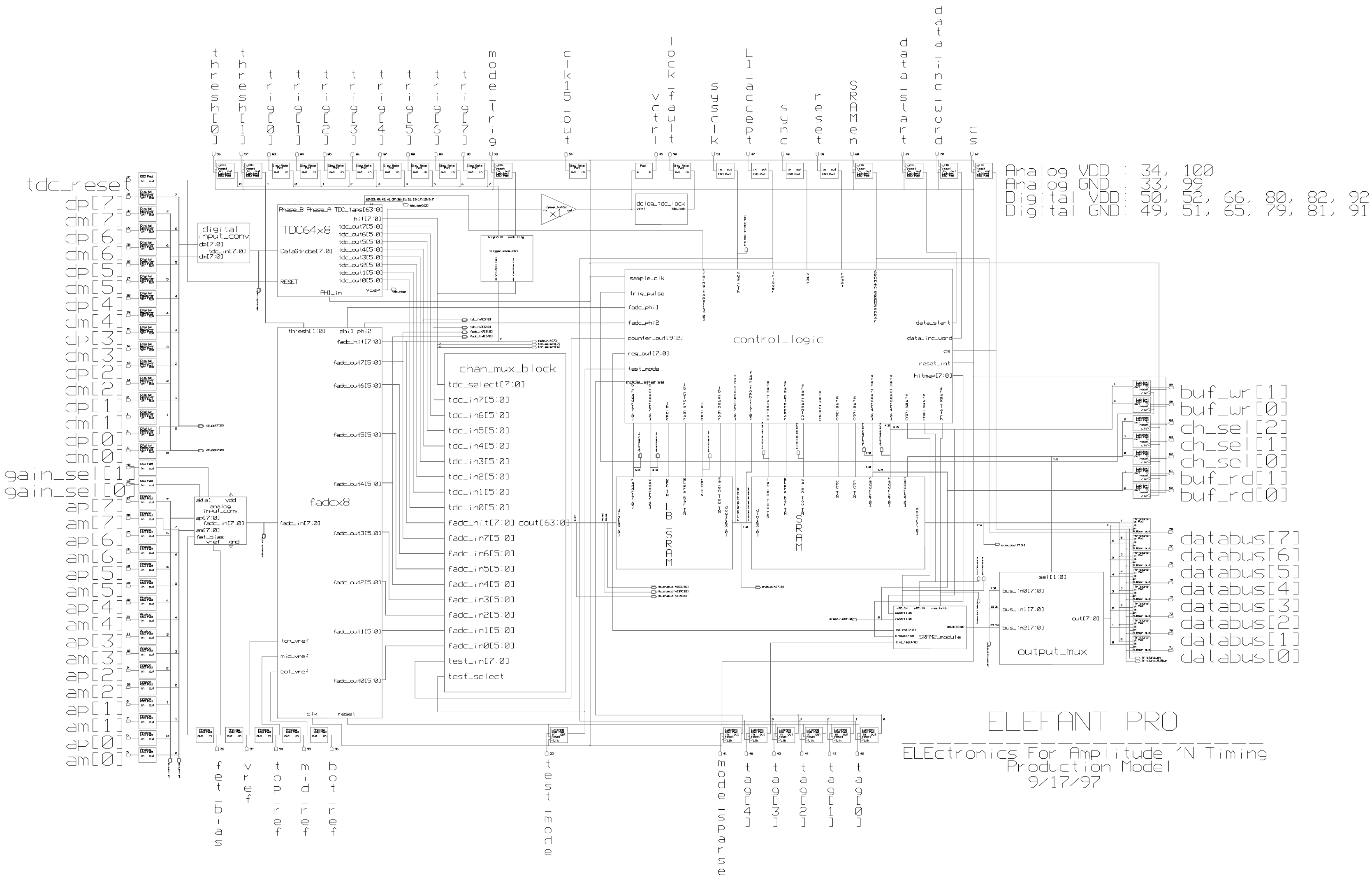
Parameter	Specification	Variation	Pre-Production Model	Production Model (Expected)
Power	< 500 mW	Less is better	420 mW	450 mW
Analog Vdd	+5 V	+/-0.2 V	5 V +/-0.2 V	5 V +/-0.2 V
Digital Vdd	+5 V	+/-0.2 V	5 V +/-0.2 V	5 V +/-0.2 V
Analog Receiver Frequency Response	5 MHz @ Gain of 10	-3 MHz/ +Any	> 20 MHz @ Gain of 10	> 20 MHz @ Gain of 10
Gain Settings	5, 10, 20, 40	Rough Settings	5, 9, 17, 29	5, 9, 17, 29
Digital Input	+/- 400 uA	up to +/- 1.6 mA	> +/- 200 uA	> +/- 200 uA
FADC Resolution	6 Bits	N/A	7 Bits	8 Bits
TDC Resolution	1.05 ns	1.07ns	1.05 ns	1.05 ns
TDC Jitter	< 0.1 ns	< 0.1 ns	< 0.1 ns	< 0.1 ns
L1 Buffer Length	12.9 us	12.9 us	12.9 us	12.9 us
# Of Event Buffers	4	4	4	4
Fast Control Protocol	Implement Portion	N/A	Implemented	Implemented

Elefant Digitizer IC Final Design Review

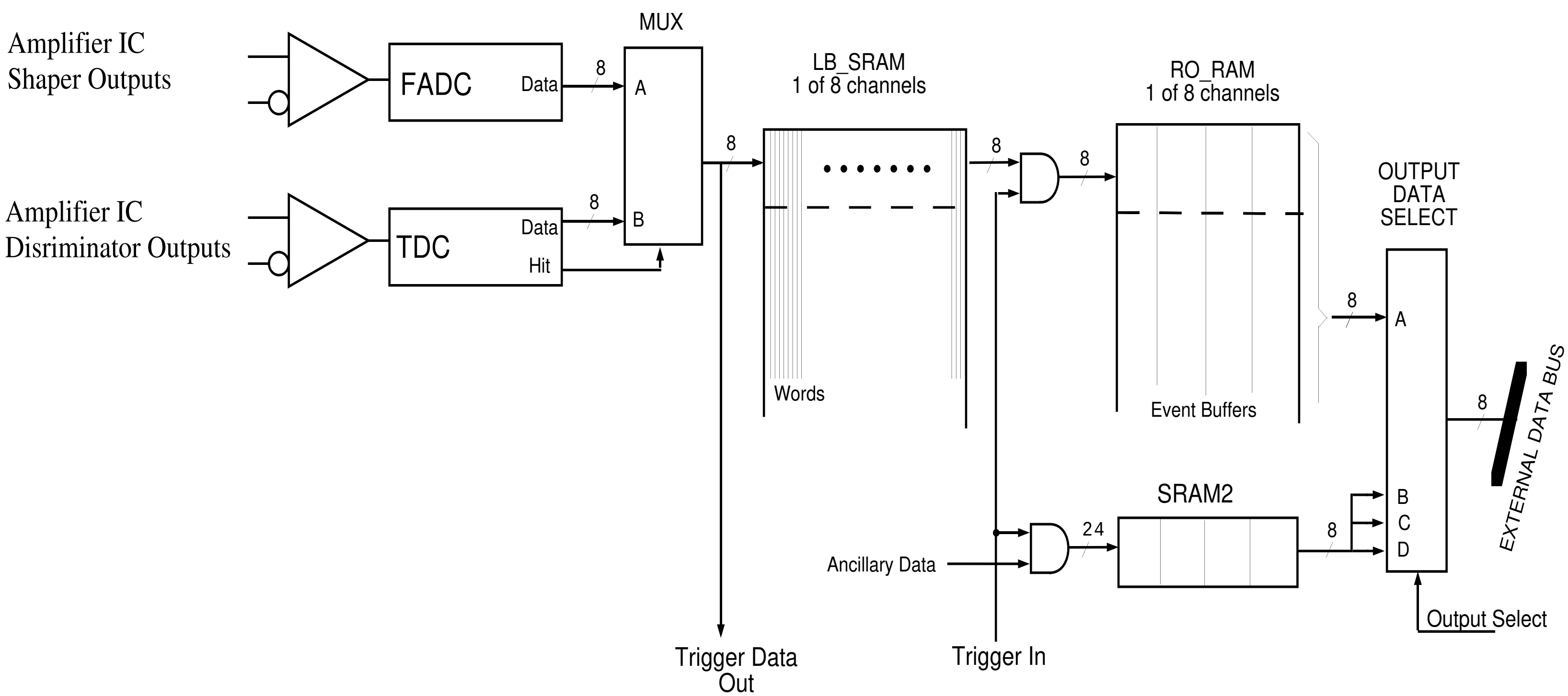


Elefant Digitizer IC Layout

Elefant Digitizer IC Final Design Review



Elefant Digitizer IC Top Level Schematic



Simplified Elefant Block Diagram

Overview Of The Elefant Digitizer IC

Specifications Review

From The PDR To The Prototype

Verification Procedures