The STAR Scaler Board, A 10 MHz 24-bit VME Memory Module

H.J.Crawford[1], F.S.Bieser[2], T.Stezelberger[2]
[1]University of California Space Sciences Laboratory
[2]Lawrence Berkeley National Laboratory

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Abstract

This note describes a 24 bit 10 MHz VME memory module, the STAR Scale Board, developed for use in investigations of polarized proton interactions and high energy nucleus-nucleus collisions. Operating as a histogramming memory, each of the 2^{24} cells has a 40-bit deep counter which is incremented by 1 count each time the 24 bit input pattern representing the cell address is observed in coincidence with the leading edge of a clock pulse. Each module is controlled by a resident XiLinx Field Programmable Gate Array (FPGA) programmed to respond to various control registers' contents at each clock edge. The STAR experiment uses 12 scaler boards to keep a continuous (deadtimeless) record of fast-detector and RHIC Accelerator-related correlations.

1 Introduction

One of the central problems in physics is to identify the origin of the spin carried by elementary particles. Experimental investigations typically employ polarized beams and targets in which specific quark (q) or gluon (g) moderated interactions are investigated to isolate the spin dependence. The Relativistic Heavy Ion Collider (RHIC) at the Brookhaven National Laboratory (BNL) allows investigation of colliding beams of polarized protons and of high energy nuclei.

RHIC typically runs with 120 bunches in each beam. The polarization of the protons is introduced by the source, the Alternating gradient Synchrotron (AGS), with a typical polarization of 40% spin up or spin down in any given bunch. To better understand systematic effects in measuring

spin dependent variables, some of the bunches are polarized with spin up, some with spin down, some are unpolarized and some are empty. Thus, at each interaction region, the pattern of the 120 bunches is complex, consisting of up-up, up-dn, up-none, dn-none, etc., each producing a different rate of quark-quark (qq), quark-gluon (qg), and gg interactions. The bunch patterns are stable for each fill of the collider, so that identifying the bunch numbers for each interaction allows the experiments to unfold the polarization content.

The Solenoidal Tracker at RHIC (STAR) experiment is a nearly hermetic detector consisting of both very fast detectors, that respond for each beam crossing, and very slow detectors, that integrate for a time that covers many beam crossings. The fast detectors cover 2π in ϕ and different regions of pseudorapidity, η. Because spin effects are often subtle it is necessary to compare large numbers of events for each of the polarization combinations. The scaler board described here was designed to correlate the fast detector data with the bunch number information to uncover the spin dependence.

Data from the fast detectors consists of discriminator outputs from individual phototubes (PMT) as well as logic levels produced by the STAR Level 0 trigger electronics [**?**]. These signals can be aligned to the same bunch through appropriate digital delay logic on the scaler board and presented to the latch simultaneously with a 7-bit pattern that encodes the bunch number. For the polarization studies, the 24 input bits of the scaler board typically consist of 17 detector-related bits and 7 bunch number bits. For unpolarized beam studies, the 24 input bits may consist of a mix of detector/logic bits and STAR status bits.

The scaler board has 2^{24} memory cells with each cell 5 bytes (40 bits) deep. Thus the board contains 5 bytes of memory for each 3 byte address. A 10 MHz clock corresponding to the bunch crossing frequency drives the boards at STAR. The contents of a memory cell are incremented by 1 each time the cell's address pattern is present at the leading edge of the clock pulse. Thus, the scaler boards allow us to analyze detector/accelerator correlations at a 10 MHz rate. The 40 bit depth allows us to operate the board continuously for up to 24 hours at 10 MHz. The board will operate with a lower frequency clock if longer integration times are desired.

The boards can be run as a master or a slave to allow ping-pong operation in which one board is being read-out while the other is collecting data. The input signals are not terminated on the board unless a termination resistor has been specifically requested for a given input channel, to allow daisy chin operation of the input signals. In typical ping-pong operation, the signals drop first in one unterminated board and end in a terminated

board. Switching between the master/slave states is accomplished within a single clock cycle, with the master board controlling the operation and sending the switch order to the slave via a front panel LEMO connection. Many functions can be performed within the board to eliminate or reduce time-consuming VME communication, such as clearing each memory cell or zero-suppressing output.

2 Technical description

The board consists of a central FPGA engine, two fast memories, front-panel input and VME backplane communication lines as indicated in the block diagram of Figure 1. In VME, the board occupies 0x10M (m$\rightarrow 10^6$) cells in memory space starting at its base address. Operation is controlled by a series of 32 bit registers shown in Table I whose addresses (in bytes) begin at the board base address. The contents of register 0 are fixed to return the pattern "deadf0c0" when read.

The board can be made active in either of two separate states using register 4 (Reg4). If you want the board to record data only when some other component is present, an external signal can be required in LEMO input 2 to make the board active by setting Reg4 = 2. Alternatively, when this register is set to 4 (Reg4 = 4) the board will "free run" as soon as the value of 4 is latched. When the register is set to 0, the board is not active and will not accumulate counts. The board must be set to active=0 (i.e., off) to be read. For test purposes, the user can write directly to the board when it is inactive (Reg4 = 0), adressing each cell directly.

The two memory banks can be read separately (Reg8 =0) or together (Reg8 =1). For debugging, separate reading is desrable, while in operation, we use combined reads. The lower 32 bits of the count in each channel is at address "board base address + 0x8M + 8*channel" while the upper 8 bits are at "board base address + 0x8M + 8*channel + 4".

The mode of operation, either "classic" (bit=0) or "new" mode (bit=1) is set by register c. The board counts bits as on if they are high on receipt of the leading edge of the clock pulse. Thus, if the input is a pulse it must be timed correctly. In "classic" mode, the input data is assumed to be pulses whose leading and trailing edges encompass the clock pulse. In "new" mode, the scaler board sets a one shot on receipt of the input pulse leading edge and clears this one shot 2.5ns after the leading edge of the clock pulse. This makes it easier to guarantee that and input signal is "high" when the clock

Address(HEX)	read/write	Register name
0	r	Board ID (HEX: deadf0c0)
4	rw	scaler active
8	rw	Memory bank BIt(0): (0=A, 1=B); Bit(1)=1 A+B (reading)
c	rw	bit0=0→ classic mode (bitmask) bit0=1 → new mode (bitmask)
10	rw	event counter LSB
14	rw	event counter MSB
20	w	Bit(0)=1 indicates automatic memory clear
24	r	Bit(0)=1 indicates board is busy clearing memory
30	w	Bit(0)=1 starts zero suppression Bit(1)=1 resumes zero suppression
38	r	Bit(0)=1 indicates board busy doing zero supression
3c	r	number of events in zero suppression buffer
100-15c	rw	Delay registers
200-25c	rw	Vernier delay registers
300-35c	r	positive phase offset meter
400-45c	r	negative phase offset meter
10000-11ffc	r	zero suppression buffer

Table 1: Registers

leading edge occurs. The Regc [1] is a bit mask so that each of the 24 input bits can be treated as "classic" or "new" separately.

A count of the total number of clock cycles the board has integrated while in an active state is kept in Reg10 (lower 4 bytes) and Reg14 (upper 4 bytes). A check of the sum of all channel populations should equal this clock sum.

Reading and writing each channel in the board using VME commands can be quite time consuming, although it is possible to do so for all data channels. For this reason the board has both an automatic clear command, initiated by setting Reg20=1, and a zero suppression readout mode, initi-

[1] registers are identified by their HEX address offset

Bit	Function
0	active master gated with RUN STOP ON
1	active slave (gated with RUN STOP ON
2	force active master
3	frce active slave

Table 2: Scaler active register settings

ated by setting Reg30=1. Register 24 is set by the FPGA when the board is busy clearing, and register 38 is set when the board is busy doing the zero suppression. The FPGA will set Reg34=1 when zero suppression is complete. When being read with zero-suppression on, the FPGA looks at each channel and copies those having non-0 counts into an intermediate buffer which holds 128 channels worth of information (1024 bytes). In this mode, the lower 4 bytes are at "board base address + 0x8M + channel*8", with the upper byte at "board base address + 0x8M+channel*8+4". The channel is held in the upper 3 bytes of the second read cycle, that is, starting at "board base address + 0x8M + channel*8 + 5". This buffer will be automatically replenished after each 128 channels are read until all non-zero channels are read. When all non-zero channels have been read, the FPGA sets register 34 to a value of 1. The number of events in the zero-suppression buffer can be read from register 3c.

It is often the case that the 24 input bits arrive from different sources at different times, when in fact they represent an "event" and all should be considered "simultaneous". The scaler board thus has two types of delays for each input bit, a 4-bit coarse and a 3-bit fine delay. The units of the coarse delay are clock intervals, and the units of the fine delay are internal clock intervals, which are the clock interval divided by 8. At RHIC, the clock is $\sim$ 10 MHz, so the clock interval is $\sim 100ns$. Thus the fine delay is in units of $\sim 12.5ns$ steps. To determine the correct delays for each of the input signals, the board has phase-offset meters for each bit for both the leading (positive) and trailing (negative) edges. The values in registers 0x300 - 0x35c record the internal clock value when the positive-going edge is detected, while registers 0x400-0x45c record the internal clock value when the negative-going edge is detected. Thus, to determine the correct delay setting for each signal, these registers can be read for a number of events and their mean value determined. This operation assumes that the relative bit timing is stable. Determining the coarse delay is accomplished by cycling

LEMO(from top)	Function
1(J5)	interconnection master/slave
2(J7)	"RUN-STOP" input on master

Table 3: Front panel LEMO connectors

Jumper	Function
S1 A28-A31	Board base address
S1 A24	jumper in → Master: jumper out → Slave
J4	inter board communication OUT → Master : IN → Slave
J6	RUN STOP ON IN → Master : OUT → Slave

Table 4: Board jumper settings

through a set of coarse delays until the desired coincidence is achieved.

We next describe histogram operation in a ping-pong mode. First the boards are set up to operate as a pair by connecting their 2nd LEMO inputs together (see Table 3) and by setting the jumper (see Table 4) on one board to be the master and the other to be the slave. Next the boards memories are cleared by first setting the board to be inactive (Reg4=0) and then setting Reg20=1. The board will hold register 24 high until the memory is clear. The master-board can then be made active using Reg4, setting it equal to 2 to run synchronously with an external signal in LEMO 1, or setting it to 4 to run independently. The slave-board is left in the inactive state until the master is ready to be read out. Writing a 0 to the active register of the master causes the slave to begin operating on the next clock tick in the same mode that was set for the master, ie, gated with the external signal or free running. Since the master is now inactive, it is safe to begin the read cycle for the master.

There are 4 LEDs on the front of the board that are used to give visual indication of the board status. These are defined in Table 5.

3 Conclusion

The STAR experiment now has 12 of these scaler boards taking data at RHIC. They have been used successfully to measure vertical polarization

LED(from top)	Function
1	Board active
2	Memory bank selected off→ Memory A; on→ Memory B
3	VME access in progress
4	not defined

Table 5: Front Panel LEDs

components, to verify operation of the spin rotators, and to normalize all of the STAR Heavy Ion data for AuAu and dAu collisions.

References

[1] Bieser et al