Simulation of a New Back Junction Approach for Reducing Charge Collection in 200 GHz SiGe HBTs

Guofu Niu, *Senior Member, IEEE*, Hua Yang, Muthu Varadharajaperumal, *Student Member, IEEE*, Yun Shi, John D. Cressler, *Fellow, IEEE*, Ramkumar Krithivasan, Paul W. Marshall, *Senior Member, IEEE*, and Robert Reed, *Senior Member, IEEE*

***Abstract*—We present a new back junction approach for reducing SEU-induced charge collection in SiGe HBTS, and demonstrate its effectiveness in a state-of-the-art 200 GHz SiGe HBT using full 3-D device simulation. An additional n^+ layer is used below the p-type isolation layer to form a back junction. The back junction limits potential funneling to within the p-type layer, which effectively limits the total amount of drift charge collection that is now shared by the collector-to-substrate junction and the back junction. The back junction also cuts off the diffusion charge coming from the substrate, further limiting charge collection by the HBT collector. A thinner p-type "substrate" layer and a better contact to the added n^+ layer are shown to help reduce charge collection by the HBT collector, the sensitive node.**

***Index Terms*—Charge collection, charge sharing, SEU, SiGe HBT.**

I. Introduction

HIGH-SPEED SiGe HBTS have demonstrated excellent hardness to both total dose and displacement radiation without intentional hardening, making them very attractive for space applications. Single-event upset, however, is a potential concern, because of the existence of the n^+ buried layer to p-substrate junction [1]–[3]. This SEU problem is particularly worse for heavy ions that penetrate deeply into the substrate, as it is typically lightly doped (p-type). The light doping leads to a wider depletion layer and a large amount of charge collection after a heavy ion strike. A natural approach to SEU hardening is to fabricate the SiGe HBT on an SOI substrate [4]–[7], thus eliminating the n^+ buried layer to p-substrate collecting junction. A practical problem with the SOI SiGe HBT is compatibility with SOI CMOS processes, which, however, often use a very thin silicon film, making collector resistance high. Recently, the buried oxide was etched away to form a low resistance n^+ collector in the p-substrate underneath the buried oxide in a SiGe technology [8]. This SOI approach, however, makes the SiGe HBT on SOI equivalent to a bulk SiGe HBT from a charge collection standpoint.

Manuscript received July 1, 2005; revised October 1, 2005. This work was supported in part by NASA-GSFC under the NASA Electronic Parts and Packaging Program and in part by DTRA under the Radiation Hardened Microelectronics Program.

G. Niu, H. Yang, M. Varadharajaperumal, and Y. Shi are with the Electrical and Computer Engineering Department, Auburn University, Auburn, AL 36849 USA (e-mail: niuguof@auburn.edu).

J. D. Cressler and R. Krithivasan are with the Georgia Institute of Technology, Atlanta GA 30332 USA.

P. W. Marshall is with NASA-GSFC, Greenbelt, MD 20771 USA.

R. Reed is with Vanderbilt University, Vanderbilt, TN 37203 USA.

Digital Object Identifier 10.1109/TNS.2005.860744

We propose in this work a new back junction approach to reducing charge collection in SiGe HBTS, and demonstrate its effectiveness in 200 GHz SiGe HBTS using full 3-D device simulation. The basic idea is to add another n^+ layer below the p-type "substrate," to form a *back pn* junction, as detailed below. The underlying physics is similar to that in the back junction SiGe channel p-MOSFET proposed previously, where the back junction is used to reduce the vertical electric field for enhanced hole confinement in the SiGe quantum well [9], [10]. This back junction structure is designed to reduce charge collection in several ways. First, the total amount of charge that can be collected is now limited by the thickness of the p-layer. Second, the charge deposited in the p-layer will be collected by both the normal n^+ buried layer to p-layer junction and the added back junction, further reducing charge collection by the sensitive transistor collector node. In addition, the path of diffusion from substrate toward the collector in the conventional SiGe HBT is cut off by the back junction. Using 3-D device simulation, we examine here the impact of the back junction design and p-layer thickness on charge collection, and perform a quantitative comparison at the 200 GHz SiGe technology node of charge collection between a back junction SiGe HBT and a conventional SiGe HBT.

II. Device Structures

To verify the effectiveness of the proposed back junction approach, we have simulated the charge collection characteristics in a state-of-the-art 200 GHz bulk SiGe HBT, with and without the proposed back junction. The SiGe HBT features a 200 GHz peak cutoff frequency (f_T). Figs. 1 and 2 show the 2-D cross-sections of the conventional SiGe HBT and the back junction SiGe HBT, respectively, which are obtained from cuts made through the center of the 3-D structures. This 200 GHz SiGe HBT features a raised extrinsic base to reduce base resistance and collector-base capacitance [11]. The conventional SiGe HBT has a lightly doped p-type substrate, an n^+ buried layer for reducing collector resistance, a selectively implanted collector, epitaxial intrinsic and raised extrinsic base, a polysilicon emitter, and shallow and deep trench isolation.

Figs. 3 and 4 show the 3-D structures of the conventional SiGe HBT and the back junction SiGe HBT. The active emitter area is $0.12 \times 0.6\ \mu\mathrm{m}^2$, which is only a small portion of the total silicon area enclosed by the deep trench ($1.5 \times 4.34\ \mu\mathrm{m}^2$). The cut-planes used to generate the 2-D cross-sections are also shown. For obtaining high speed, the conventional SiGe HBTS

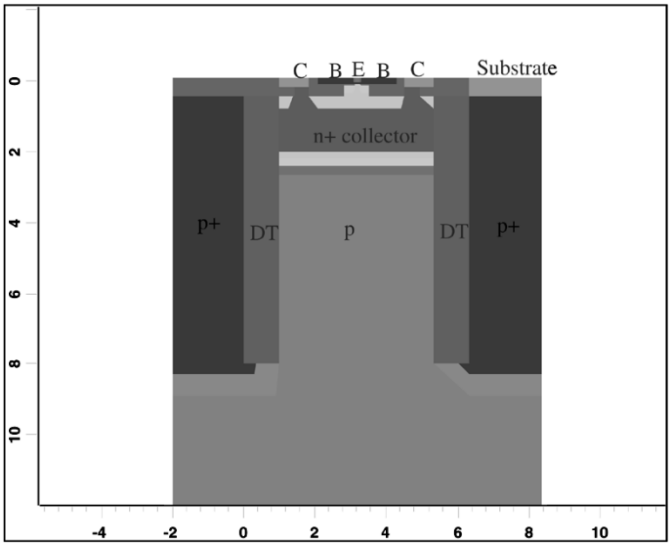

Fig. 1. The 2-D cross-section of the conventional SiGe HBT.

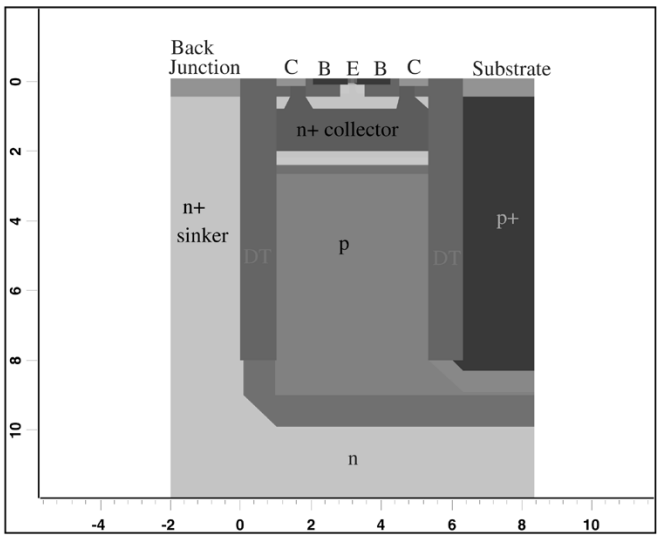

Fig. 2. The 2-D cross-section of the back junction SiGe HBT.

in this technology have double base contacts and double collector contacts. The contact to the n^+ layer of the back junction is made from the top on the left side, and the contact to the p-layer of the back junction is made from the top on the right side. The emitter and base contacts are simulated as a plane with zero thickness, and are not visible in Figs. 3 and 4. As discussed below, contact to the n^+ layer of the back junction can also be made surrounding the deep trench isolation ring of the active device. This, together with a wider n^+ sinker, help to enhance charge collection by the back junction. As a result, the collector charge collection is further reduced.

III. 3-D Simulation

The 3-D SiGe HBT structures were constructed based on device layout, process information, and careful calibration of $I-V$, f_T-I_C, and the $M-1-V_{\mathrm{CB}}$ to measured data. The electrical characteristics were simulated using DAVINCI [12].

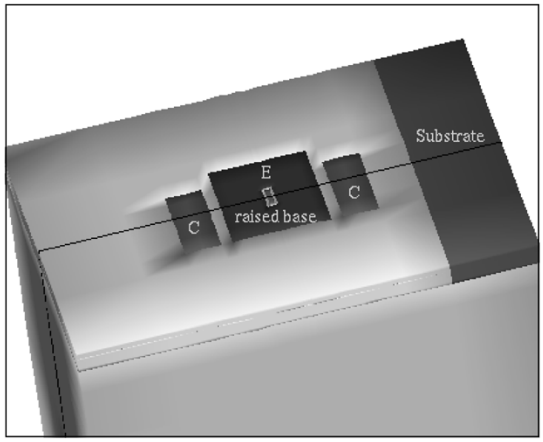

Fig. 3. The 3-D structure of the conventional SiGe HBT.

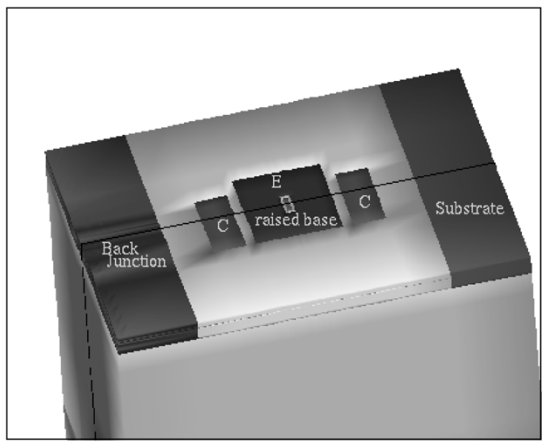

Fig. 4. The 3-D structure of the back junction SiGe HBT.

To mimic worst case deep ion strikes that traverse the entire device, we have assumed charge deposition throughout the whole simulated structure. Initial simulations were performed on a 50 μm thick structure and a 100 μm thick structure, and no difference was observed in charge collection, confirming that 50 μm is sufficient to realistically mimic the real substrate. We chose a 0.1 pC/μm charge deposition, which is equivalent to an LET of 10 MeV-cm^2/mg for its relevance to orbital applications. The charge track was generated over a period of 10 psec using a Gaussian waveform. The $1/e$ characteristic time scale is 2 psec and the $1/e$ characteristic radius is 0.2 μm. These choices are somewhat arbitrary, but expected to produce reasonable charge collection results. A smaller radius, e.g., 10 nm, does not affect charge collection result, so long as it is much smaller than the distance between the deep trench isolation edges, which is at least 1 μm. The charge deposition can be viewed as instant as the time scale involved is on the order of pico seconds, and much smaller than the drift charge collection time, which is on the order of nano seconds. The peak of the gaussian occurs at 4 psec. The simulator does not at present support the variation of these constants with LET, or non-Gaussian waveforms of charge track generation.

An ion strike through the center of the emitter is assumed and fine gridding is placed around the charge track. The physics simulated includes concentration dependent Shockley-Read-Hall

recombination, Auger recombination, the Philips unified mobility model, velocity saturation, and bandgap narrowing. Unless specified, the p-type "substrate" contact was biased at $V_{\rm EE} = -5$ V, and all other terminals were grounded. This represents a worst bias situation in a SiGe HBT digital circuit. Each transient simulation was performed until the current decayed to zero. The simulated transient waveforms are constantly monitored during simulation, and the simulation was terminated when charge collection was judged to be complete. As we will show below, charge collection is significantly faster in the back junction SiGe HBT than it is in the conventional SiGe HBT.

IV. Results and Discussion

A. Charge Collection Characteristics

We first consider the back junction SiGe HBT shown in Fig. 4. For a relatively straightforward comparison with the conventional SiGe HBT, we first consider a 8 μm thick p-layer so that the deep trench thickness can be kept the same as in the conventional HBT. The supporting substrate below the p-layer is assumed to be $\rm n^+$ for simplicity in simulation. For reducing collector charge collection, this $\rm n^+$ layer only needs to be a few microns thick, similar to the $\rm n^+$ collector buried layer, and can sit on top of a p-type supporting substrate. The doping of this layer does not need to be as heavy as the $\rm n^+$ collector. Charge collection can occur through the additional junction for deep strikes. This, however, does not affect the transistor collector charge collection, despite increased charge collector by the p-layer due to additional charge collection through the back junction $\rm n^+$ layer to p-type supporting substrate junction. A shunt between the back junction p-layer and the p-type supporting substrate can occur upon ion strike, depending on the biasing difference, similar to the shunt between the p-type SiGe base and the p-substrate in a conventional SiGe HBT. The effect of such shunt on charge collection, however, is negligibly small in general, as shown by the small amount of base and emitter charge collections. Furthermore, any additional electrons brought closer to the surface due to this shunt effect would meet the $\rm n^+$ back junction first before reaching the transistor collector. We thus do not expect significant effect of this shunt on the transistor collector charge collection. A 2.0 μm wide $\rm n^+$ sinker was used on the left side of the deep trench to make contact with the $\rm n^+$ layer of the back junction. We will refer to this terminal as the "back junction" contact here-after. We will continue to refer to the p-layer as the "substrate" for consistency with notation used in the conventional SiGe HBT. As we will show below, a thinner p-layer is desired for both reduced charge collection and easier device fabrication.

Fig. 5 shows the transient terminal currents as a function of time and Fig. 6 shows the charges collected by individual terminals as a function of time. Observe that charge collection is complete within 2 ns, and is mostly due to drift. Most of hole charge collection occurs through the p-type substrate terminal. The base collects a small amount of hole charge, and the emitter collects a small amount of electron charge. The collector collects 0.8 pC electron charge, while the back junction collects 0.4 pC electron charge.

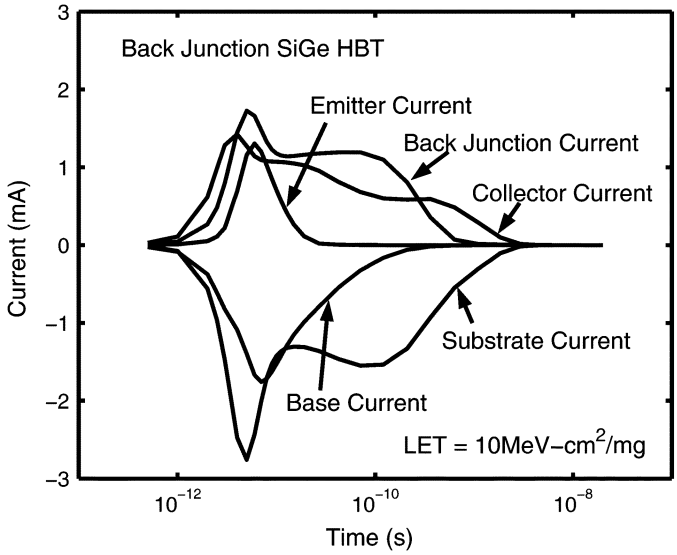

Fig. 5. Transient terminal currents as a function of time for the back junction SiGe HBT. The p-layer of the back junction is 8 μm thick.

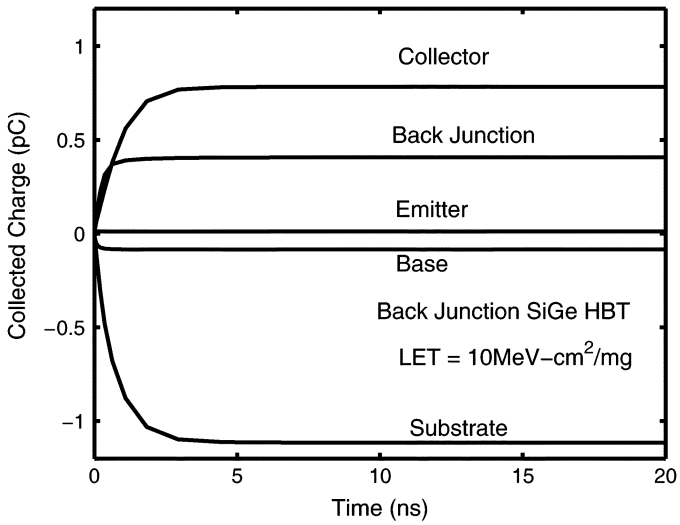

Fig. 6. Charge collected by the terminals as a function of time for the back junction SiGe HBT. The p-layer of the back junction is 8 μm thick.

B. Back Junction N^+ Sinker Design

The simulation details show that the resistance of the $\rm n^+$ sinker for contacting the $\rm n^+$ layer of the back junction is important for the overall charge collection through the back junction. To explore this, we increased the $\rm n^+$ sinker width to 4 μm and placed the $\rm n^+$ sinker on the left, top, and right of the deep trench isolation ring, effectively reducing the impedance to the back junction. The terminal charge collection results are summarized in Table I, together with the results for the conventional device. The amount of collector charge collection decreases from 0.78 to 0.52 pC with the 4 μm $\rm n^+$ sinker placed around the perimeter of the deep trench ring surrounding the active area of the HBT.

Fig. 7 compares the collector charge collection of the back junction SiGe HBT and the conventional SiGe HBT. Both back junction $\rm n^+$ sinker designs are shown. With the 4 μm $\rm n^+$ sinker back junction design, the amount of collector charge collection is 0.52 pC, a significant $(3\times)$ reduction compared to 1.56 pC

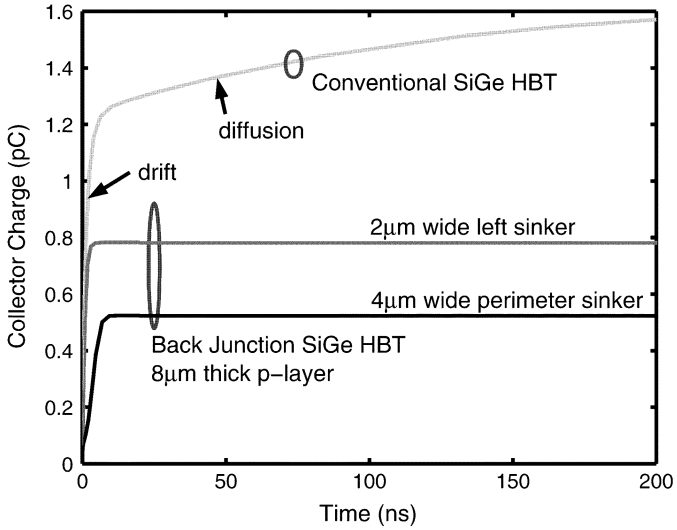

Fig. 7. Comparison of collector charge collection in the back junction SiGe HBT and the conventional SiGe HBT. The p-layer of the back junction is 8 μm thick.

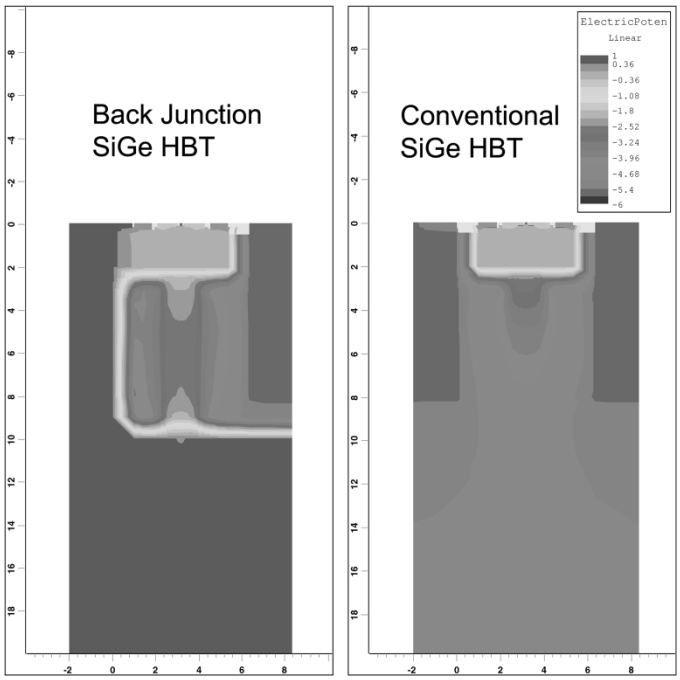

Fig. 8. Comparison of potential contours at 4 psec in the back junction SiGe HBT and the conventional SiGe HBT. The p-layer of the back junction is 8 μm thick.

in the conventional device. In addition, note that in the conventional SiGe HBT charge collection takes much longer because of the much slower diffusive charge collection within the lightly doped substrate. In the back junction SiGe HBT, however, charge collection primarily occurs within the p-layer. The potential funneling in the collector n^+ to p-substrate junction can interact with the potential funneling in the back junction, thus significantly speeding up the overall charge collection. This should produce an obvious advantage for SEU. A comparison of the potential contours at 4 psec between the back junction and conventional SiGe HBTS is given in Fig. 8. This time instant corresponds to the peak of the Gaussian waveform for electron-hole pair generation.

TABLE I
TERMINAL CHARGES COLLECTED IN pC FOR DIFFERENT n^+ SINKER TO BACK JUNCTION DESIGNS AND CONVENTIONAL SiGe HBT

	Back Junction		Conventional
	2.0μm sinker left	4.0 μm sinker perimeter	
back junction	0.41 pC	0.48 pC	N/A
collector	0.78 pC	0.52 pC	1.56 pC
substrate	1.12 pC	0.93 pC	1.53 pC
emitter	0.011 pC	0.009 pC	0.041 pC
base	0.085 pC	0.085 pC	0.078 pC

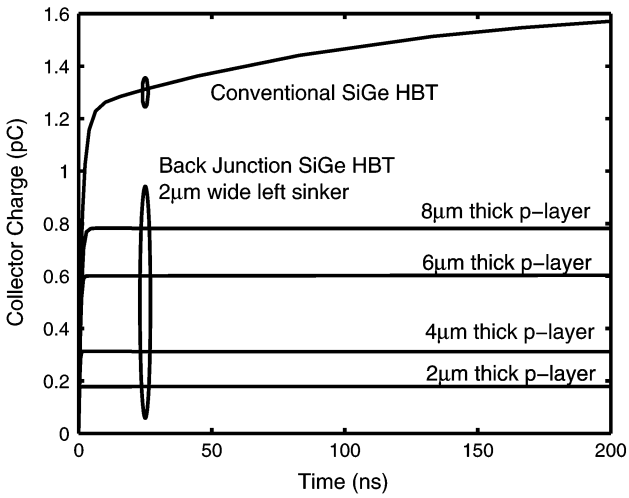

Fig. 9. Comparison of collector charge collection for different p-layer thickness. The n^+ sinker for contacting the back junction is 2 μm and placed on the left side.

C. p-Layer Thickness Issues

The p-layer thickness limits the total amount of drift charge collection, and thus a thinner p-layer should lead to a further reduction of collector charge collection. Fig. 9 shows the simulated collector charge collection characteristics for different p-layer thicknesses. The n^+ sinker for contacting the back junction is 2 μm and placed on the left side for all of the p-layer thicknesses. By decreasing the p-layer thickness to 4 μm, we can further decrease the collector charge collection to 0.3 pC, a significant improvement over the 1.6 pC charge collection in the conventional device. For the 8 and 6 μm p-layers, the collector charge is approximately equal to the charge deposited in the p-layer. This cannot be generalized though, as part of the charge can also be collected by the back junction, as shown in Table I. A better contact to the back junction was shown earlier to favor more charge collection by the back junction. Due to the reverse biases on the back junction and the collector-substrate junction, much of the 4 μm p-layer is depleted, resulting a high impedance for holes to exit the p-layer. This, we believe, is responsible for the less efficient charge collection (0.3 pC collected versus 0.4 pC deposited). As the p-layer thickness decreases to below 4 μm, the p-layer doping must be increased and the reverse bias V_{EE} reduced to -3 V to prevent punchthrough. The higher doping helps reducing the impedance seen by holes. A thinner p-substrate layer is clearly much easier to fabricate if high-temperature epitaxy is used to form this layer.

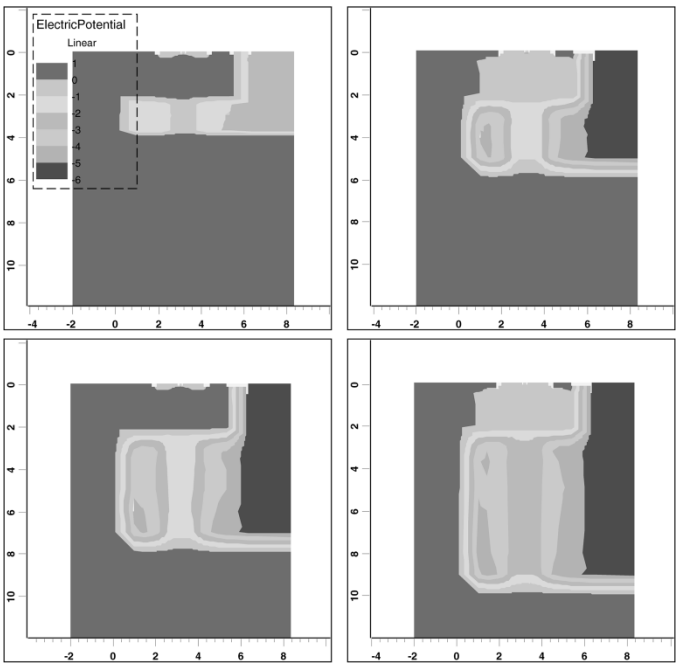

Fig. 10. Comparison of potential contours at 4 psec in the back junction SiGe HBT with 2 μm, 4 μm, 6 μm, 8 μm p-layer thickness.

Fig. 10 shows the simulated potential contours at 4 psec in the back junction SiGe HBT for various p-layer thicknesses. The results clearly show that potential funneling is well confined in the p-layer, and the length of the potential funneling region is proportional to the p-layer thickness, as theoretically expected. Consequently, a thinner p-layer leads to less collector charge collection, as was shown in Fig. 9.

D. Device Fabrication Considerations

A straightforward way to fabricate the proposed structure is to start with a p-type supporting substrate, create a relatively heavily doped n-layer by diffusion for formation of the back junction, grow several microns p-type layer, and then create the n^+ collector buried layer, again by diffusion. The rest of the processing would be the same as for a conventional SiGe HBT. Alternatively, one might form the back junction n-layer by a high energy n-type implantation. If necessary, another p-type implant could be used to increase the doping level of the p-type "substrate" layer. The n^+ collector buried layer can then be made the same way as for a conventional SiGe HBT. Only the sinker formation for contacting the back junction and p-layer requires additional masks. The area penalty is not as significant as it may appear, because these added contacts are not essential to device operation, and can be placed in the same manner as the substrate contact. That is, these contacts are shared by all devices on the same chip, and only need to be placed with a reasonable density to ensure good global contact. Any unused spaces between devices can also be used to further improve contact to the p-layer and the back junction.

V. Summary

We have presented a new back junction approach for reducing charge collection in SiGe HBTS, and simulated its effectiveness in a 200 GHz SiGe process technology. The back junction limits potential funneling to within the p-layer, thus placing an upper limit to the total amount of drift charge collection. The path of diffusion charge collection in the conventional HBT is also cut off by the back junction. A wide n^+ sinker around the deep trench perimeter helps by enhancing back junction charge collection, hence further reducing charge collection at the sensitive collector node. A thinner p-type "substrate" layer also effectively decreases collector charge collection.

Acknowledgment

The authors would like to thank R. Ladbury, K. Label, L. Cohn, and A. Joseph for their contributions and support of this work.

References

[1] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Junction Bipolar Transistors*. Norwood, MA: Artech House, 2003.

[2] G. Niu, J. D. Cressler, M. Shoga, K. Jobe, P. Chu, and D. L. Harame, "Simulation of SEE-Induced Charge Collection in UHV/CVD SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2682–2689, Dec. 2000.

[3] M. Varadharajaperumal, G. Niu, R. Krithivasan, J. D. Cressler, R. A. Reed, P. W. Marshall, G. Vizkelethy, P. E. Dodd, and A. J. Joseph, "3-D simulation of heavy-ion induced charge collection in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2191–2198, Dec. 2003.

[4] M. Varadharajaperumal, G. Niu, J. D. Cressler, R. A. Reed, and P. W. Marshall, "Three-dimensional simulation of heavy-ion induced charge collection in SiGe HBT's on SOI," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3298–3303, Dec. 2004.

[5] F. Sato, T. Hashimoto, H. Tezuka, M. Soda, T. Suzaki, T. Tatsumi, and T. Tashiro, "A 60-GHz f_T self-aligned selectively grown SiGe-base (SSSB) bipolar transistor with trench isolation fabricated on SOI substrate and its application to 20-Gb/s optical transmitter IC's," *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1332–1338, Jul. 1999.

[6] J. Cai, M. Kumar, M. Steigerwalt, H. Ho, K. Schonenberg, K. Stein, H. Chen, K. Jenkins, Q. Ouyang, P. Oldiges, and T. Ning, "Vertical SiGe-base bipolar transistors on a CMOS-compatible SOI substrate," in *Proc. IEEE BCTM*, 2003, pp. 215–218.

[7] M. Racanelli and P. Kempf, "SiGe BiCMOS technology for communication products," in *Proc. IEEE Custom Int. Circ. Conf.*, 2003, pp. 331–334.

[8] H. Rueker, B. Heinemann, R. Barth, D. Bolze, J. Drews, O. Fursenko, T. Grabolla, U. Haak, W. Hoeppner, D. Knoll, S. Marschmeyer, N. Mohapatra, H. H. Richter, P. Schley, D. Schmidt, B. Tillack, G. Weidner, D. Wolansky, H. Wulf, and Y. Yamamoto, "Integration of high-performance SiGe:C HBT's with thin-film SOI CMOS," *IEDM Tech. Dig.*, pp. 239–242, Dec. 2004.

[9] G. Niu, G. Ruan, T. Tang, and R. Kwor, "Back junction SiGe PMOS—a new structure with an improved effective channel mobility," in *Proc. Eur. Solid-State Dev. Res. Conf.*, Erlangan, Germany, Sep. 1994, pp. 151–154.

[10] G. Niu, G. Ruan, and T. A. Tang, "Inversion charge modeling of SiGe PMOS and approaches to increasing the hole density in the SiGe channel," *Solid-State Electron.*, vol. 38, no. 2, pp. 323–329, Feb. 1995.

[11] B. A. Orner, Q. Z. Liu, B. Rainey, A. Stricker, P. Geiss, P. Gray, M. Zierak, M. Gordon, D. Collins, V. Ramachandran, W. Hodge, C. Willets, A. Joseph, J. Dunn, J. Rieh, S. Jeng, E. Eld, G. Freeman, and D. Ahlgren, "0.13 μm BiCMOS technology featuring a 200/280 ghz $(f_t f_{\max})$ SiGe HBT," in *Proc. IEEE BCTM*, 2003, pp. 203–206.

[12] *Synopsys*, 2004. DAVINCI, 3D Device Simulation Software.