1st NASA/ESA Conference on Adaptive Hardware and Systems

June 15 - 18, 2006

Istanbul, Turkey

The *First NASA/ESA Conference on Adaptive Hardware and Systems* (AHS-2006) will be held June 15-18, 2006, in Istanbul, Turkey, immediately following and co-located with the IEEE Conference on Communications (June 11-15, 2006). The purpose of AHS-2006 is to bring together leading researchers from the adaptive hardware and systems community to exchange experiences and share new ideas in the field. The conference expands the topics addressed by the precursor annual series of NASA/DoD Conference on Evolvable Hardware held between 1999 and 2005.

Adaptation reflects the capability of a system to maintain or improve its performance in the context of internal or external changes, such as uncertainties and variations during fabrication, faults and degradations, modifications in the operational environment, incidental or intentional interference, different users and preferences, modifications of standards and requirements, trade-offs between performance and resources, etc.

Adaptation at hardware levels increases the system capabilities beyond what is possible with software-only solutions, and a large number of adaptation features employing both analog and digital adjustments are becoming increasingly present in the most elementary system components. Algorithms, techniques, and their implementation in hardware are developed over a diverse variety of applications, such as adaptive communications (adapting to changing environment and interferences), reconfigurable systems on a chip and portable wireless devices (adapting to power limitations) or survivable spacecraft (adapting to extreme environments and mission unknowns). This meeting will provide a forum for discussion on the generic techniques of adaptive hardware and systems, with a focus on communications and space applications, with view to its expansion and exploitation in other applications such as consumer, medical, defense and security, etc.

Registration & check-in information

The meeting will begin at 9:00 A.M. on Thursday, June 15, at the Besiktas Campus of the Bahcesehir University (Osmanpasa Mektebi Sokak, No:4-6 Besiktas, Istanbul, Turkey) in the Fazil Say Conference Room, located on the first floor of the Besiktas Campus main building. On Thursday June 15, the meeting will start with a series of five tutorials presented by experts in the domain of adaptive hardware and systems. The meeting will continue on Friday, Saturday, and Sunday with the presentations of papers and posters. The tutorials are free for the attendees of AHS-2006 and the IEEE International Conference on Communications (ICC 2006), but registration on the conference registration web site is required for tutorials as well as for the conference. On-site check-in will begin on Thursday, June 15 from 8:00 A.M. to 12:00 A.M., and Friday, June 16 at 8:00 A.M. at the meeting site. At this time, you will be given your meeting badge and receipt for the registration fee, plus a packet of meeting materials.

All participants are expected to pay the conference registration fee of EURO 450 before May 26 (EURO 550 after May 26) which covers the cost of the conference, plus break service, a reception and a banquet. The student registration fee is EURO 200. Please go on our registration web site and follow the instructions. Note that no purchase orders, foreign checks or foreign currency can be accepted. Credit Cards (VISA, MASTER and AMERICAN EXPRESS) and US dollar traveler's checks are accepted. For our planning purposes, pre-registration with payment of fees is appreciated. Questions regarding registration should be addressed to:

Nizamettin Aydin n.aydin@bahcesehir.edu.tr Tel: +90 212 669 6523 Ext:1233 Fax: + 90 212 669 4398

Conference Registration Web Site: http://www.ahs2006.org/

Accommodation

You can book your hotel on the conference registration web site through Dekon Congress & Tourism organisation. The hotels listed on our registration web site are conveniently located near the conference venue. Also a limited block of rooms has been set aside at the Bahcesehir University Guest House at a rate of EURO 45 for single room and EURO 35 for double occupancy plus tax. The number of rooms at the Guest House are limited and we encourage you to book your room as soon as possible using the conference registration web site.

Transportation

The Besiktas Campus of the Bahcesehir University area is served by two major airports: Istanbul Ataturk International Airport (http://www.ataturkairport.com/) (30 kms from the Besiktas campus on the Europian side of the city – 45 minutes drive, however, based on the time of the day, it may take slightly longer or shorter – Taxi approximately 20 EURO), and Sabiha Gökçen International Airport (http://www.sgairport.com/) (30 kms from the Besiktas campus on the Anatolian side of the city. – 45 minutes drive, however, based on the time of the day, it may take slightly longer or shorter – Taxi approximately 20 EURO). From Istanbul Ataturk International Airport, the Swissotel and Sozbir Royal Residence Hotel have a fee on-call shuttle service which provides door-to-door from 7 a.m. until 10 p.m. Please contact the hotel for further information. There are several shuttles which provide door-to-door, on-call van service from the airport to selected Hotels. Taxis and rental cars are also readily available at the airports. For further information, call or email the conference reservation organisation:

Dekon Congress & Tourism: dekon@dekon.com.tr Tel: +90 212 347 6300 Fax: +90 212 347 6363

For further information plase check the conference web site or contact

Conference Web Site: http://ehw.jpl.nasa.gov/events/ahs2006

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Thursday, June 15, 2006

8:00 - 9:00 **Registration (Tutorials are free to AHS attendees and IEEE Conference on Communications registered attendees, but registration is required due to limited seating.)**

Track 1

Location: Besiktas Campus of the Bahcesehir Universy

9:00 - 10:20 **Tutorial 1: Evolvable Hardware**

Tetsuya Higuchi, National Institute of Advanced Industrial Science and Technology (AIST), Japan

Abstract

This tutorial introduces the basic concept of evolvable hardware and gives the overview of industrial applications of evolvable hardware,including prothetic hand, data compression, semiconductor applications.

10:20 - 10:30 *Break*

10:30 - 11:50 **Tutorial 2: High Performance Reconfigurable Architectures for SoC era**

Tughrul Arslan, The University of Edinburgh, UK

Abstract

The tutorial will provide a review of embedded reconfigurable architectures targeting applications with strict power/speed/area constraints. Example applications will include image processing, telecomunication, aerospace and speech coding. The tutorial will provide design flow for integrating such architectures within modern system on chip design methodologies. In addition, the tutorial will provide an overview of how such architectures can be reconfigured for applications where on-line real-time adaptation is required for conditions such as change in channel environments in the case of telecommunication or environmental varaition in aerospace.

11:50 - 12:00 *Break*

12:00 - 1:20 **Tutorial 3: Reconfigurable Computing by Reconfigurable Logic**

Jim Torresen, University of Oslo, Norway

Abstract

Swapping of software processes at run-time has been common for a long time. However, it has not yet been very common having hardware being dynamic and adaptable at run-time. With the recent progress in reconfigurable technology (typically FPGAs), systems applying run-time reconfiguration has started to appear. This tutorial will give an introduction to run-time reconfiguration of hardware and present what is state-of-the-art today.

Track 2

Location: Besiktas Campus of the Bahcesehir Universy

10:30 - 11:50 **Tutorial 4: Evolvable Hardware in the View of Theoretical Computer Science**

Lukas Sekanina, Brno University of Technology, Czech Republic

Abstract

In this tutorial, the area of evolutionary digital circuit design and evolvable hardware will be briefly introduced. This mainly experimental work will be generalized and the concept of evolvable computational machines will be proposed. Evolvable computational machines will be defined formally and their properties will be investigated. We will ask whether the evolved machines are computational mechanisms and whether they can be simulated on a standard Turing machine. This tutorial presents a non-traditional view on these topics in which the evolved systems are considered as computational machines and investigated from the point of view of theoretical computer science.

11:50 - 12:00 *Break*

12:00 - 1:20 **Tutorial 5: Hardware Accelerators for Evolving Building Block Modules for Artificial Brains**

Hugo de Garis, Wuhan University, China

Abstract

Evolution of neural net circuits on inexpensive FPGA hardware (~$10,000) offers speed-ups by a factor of about 50 relative to using an ordinary PC. This makes the evolution of large numbers of modules (~10,000) each with its own function, doable in a reasonable time. Software to connect up the modules to build artificial brains is needed and will be in the future specified according to the designs of human brain architects. The artificial-brain in the PC could then control the many behaviors of a robot using 2-way radio antenna, a gripper, a CCD camera on the robot. This may be an affordable alternative to the using PC clusters with thousands of nodes (e.g. the Blue Brain project, CCortex project etc).

1:30 - 2:30 *Lunch (on your own)*

2:15 - 6:00

Visiting Tour to Dolmbahce Palace

Free tour to the Dolmbahce Palace, a magnificent 19th centery palace with 14 tons of pure gold used for its interior decoration, a rich collection of Bohemian crystal in addition to its famous Harem section. Transportation will be provided from Conference Venue (departure at 2:15pm) to the Dolmbahce palace and from Dolmbhace palace (departure 6pm) to Welcome Diner.

Visit our Tours and Excursions on your own are also available on the Web Site: **http://www.ahs2006.org/tours.php**

7:00 - 9:00 **Welcome Diner**

Come and enjoy Classical Turkish music and cuisine in an authentic Turkish venue (free for registered attendees of AHS-2006). After diner, transportation will be provided from the Restaurant to Taksim area (Hilton, Swissotel, Tashik, Macka hotels).

Location: Sehzade Mehmed Sofrasi

Friday, June 16, 2006

8:00 - 9:00	**Registration**
9:00 - 9:30	**Adrian Stoica,** Jet Propulsion Laboratory, USA **and Tughrul Arslan,** Edinburgh University, UK *Welcome and Organizationals Remarks*
9:30 - 10:15	**Martin Suess,** European Space Agency, Netherlands *Technologies for Adaptive Systems for Space (Invited keynote address)*
10:15 - 11:00	**Pekka Karp,** Future and Emerging Technologies, European Commission, Belgium *Foundational ICT research in the new European Framework Programme (Invited keynote address)*
11:00 - 11:10	*Break*
11:10 - 11:55	**Tetsuya Higuchi,** National Institute of Advanced Industrial Science and Technology, Japan *Evolvable Hardware for Industrial Applications (Invited keynote address)*
11:55 - 1:00	*Lunch*
	Session 10: ESPACENET (Invited Papers) *Chair:* **Adrian Stoica,** Jet Propulsion Laboratory, USA
1:00 - 1:25	**T. Arslan, N. Haridas, E. Yang, A. T. Erdogan, N. Barton, A. J. Walton, J. S. Thompson,** University of Edinburgh, UK**, A. Stoica,** JPL, USA**, T. Vladimirova,** University of Surrey, UK**, K. D. McDonald-Maier,** University of Essex, UK **and W. G. J. Howells,** University of Kent, UK *ESPACENET: A Framework of Evolvable and Reconfigurable Sensor Networks for Aerospace-Based Monitoring and Diagnostics*
1:25 - 1:50	**Tanya Vladimirova, Xiaofeng Wu, Kawsu Sidibeh, David Barnhart, and Abdul-Halim Jallad,** University of Surrey, UK *Enabling Technologies for Distributed Picosatellite Missions in LEO*
1:50 - 2:15	**Andrew B. T. Hopkins and Klaus D. McDonald-Maier,** University of Essex, UK *A Generic On-Chip Debugger for Wireless Sensor Networks*
2:15 - 2:40	**Gareth Howells, Evangelos Papoutsis,** University of Kent, UK**, and Klaus McDonald-Maier,** University of Essex, UK *Novel Techniques for Ensuring Secure Communications for Distributed Low Power Devices*
2:40 - 2:50	*Break*
	Session 4: Adaptive Signal Processing *Chair:* **TBD**
2:50 - 3:15	**Joseph Kolibal,** University of Southern Mississippi, USA **and Daniel Howard,** University of Limerick, Ireland *The Novel Stochastic Bernstein Method of Functional Approximation*
3:15 - 3:40	**Horia-Nicolai Teodorescu,** Technical University of Iasi, Romania *An Adaptive Heuristic Filter for Acceleration Measurements in Planetary Atmospheres*
3:40 - 4:05	**Gorn Tepvorachai and Chris Papachristou,** Case Western Reserve University, USA *Self-Configurable Neural Network Processor for FIR Filter Applications*
	Session 2: Adaptive Antennas *Chair:* **TBD**
4:05 - 4:30	**Nakul Haridas, Ahmet T. Erdogan, Tughrul Arslan, and Mark Begbie,** University of Edinburgh, UK *Adaptive Micro-antenna on Silicon Substrate*
4:30 - 4:55	**Gabriella Kókai,** Friedrich-Alexander University of Erlangen-Nürnberg**,** Germany**, Tonia Christ, and Hans Holm Frhauf,** Fraunhofer Institute for Integrated Circuits, Germany *Using Hardware-Based Particle Swarm Method for Dynamic Optimization of Adaptive Array Antennas*
4:55 - 5:20	**Ozgur Tamer and Ahmet Ozkurt,** Dokuz Eylul University, Turkey *Systolic Array Based Adaptive Beamformer Modelling in SystemC Environment*
5:20 - 5:30	*Break*
	Session 1: Adaptive Analog Circuits *Chair:* **Didier Keymeulen,** Jet Propulsion Laboratory, USA
5:30 - 5:55	**Varun Aggarwal, Meng Mao, and Una-May O'Reilly,** MIT, USA *A Self-Tuning Analog Proportional-Integral-Derivative (PID) Controller*
5:55 - 6:20	**Mustafa Keskin,** Qualcomm Inc., USA *A Background Mismatch Calibration for Capacitive Digital-to-Analog Converters*
6:20 - 6:45	**Martin Trefzer, Jörg Langeheine, Karlheinz Meier, and Johannes Schemmel,** Ruprecht-Karls-University of Heidelberg, Germany *A Modular Framework for the Evolution of Circuits on Configurable Transistor Array Architectures*
6:45 - 7:10	**Aleksandar Tasić,** University of Heidelberg, Germany *Adaptive Multifunctional Circuits and Systems for Future Generations of Wireless Communications*
7:10 - 7:30	*Break*
7:30 - 9:30	**Short Papers/Posters and Reception Cocktail** *Chair:* **Nizamettin Aydin**, Bahçeşehir University, Turkey *Location:* Bosphore Terrasse on the roof of the conference venue Each author will give a 5 minutes overview of his poster.

Saturday, June 17, 2006

8:00 - 8:30	**Registration**
8:30 - 9:15	**Tanya Vladimirova,** Surrey Space Centre, UK *Addressing the Challenges of Microelectronics Design for Space Applications.* *(Invited keynote address)*
9:15 - 9:25	*Break*
	Session 12: Applications to Sensing and Image Processing *Chair:* **H.N. Teodorescu**, University of Iasi, Romania
9:25 – 9:50	**N. İsmailoğlu, O. Benderli, S. Yeşil, R. Sever, B. Okcan, O. Şengül, and Ruşen Öktem,** TÜBİTAK BİLTEN, Turkey *GEZGİN & GEZGİN-2: Adaptive Real-Time Image Processing Subsystems for Earth Observing Small Satellites*
9:50 – 10:15	**Muhammed R. Pac, Aydan M. Erkmen, and Ismet Erkmen,** Middle East Technical University, Turkey *Towards Fluent Sensor Networks: A Scalable and Robust Self-Deployment Approach*
10:15 – 10:40	**Kyrre Glette, Jim Torresen,** University of Oslo, Norway**, Moritoshi Yasunaga, and Yoshiki Yamaguchi,** University of Tsukuba, Japan *On-Chip Evolution Using a Soft Processor Core Applied to Image Recognition*
10:40 – 11:05	**Mustafa Parlak and Ilker Hamzaoglu,** Sabanci University, Turkey *An Efficient Hardware Architecture for H.264 Adaptive Deblocking Filter Algorithm*
11:05 – 11:30	**Syamsiah Mashohor, Jonathan R. Evans, and Ahmet T. Erdogan,** University of Edinburgh, UK *Automatic Hybrid Genetic Algorithm Based Printed Circuit Board Inspection*
11:30 – 11:40	*Break*
	Session 3: Adaptive Optical Systems *Chair:* **H.J. Kadim,** Liverpool JM University, UK
11:40 – 12:00	**Hirokazu Nosato, Masahiro Murakawa, and Tetsuya Higuchi,** AIST, Japan *Automatic Alignment of Multiple Optical Components Using Genetic Algorithm*
12:00 – 12:20	**Onur Keskin, Peter Hampton, Rodolphe Conan, Colin Bradley, Aaron Hilton, and Celia Blain,** University of Victoria, Canada *Woofer-Tweeter Adaptive Optics Test Bench*
12:20 – 12:40	**Omar Paranaiba Vilela Neto, Leone Pereira Masiero, Marco Aurélio C. Pacheco, and Carlos R. Hall Barbosa,** PUC-RIO, Brazil *Evolvable Hardware Applied to Nanotechnology*
12:40 - 2:00	*Lunch*
2:00 - 2:45	**Radu Andrei,** Plura Tech, US *Single-Chip Adaptive Storage Technology.* *(Invited keynote address)*
	Session 14: Biometrics and Content Based Security Systems (Invited Papers) *Chair:* **A. Bouridane**, Queens' University Belfast, UK
2:45 - 3:10	**Khalil Zebbiche, Lahouari Ghouti, Fouad Khelifi, Ahmed Bouridane,** Queen's University of Belfast, UK *Protecting Fingerprint Data Using Watermarking*
3:10 - 3:35	**Amr T. Abdel-Hamid,** West Virginia University, Institute of Technology, USA**, Sofiène Tahar,** Concordia University, Canada **and El Mostapha Aboulhamid,** Montreal University, Canada *Finite State Machine IP Watermarking: A Tutorial*
3:35 - 4:00	**Walid R. Boukabou, Lahouari Ghouti, and Ahmed Bouridane,** Queen's University of Belfast, UK *Face Recognition Using a Gabor Filter Bank Approach*
4:00 - 4:25	**Lin Yuan, Gang Qu, Lahouari Ghouti, and Ahmed Bouridane,** University of Maryland, College Park, USA *VLSI Design IP Protection: Solutions, New Challenges, and Opportunities*
4:25 - 4:50	**Osama Al-Khaleel, Chris Papachristou, Frank Wolff,** Case Western Reserve University, USA **and Kiamal Pekmestzi,** National Technical University of Athens, Greece *A Large Scale Adaptable Multiplier for Cryptographic Applications*
4:50 - 5:00	*Break*
	Session 13: Applications in Communications *Chair*: **TBD**
5:00 - 5:20	**Balal Ahmad, Ahmet T. Erdogan, and Sami Khawam,** University of Edinburgh, UK *Architecture of a Dynamically Reconfigurable NoC for Adaptive Reconfigurable MPSoC*
5:20 - 5:40	**Jichuan Zhao and Ahmet T. Erdogan,** University of Edinburgh, UK *A Novel Self-Organizing Hybrid Network Protocol for Wireless Sensor Networks*
5:40 - 6:00	**Ediz Cetin,** University of Westminster, UK**, Suleyman S. Demirsoy,** Altera, UK**, Izzet Kale, and Richard C. S. Morling,** University of Westminster, UK *A Low-Complexity Self-Calibrating Adaptive Quadrature Receiver*
6:00 - 6:20	**Heiko Hinkelmann, Peter Zipf, and Manfred Glesner,** Darmstadt University of Technology, Germany *Design Concepts for a Dynamically Reconfigurable Wireless Sensor Node*
6:20 - 6:40	**Gökmen Altay, Osman N. Ucan, Nejla Altay, and Şenay Yalçın,** Bahçeşehir University, Turkey *On the Trellis Structures of Geometric Augmented Product Codes*
7:30 - 10:00	**Banquet:** *Bosphore Cruise (boarding at the conference venue)*

Sunday, June 18, 2006

8:30 - 9:15	**Bulent Celebi,** CEO AirTies, Turkey *Shift of product design to silicon suppliers is resulting in unhappy end users (Invited keynote address)*
9:20 - 9:30	*Break*
	Session 8: Reconfigurable Systems (Invited Papers) *Chair:* **Tughrul Arslan,** University of Edinburgh, UK
9:30 - 9:55	**Martin Margala,** University of Rochester, USA *Adaptable Architectures for Signal Processing Applications*
9:55 - 10:20	**Wim Vanderbauwhede,** University of Glasgow, UK *The Gannet Service-Based SoC: A Service-Level Reconfigurable Architecture*
10:20 -10:45	**Tanya Vladimirova and Xiaofeng Wu,** University of Glasgow, UK *On-Board Partial Run-Time Reconfiguration for Pico-Satellite Constellations*
10:45 - 11:10	**Sajid Baloch, Tughrul Arslan,** University of Edinburgh, UK **and Adrian Stoica,** JPL, USA *Embedded Reconfigurable Array Fabrics for Efficient Implementation of Image Compression Techniques*
	Session 6: Evolution of Digital Systems *Chairs:* **Li-Shan Kang and Sanyou Zeng,** Wuhan University , China
11:10 - 11:35	**Lukas Sekanina,** Brno University of Technology, Czech Republic *Evolutionary Design of Digital Circuits: Where Are Current Limits?*
11:35 - 11:45	*Break*
11:45 - 12:10	**Jorge Peña,** University of Lugano, Switzerland**, Andres Upegui, and Eduardo Sanchez,** EPFL, Switzerland *Particle Swarm Optimization with Discrete Recombination: An Online Optimizer for Evolvable Hardware*
12:10 - 12:35	**Emanuele Stomeo, Tatiana Kalganova, and Cyrille Lambert,** Brunel University, UK *Generalized Disjunction Decomposition for the Evolution of Programmable Logic Array Structures*
12:35 - 1:00	**Wing On Fung, Tughrul Arslan, and Sami Khawam,** University of Edinburgh, UK *Genetic Algorithm Based Engine for Domain-Specific Reconfigurable Arrays*
1:00 – 1:55	*Lunch*
1:55 - 2:20	**Evangelos F. Stefatos, Tughrul Arslan,** University of Edinburgh, UK**, Didier Keymeulen, and Ian Ferguson,** JPL, USA *Towards the Integration of Drive Control Loop Electronics of the JPL/Boeing Gyroscope within an Autonomous Robust Custom-Reconfigurable Platform*
2:20 – 2:45	**Rui Liu** (1)**, Sang-you Zeng** (1)**, Lixin Ding,** Wuhan University, China**, Lishan Kang, Hui Li, Yuping Chen, Yong Liu, and Yueping Han,** (1) China University of Geosciences, China *An Efficient Multi-objective Evolutionary Algorithm for Combinational Circuit Design*
	Session 7: Reconfigurable Devices and Architecture *Chair:* **Ahmet Ergodan,** University of Edinburgh, UK
2:45 - 3:10	**Mohsin A. Syed,** EADS Astrium GmbH, Germany **and Eberhard Schueler,** PACT XPP Technologies AG, Germany *Reconfigurable Parallel Computing Architecture for On-Board Data Processing*
3:10 - 3:35	**H. Fatih Ugurdag, Yahya Sahin, Onur Baskirt, Soner Dedeoglu, Sezer G. Ugurdag, and Yasar S. Kocak,** Bahcesehir University, Turkey *Population-Based FPGA Solution to Mastermind Game*
3:35 - 4:00	**Andy M. Tyrrell and Hong Sun,** University of York, UK *A Honeycomb Development Architecture for Robust Fault-Tolerant Design*
4:00 - 4:25	**H. J. Kadim,** Liverpool JM University, UK *State-Space Based Analytical Modelling for Real-Time Fault Recovery and Self-Repair with Applications to Biosensors*
4:25 - 4:35	*Break*
	Session 5: Morphogenetic and Cellular Adaptive Hardware *Chair:* **Andy Tyrrell,** University of York, UK
4:35 - 5:00	**Gianluca Tempesti, Pierre-André Mudry, and Guillaume Zufferey,** EPFL, Switzerland *Hardware/Software Coevolution of Genome Programs and Cellular Processors*
5:00 - 5:25	**Gunnar Tufte,** The Norwegian University of Science and Technology, Norway *Gene Regulation Mechanisms Introduced in the Evaluation Criteria for a Hardware Cellular Development System*
5:25 - 5:50	**Justin Lee and Joaquin Sitte,** Queensland University of Technology, Australia *Gate-Level Morphogenetic Evolvable Hardware for Scalability and Adaptation on FPGAs*
5:50 – 6:15	**Andres Upegui and Eduardo Sanchez,** EPFL, Switzerland *Evolving Hardware with Self-Reconfigurable Connectivity in Xilinx FPGAs*
6:15 - 6:30	**Concluding Remarks, Plans for the future**

7:30–9:30 PM	Friday, June 16, 2006

Short Papers/Posters Presentation

Chair: **Nizamettin Aydin,** Bahçeşehir University, Turkey
Each author will give a 5 minutes overview of his poster.

07:30 PM **Adrian Stoica, Ricardo S. Zebulum, Didier Keymeulen, Rajeshuni Ramesham,** JPL, USA**, Joseph Neff,** SPAWAR, USA**, and Srinivas Katkoori,** University of South Florida, USA
Temperature-Adaptive Circuits on Reconfigurable Analog Arrays

07:35 PM **Mustafa Keskin and Nurcan Keskin,** Qualcomm Inc., USA
A Tuning Technique for Switched-Capacitor Circuits

07:40 PM **Nizamettin Aydin,** Bahcesehir University, Turkey **and Tughrul Arslan,** University of Edinburgh, UK
Power Driven Reconfigurable Complex Continuous Wavelet Transform Processor

07:45 PM **Remzi Arslanalp and Abdullah T. Tola,** Pamukkale University, Turkey
A New State Space Representation Method for Adaptive Log Domain Systems

07:50 PM **Shengmin Ge and Hao Cheng,** Harbin Institute of Technology, China
A Comparative Design of Satellite Attitude Control System with Reaction Wheel

07:55 PM **Selcuk Okdem and Dervis Karaboga,** Erciyes University, Turkey
Routing in Wireless Sensor Networks Using Ant Colony Optimization

08:00 PM **Ioannis Nousias and Tughrul Arslan,** University of Edinburgh, UK
Wormhole Routing with Virtual Channels Using Adaptive Rate Control for Network-on-Chip (NoC)

08:05 PM **Nasri Sulaiman and Ahmet T. Erdogan,** University of Edinburgh, UK
A Multi-objective Genetic Algorithm for On-Chip Real-Time Adaptation of a Multi-carrier Based Telecommunications Receiver

08:10 PM **Steffen Toscher, Thomas Reinemann, and Roland Kasper,** University of Magdeburg, Germany
An Adaptive FPGA-Based Mechatronic Control System Supporting Partial Reconfiguration of Controller Functionalities

08:15 PM **Xue-song Yan, Wei Wei, Rui Liu, San-you Zeng, and Li-shan Kang,** China University of Geosciences, China
Designing Electronic Circuits by Means of Gene Expression Programming

08:20 PM **Sajid Baloch, Tughrul Arslan,** University of Edinburgh, UK **and Adrian Stoica,** JPL, USA
An Efficient Technique for Preventing Single Event Disruptions in Synchronous and Reconfigurable Architectures

08:25 PM **Didier Keymeulen, Ricardo Zebulum, Ramesham Rajeshuni, Adrian Stoica,** JPL, USA**, Srinivas Katkoori,** University of South Florida, USA**, Sharon Graves, Frank Novak, and Charles Antill,** NASA LaRC, USA
Self-Adaptive System Based on Field Programmable Gate Array for Extreme Temperature Electronics

08:30 PM **Robert Ross and Richard Hall,** La Trobe University, Australia
A FPGA Simulation Using Asexual Genetic Algorithms for Integrated Self-Repair

08:35 PM **Stefanos Skoulaxinos,** Heriot-Watt University, UK
SW-HW Co-design and Fault Tolerant Implementation for the LRID Wireless Communication System

08:40 PM **H. J. Kadim,** Liverpool JM University, UK
Analytical Modelling of Power Attenuation under Parameter Fluctuations with Applications to Self-Test and Repair

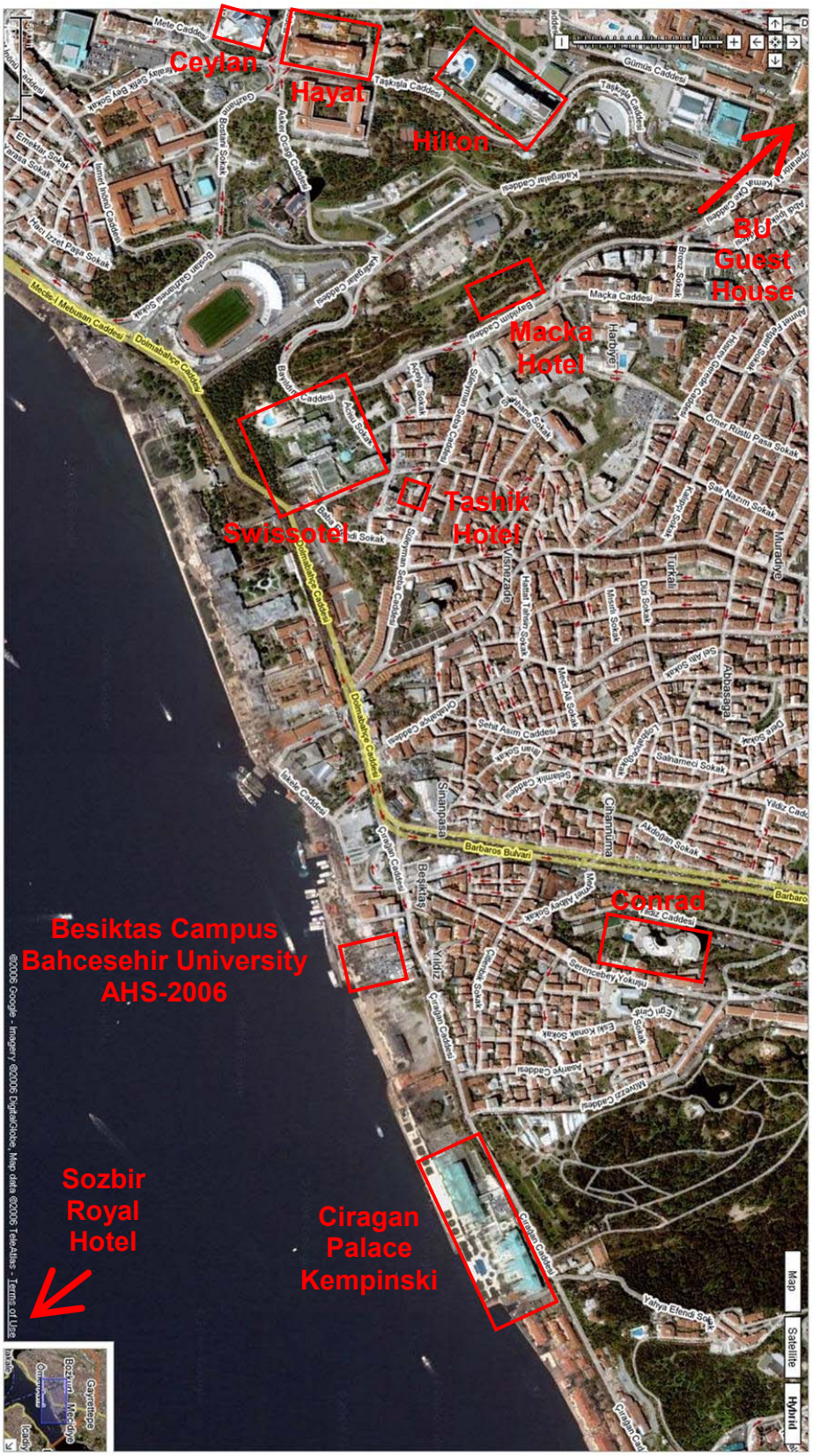
08:45 PM **Savio Chau, Van Dang, Joseph Xu, and James Lu,** JPL, USA
An Automatic Technique to Synthesize Avionics Architecture

08:50 PM **Katarina Paulsson, Michael Hübner, and Jürgen Becker,** Universitaet Karlsruhe, Germany
Strategies to On-Line Failure Recovery in Self-Adaptive Systems Based on Dynamic and Partial Reconfiguration

08:55 PM **Jim Torresen and Jonas Jakobsen,** University of Oslo, Norway
An FPGA Implemented Processor Architecture with Adaptive Resolution

09:00 PM **Lukas Sekanina, Lukas Starecek, Zbysek Gajda, and Zdenek Kotasek,** Brno University of Technology, Czech Republic
Evolution of Multifunctional Combinational Modules Controlled by the Power Supply Voltage

09:05 PM **John Maher, Colin Mullaney, and Fearghal Morgan**, NUI Galway, Ireland
A Platform for Digital Intrinsic Hardware Evolution



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