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ABSTRACT

We report on fabrication of silicon heterojunction (SHJ) solar cells based on Al-backed p-type silicon wafers, with hot-wire chemical vapor deposition (HWCVD) hydrogenated amorphous silicon (a-Si:H) emitter layers. The two-layer emitters are comprised of an extremely thin (~5-nm) intrinsic a-Si:H (a-Si:H(i)) layer topped with a slightly thicker phosphorous-doped a-Si:H layer (a-Si:H(n)). Open-circuit voltages (V_{oc}) above 620 mV are routinely achieved with a maximum of over 640 mV, indicating effective passivation of the crystalline silicon (c-Si) surface by the thin a-Si:H(i/n) stack. We used real-time spectroscopic ellipsometry (RTSE) as an in-situ diagnostic tool to monitor film thickness and roughness in real-time and to observe silicon crystallinity by further ex-situ data analysis. The deposited films were also examined by high-resolution transmission electron microscopy (HRTEM). Immediate a-Si:H deposition and a flat interface to the c-Si is the key factor in obtaining high V_{oc}. On commercial p-type B-doped Czochralski silicon (CZ-Si) wafers with a polished surface and 2.1 Ω·cm resistivity, the best efficiency obtained is 14.8%. Efficiency above 15.7% is achieved on a 1.3 Ω·cm, p-type B-doped float-zone silicon (FZ-Si) wafer with a chemically polished front surface and a screen-printed Al-BSF.

1. INTRODUCTION

Although plasma-enhanced chemical vapor deposition (PECVD) is the dominant method for heterojunction silicon solar cell fabrication, HWCVD may have simpler reactor design and control, higher deposition rates, reduced ion bombardment of the base wafer, and atomic hydrogen (H) generation, which can be used for in-situ surface treatment and may passivate the c-Si. Furthermore, knowledge learned from the development of HWCVD heterojunction solar cells will advance our understanding of the a-Si/c-Si heterointerface.

The most important step in SHJ device development is to determine the optimum deposition condition for a-Si:H(i) and a-Si:H(n) layers to obtain immediate a-Si:H deposition with an abrupt interface to c-Si with good conformal coverage, no epitaxy, and insensitivity to c-Si substrate orientation. With RTSE and HRTEM as the in-situ and ex-situ characterization tools, it was found that, under the conditions at which a good a-Si:H film is deposited on a glass substrate, epitaxial growth on a clean c-Si substrate is usually obtained [1]. The extent of epitaxial growth is larger as substrate temperature gets higher or with a (100)-oriented wafer. Similar deposition ambiguities have also been reported by E. Centurioni [2]. Partial epitaxy is especially difficult to avoid with HWCVD. This is undesirable because it roughens the a-Si/c-Si interface and increases the interface area and may increase the total number of interface defects. Worse yet, if part of the epitaxy reaches the doped a-Si:H region, the much higher density of trap states in doped a-Si:H (compared to those in a-Si:H(i)) will provide tunneling recombination centers for photo-generated electrons and degrade the solar cell performance. The best interface passivation and solar cell performance is achieved by a clean and flat c-Si surface in contact with a-Si:H(i). To optimize a heterojunction solar cell's performance, the a-Si:H(i/n) emitter thickness must be minimized so that parasitic light absorption in the emitter is reduced. Finally, the a-Si:H(i) should be as thin as possible too

permit photogenerated holes to tunnel through to the doped a-Si:H(n) layer [3]. Here we report improved device performance after carefully tailoring growth conditions to obtain abrupt a-Si:H growth for truly heterojunction c-Si devices.

2. EXPERIMENTAL

Fig. 1 shows a schematic of our SHJ device structure. The pre-cleaned medium quality, commercial p-type B-doped CZ-Si wafers used in our device development have a polished front surface and a damage-removed back surface. We have studied a wafer resistivity range from 0.4 to 3 Ω·cm. These wafers are diamond scribed and cleaved into 25-cm by 50-cm substrates that fit into our HWCVD chamber. They are then subjected to a stringent cleaning procedure including degreasing in trichloroethylene, acetone, isopropyl alcohol, and methanol followed by drying with N_2 gas. This is followed by 1) an immediate 10-min soak in boiling de-ionized (DI) water (90 MΩ·cm), 2) a 1-min DI water cascade rinse, 3) a 1% by volume hydrofluoric acid (HF) dip for 1-min or until the c-Si surface turns hydrophobic, 4) a 1-min DI water cascade rinse, and 5) drying with N_2 gas. We then deposit 800-nm of aluminum at 2-nm/s by electron beam evaporation at room temperature on the back surface and alloy this back contact in a quartz tube furnace at 600°C for 20-min in 99.999% pure (5-N) forming gas (10% H_2 + 90% N_2). This Al-based back contact is capable of achieving 80% fill-factor and V_{oc} exceeding 640 mV. Chemically polished 1.3 Ω·cm p-type B-doped FZ-Si wafers are cleaved into the same size as the CZ-Si substrates, screen-printed with Al paste and fired at a peak temperature around 750°C for a few minutes at Georgia Tech. At NREL the same top surface cleaning protocol is performed before HWCVD emitter deposition.

Deposition of the heterojunction emitter a-Si:H(i/n) stack (Fig. 1) is performed by HWCVD with a tungsten filament at ~1800°C . A brief rinse of the front surface with 5-vol.% HF is employed prior to loading substrates onto the HWCVD sample platen and into the chamber load lock maintained at 1x10^{-6} Torr. NREL's System-T HWCVD chamber is equipped with optical access ports for RTSE at a 70° angle of incidence. A typical deposition consists of a brief 10-sec atomic H surface treatment at 60-mTorr with 80-sccm H_2 gas flow at 100-150°C substrate temperature, followed by 10-sec (5-nm) a-Si:H(i) deposition at 100-150°C and 20-sccm silane gas (SiH_4) flow at 10 mTorr. The 5 to 20-nm a-Si:H(n) layer is deposited using SiH_4, phosphine (PH_3), and H_2 gases at 100-300°C substrate temperature and 2.5-sccm, 3-sccm, 50-sccm gas flows respectively. The entire deposition process is continuously monitored by RTSE for in-situ film thickness and surface roughness feedback and for post-deposition analysis of material properties [4].

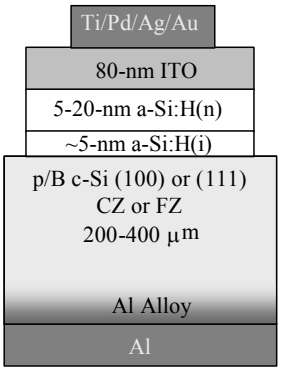

Fig. 1 Schematic of hetero-junction solar cell structure.

With a completed emitter, we then deposit of 80-nm of indium-tin-oxide (ITO) as the front contact and single-layer anti-reflection coating (ARC). The ITO is deposited by thermal evaporation in an oxygen ambient at a substrate temperature of 170°C, from a 5-N purity indium-tin (90% In + 10% Sn) source in a boron nitride crucible at 900°C. This step is also believed to activate the dopants for a-Si:H(n) layers that are deposited at low temperatures (100-150°C). We then deposit the metal (50-nm Ti/60-nm Pd/2-μm Ag/50-nm Au) front grid over the surface of the ITO using a physical shadow mask with 4% grid shadow loss over the 1-cm^2 cell area. A photolithographically defined mesa is used to mask the grid and ITO for device isolation. The ITO is etched using 57-wt. % hydriodic acid in DI water [5] for 5 to 15-min at room temperature. The a-Si:H(i/n) heterojunction emitter is then etched using

reactive ion etching at 20W 13.5-MHz radio-frequency power for 2-min in a sulfur hexafluoride (SF_6) plasma at 130 mTorr.

Illuminated current-voltage characteristics (I-V) of a finished solar cell were measured by a calibrated XT-10 solar simulator maintained by NREL's Measurements and Characterization Division. The simulator was adjusted to approximate AM1.5 direct spectrum current using a primary c-Si reference cell certified in accordance with the world photovoltaic scale.

Internal quantum efficiency (IQE) is measured by combining global reflectance data taken on a Varian Cary 5G UV-Vis-NIR Spectrophotometer and external quantum efficiency (EQE) measured on a grating spectral response system also maintained by NREL's Measurements and Characterization Division. All light sources of the EQE system are filtered and a chopped triple grating monochromator (Acton Research Corporation, SpectraPro-300i) is used to produce the desired narrow spectral bands.

3. RESULTS AND DISCUSSIONS

3.1 AM1.5 J-V Results

Solar cell efficiencies of 15.7% and 14.8% have been achieved on high quality FZ-Si and lower quality CZ-Si respectively as shown in Fig. 2. From the I-V curves of Fig. 2 it is apparent that the V_{oc} for CZ-Si is lower, most likely due to the higher resistivity of 2.1 Ω·cm. This CZ-Si has a minority carrier diffusion length (L_e) of 230-μm and is slightly higher quality than the 1.0 and 0.4 Ω·cm CZ-Si L_e <100-μm we used in earlier studies [1]. An efficiency of 15.7% has been achieved on the high quality 1.3 Ω·cm p-type FZ-Si with a screen-printed Al-BSF. We believe this is the highest reported efficiency for a SHJ solar cell produced by HWCVD. On 1 Ω·cm material a V_{oc} of 628 mV is the highest we have achieved by HWCVD and the highest short-circuit current (J_{sc}) we have achieved is 31.8 mA/cm^2 without employing the high efficiency features like double ARC or texturing. The fill-factor (FF) is 78.8% but reducing the series resistance of the a-Si:H(n)/ITO interface may improve the FF further.

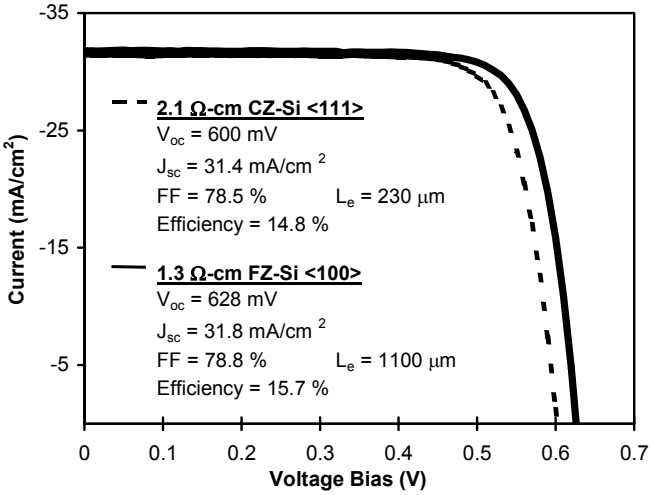

Fig. 2 AM1.5 J-V curve for high efficiency HWCVD SHJ devices on polished p-type B-doped CZ and FZ silicon.

3.2 IQE Results

FZ-Si is typically much higher quality material, which results in much higher FZ-Si cell IQE response than is obtained with the CZ-Si device (Fig. 3). The largest difference between these two devices is the L_e as calculated from the red spectral response [6]. The longer L_e for the FZ-Si material indicates that it is of much higher quality than the CZ-Si. The fact that the L_e (1100-μm) is so much longer than the FZ-Si thickness (250-um) indicates a strong contribution from the Al-BSF. Surprisingly, the good red response of the FZ-Si device did not translate into appreciably higher current than in the CZ-Si device. From the global reflectance curves (Fig. 3) there is >5% reflectance loss even at the minimum in the FZ-Si compared to <1% loss at the minimum reflectance for the CZ-Si device. The efficiency for

the FZ-Si device would be even better had the ITO surface reflectance been as low as the CZ-Si device we suspect; more analysis of variations in ITO is necessary. Optimization of the n-layer thickness is also necessary to improve the blue response for both devices. Fig. 4 shows that the IQE response in the blue spectrum decreases as the n-layer thickness is increased from 10-nm to 30-nm due to parasitic light absorption in the n-layer. However, as the a-Si:H(n) thickness is reduced from 30-nm to 10-nm we also observed a decrease in V_{oc} as great as 10 mV due to shunting or n-layer depletetion. Further optimization of a-Si:H(n) is needed.

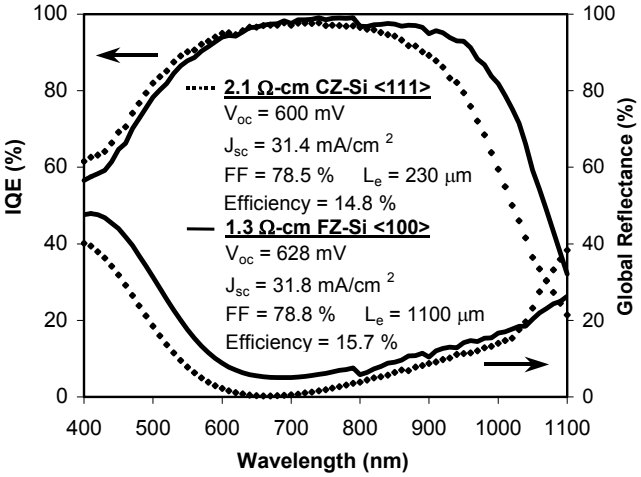

Fig. 3 IQE and global reflectance data for high efficiency p-type B-doped FZ-Si and CZ-Si devices.

4 Summary

We have demonstrated SHJ solar cell conversion efficiencies of 15.7% for FZ-Si and 14.8% for CZ-Si using HWCVD-deposited a-Si:H(i/n) emitter layers on polished p-type c-Si with Al-BSF. With the addition of high efficiency features like surface texturing and double ARC to improve light trapping, these efficiencies will improve significantly.

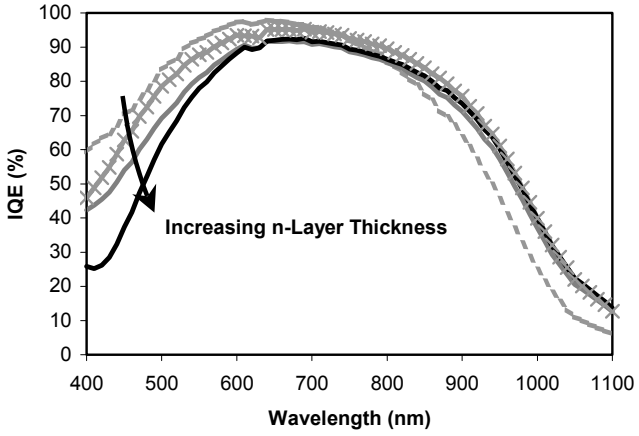

Fig. 4 Plot of IQE for SHJ devices with varying n-layer thicknesses; 10-nm, 15-nm, 20-nm, and 30-nm.

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We report on fabrication of silicon heterojunction (SHJ) solar cells based on Al backed p type silicon wafers, with hot-wire chemical vapor deposition (HWCVD) hydrogenated amorphous silicon (a-Si:H) emitter layers. The two-layer emitters are comprised of an extremely thin (~5-nm) intrinsic a-Si:H (a-Si:H(i)) layer topped with a slightly thicker phosphorous-doped a Si:H layer (a-Si:H(n)). Open-circuit voltages (Voc) above 620 mV are routinely achieved with a maximum of over 640 mV, indicating effective passivation of the crystalline silicon (c-Si) surface by the thin a Si:H(i/n) stack. We used real-time spectroscopic ellipsometry (RTSE) as an in-situ diagnostic tool to monitor film thickness and roughness in real-time and to observe silicon crystallinity by further ex-situ data analysis. The deposited films were also examined by high-resolution transmission electron microscopy (HRTEM). Immediate a-Si:H deposition and a flat interface to the c-Si is the key factor in obtaining high Voc. On commercial p type B-doped Czochralski silicon (CZ-Si) wafers with a polished surface and 2.1 Ω·cm resistivity, the best efficiency obtained is 14.8%. Efficiency above 15.7% is achieved on a 1.3 Ω·cm, p-type B-doped float-zone silicon (FZ-Si) wafer with a chemically polished front surface and a screen-printed Al-BSF.

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