Chapter 9

Forward Silicon Tracker

9.1 Introduction

The ability of BTeV to study beauty and charm decays to unprecedented precision is critically linked to the performance of its tracking system. The BTeV tracking system is based on the pixel detectors, which identify the tracks and determine their momentum in the vicinity of the interaction region, and on seven stations of straw and micro-strip planes, which cover an acceptance of about 300 $mrad$ in the forward region. Silicon micro-strip planes are placed in the innermost region, around the beam pipe, where the particle flux is very high, and cover the acceptance from the beam pipe to the inner edge of the Forward Straw system, which starts at 13 cm.

Our design consists of stations with three planes of 320 μm thick single-sided silicon micro-strip detectors with 100 μm pitch. The silicon sensors, which have an area of about $7.9 \times 7.9\ cm^2$, are arranged in ladders of 4 daisy-chained sensors each, in such a way that four adjacent ladders form a plane as illustrated in Fig. 9.1.

The ladders are mounted on a low-mass carbon fiber support which is designed to ensure a proper relative alignment among all the elements of a single plane and also among different planes within the same station.

The carbon fiber supports (see Fig. 9.18) can be stacked and properly rotated to provide three views in each station, X, U and V. The two stereo views, U and V, are at $\pm$ 11.3^o around the Y bend coordinate. Each plane contains 6144 readout channels; the entire system of 7 stations has 129,024 channels in total (1 arm).

The Si-sensors are the standard p-on-n type and are produced with the same technology developed by the CMS collaboration for their IB2 detectors. They have a multiple $\mathbf{p}^+$ guard ring structure all around the active area to allow high voltage operation. The innermost ring is used to bias the implant through arrays of poly-Silicon resistors.

The front-end electronics is distributed along the two opposite edges of each plane and is cooled by a fluid circulating in a duct embedded in the support structure around the periphery of the plane. The preamplifier chips are AC coupled to the strips by means of

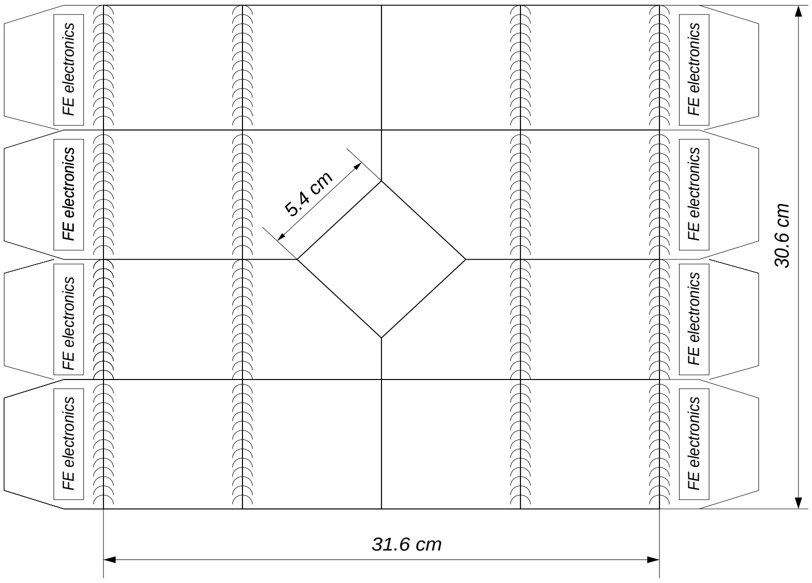

Figure 9.1: Sketch of a silicon detector plane. It consists of four ladders, each with four daisy-chained Si-sensors. The two pairs of sensors on each ladder are read out separately by the front-end electronic chips placed at the two ends of the same ladder. There is some overlap between adjacent ladders to ensure good efficiency over the entire plane.

capacitors directly integrated on the sensors. Each channel is read out in binary mode providing a $\sigma = 100\ \mu m/\sqrt{12} = 29\ \mu m$ resolution, adequate for our physics goals.

The hybrid circuits, which hold the readout chips at each end of the ladders, are connected to the periphery of the forward acceptance cone by means of a very light Kapton flex cable, which carries all the necessary power supplies, control and data signals.

We do not foresee any major problems in building these detectors since we can profit from the enormous experience accumulated in this field in the last few years.

Table 9.1 lists all the geometric parameters and the main characteristics of the Forward Silicon Microstrip system.

This configuration has sufficient segmentation to handle the high hit multiplicities that are expected when $b\bar{b}$ events are produced. Indeed, the peak occupancy value in the silicon strip detectors as predicted by BTeV GEANT is only about 2.4%, for a $b\bar{b}$ event produced at the design luminosity of 2×10^{32} cm^{-2} s^{-1}, accompanied by an average of six minimum bias events at 396 ns bunch spacing.

9.2 Forward Silicon Tracker general requirements

The Silicon Forward Tracker has to fulfill the following general requirements, which are dictated by the physics goals of BTeV.

Property	Value
Silicon Sensors	$\sim 7.9 \times 7.9\ cm^2$, p-on-n type
Pitch	100 μm
Thickness	320 μm
Sensor configuration	4 ladders with 4 sensors each
Coverage	$30.6 \times 31.6\ cm^2$
Central Hole	$5.4 \times 5.4\ cm^2$ ($7 \times 7\ cm^2$ for last station)
Total Stations	7
Z Positions	85.5, 127.5, 185.5, 277.5, 321.5, 371.5, 714.5
Views per Station	3 (X,U,V)
Channels per view	$6,144$
Total Channels	$129,024$
Readout	Sparsified Binary

Table 9.1: Properties of the forward silicon micro-strip tracker.

9.2.1 Resolution and mass

The granularity of each micro-strip plane is one of the defining characteristics of the system. The granularity has been chosen to keep the occupancy per strip at the level of a few percent when a $b\bar{b}$ event is produced at 2×10^{32} cm^{-2} s^{-1} luminosity. At the chosen value of 100 μm pitch, a strip binary read-out is enough to ensure an adequate position resolution for high momentum measurement. Particular care should be devoted to reduce the amount of material in the micro-strip planes.

- **Granularity**: the strips must have a pitch of 100 μm and a length equal to one half the length of the ladder.
- **Position Resolution**: the spatial resolution of each micro-strip plane must be of the order of 30 μm, corresponding to that achievable by reading out the micro-strips in binary mode
- **Material Budget**: each plane should have no more than 0.5 % of a radiation length (averaged over a 30 cm radius circle around the beam pipe)

9.2.2 Readout

BTeV is designed to operate at a luminosity of 2×10^{32} cm^{-2} s^{-1} with beam-crossing intervals or 132 ns or 396 ns. In the latter case, an average of 6 interactions per beam crossing are expected. No Level 1 Trigger is available to readout micro-strip data. All hit data must be read out in a zero suppressed format, and spurious hit data must be minimized. The micro-strip system must have high enough bandwidth so that all data from every beam crossing can be read out and temporarily stored for high-level trigger decision and eventually data acquisition.

- **Binary Readout**: the micro-strip readout should be binary with a threshold of about 0.2 MIP
- **Time Resolution**: time resolution of the micro-strip system has to be such that the output signals are latched in the right bunch crossing, even at 132 ns bunch crossing period.
- **Noise**: the noise rate of the system must be less than 10^{-3} per strip.
- **Efficiency**: at design luminosity, each micro-strip plane must have a hit efficiency of about 95 %, at least, during its entire operational lifetime. This includes losses due to dead strips, noisy strips whose output is suppressed, and any loss of data by readout electronics, or readout dead time.
- **Readout bandwidth**: the micro-strip readout should be very fast and data-driven. This means that all hit strip data have to be read out and be available to the trigger processor every bunch crossing.

9.2.3 Radiation hardness

The anticipated radiation field at the micro-strip detectors has been estimated with BTeV GEANT and MARS calculations. The hottest region will be those nearest the beam on each detector element. Radiation hardness requirements are driven by the most exposed plane near the interaction region. Here, the integrated number of minimum ionizing charged particles per ten years of running at a luminosity of 2×10^{32} cm^{-2} s^{-1} has a peak value of $\sim 2 \times 10^{14}$ cm^{-2} on the inner detector edge around the beam pipe and falls out roughly to a value of $\sim 10^{13}$ cm^{-2} on the detector periphery, where readout electronics is located. The detector components must continue operating in this environment, with acceptable levels of signal-to-noise, operating voltages, efficiency, and spatial resolution.

- **Radiation Tolerance**: All the components of the micro-strip system, including readout chips, sensors and glues must remain operational up to 10 years of BTeV running at the nominal luminosity.

9.2.4 Dimensions

The micro-strip detector dimensions are chosen to cover all the inner zone of the forward acceptance, where the particle flux is too high to be handled by straws. The inner hole on the planes is determined by the radius of the beam pipe, which is constant for all stations except the last one.

- **Size of micro-strip planes**: the dimensions of the active area of the micro-strip planes must be 27×27 cm^2 at least.
- **Size of the inner hole**: the size of the inner hole in the micro-strip planes should be 5.4×5.4 cm^2 for the first 6 stations and 7×7 cm^2 for the last one.

9.2.5 Electrical & Magnetic Interference

The micro-strip detector system must be designed to withstand the magnetic forces that occur on materials inside the vertex magnet and in its extensive fringe field region. In addition, it must be able to withstand the transient-induced eddy current forces that occur on any electrically conducting material when the vertex magnet is ramped to maximum current, or, more importantly, when it trips off.

- **Immunity from dipole magnet**: All the micro-strip detector system and its readout electronics must not be affected by the presence of the 1.6 T magnetic field or by tripping of the magnet.

9.3 Sensors

The sensors we plan to use have a 100 μm pitch and 320 μm thickness.

Referring to Fig. 9.1, the shape of the employed sensors is squared, $\sim 7.9 \times 7.9$ cm^2, with the exception of the four sensors surrounding the hole for the beam pipe. In this case two kinds of sensors with a corner cut-out at 45^0 are adopted, one the mirror image of the other.

The most important parameter that has to be taken into account in order to define the type and the technology of the BTeV sensors is the radiation environment where they are expected to operate. In BTeV, we expect a radiation level at the silicon detectors that decreases rapidly with increasing distance from the beam.

Important radiation damage effects will be confined to a small region closest to the beam line.

The highest level of radiation occurs at the station nearest to the interaction region. As shown in Fig. 9.4, the maximum value of the fluence is expected to be $\sim 1.6 \times 10^{13}$ $particles/cm^2/year$, given a luminosity of 2×10^{32} cm^{-2} s^{-1}.

The most severe problem induced by radiation is related to the change of doping concentration in the bulk, which causes important variations of the full-depletion voltage.

In our particular situation of highly non-uniform irradiation, this means that we have to provide a bias-voltage suitable to simultaneously fully deplete both the less radiation damaged regions as well as those highly damaged. We also have to ensure that this bias voltage remains lower than the breakdown voltage during for the entire operation of the detectors.

Several measurements have been carried out by the ROSE [2] and the CMS [4] collaborations on the radiation hardness of the silicon micro-strip detectors. In general, it turns

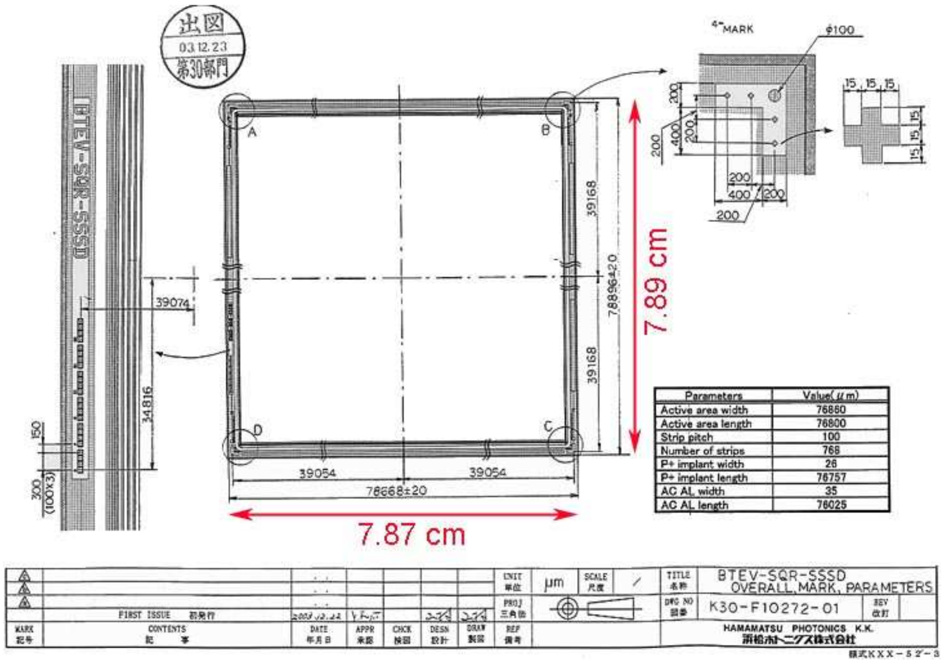

Figure 9.2: Details of the silicon strip sensors. Shown are the alignment markers placed along the sensor borders.

out that in order to limit/delay the degradation of performances due to the reverse annealing, the sensors should be kept at low temperature, typically between $-5C^o$ and $-10C^o$. For detectors with characteristics similar to ours [3], measurements [2] and simulations [4] have confirmed that, after a uniform irradiation of $\sim 2 \times 10^{14}/cm^2$ 1 MeV neutrons, the full-depletion voltage still remains lower then 400 V. This fluence corresponds to about 10 years of BTeV operation (we used the conversion factors quoted in [5]). By lowering the bulk resistivity at 1-3 $K\Omega\ cm$, one can even improve the radiation hardness by shifting toward higher values the fluence at which the *type-inversion* takes place. The second critical parameter that was measured as a function of the irradiation dose is the breakdown voltage. With a proper choice of technology [6] the breakdown voltage still remains higher than 500 V after the same dose of $\sim 2 \times 10^{14}/cm^2$ 1 MeV neutrons. For these sensors, a particular ratio between strip width and pitch, $w/p = 0.25$, was chosen as a compromise between a low total strip capacitance and a stable detector operation at high voltage. Each strip had a metal overhang in order to enhance the breakdown performance. It was determined that for the $< 100 >$ crystal orientation the inter-strip capacitance does not depend on the irradiation dose.

On the basis of the previous arguments, the Si-sensors we intend to use in BTeV are of the standard p-on-n type and are produced with the same technology developed by the CMS collaboration for their IB2 detectors. They have a multiple $\mathbf{p}^+$ guard ring structure

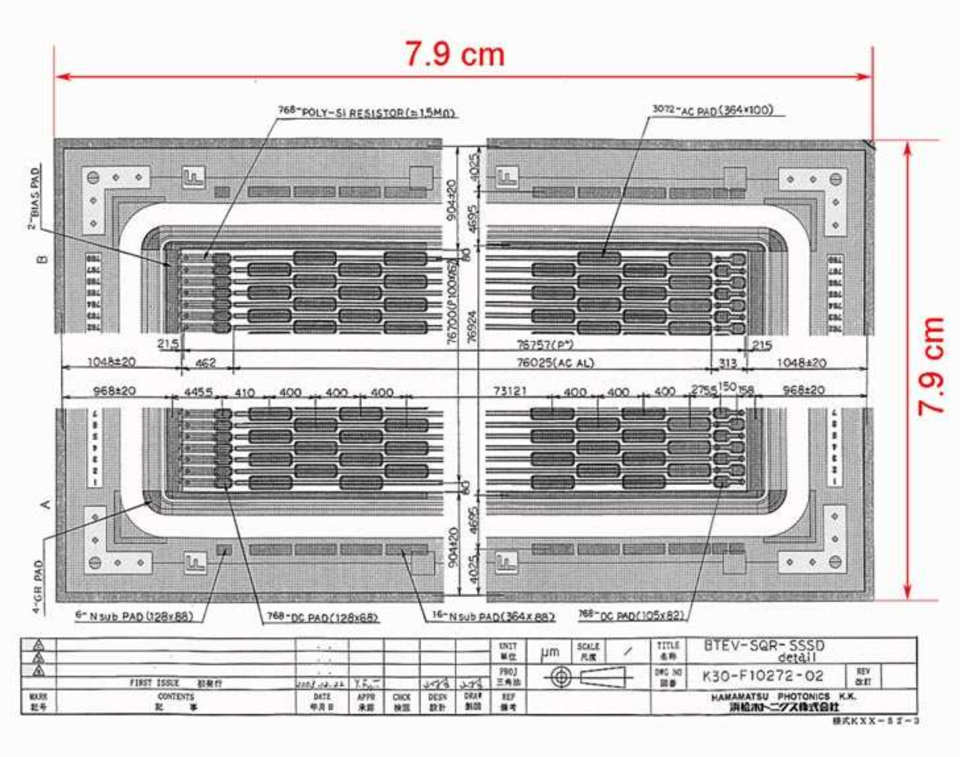

Figure 9.3: Detailed layout of the silicon sensor.

all around the active area to allow high voltage operation. The innermost ring is used to bias the implant through arrays of poly-Silicon resistors. These sensors can be provided by several vendors, such as Hamamatsu, ST or SINTEF. We bought a dozen of these sensors from CMS (CMS IB2 sensors, 61×116 mm^2 active area, 120 μm pitch, 320 μm thickness, $30 \mu m$ implant width, $< 100 >$ crystal type) to certify their performance and their radiation tolerance at the doses expected in BTeV. Our preliminary results from the irradiation tests we performed last summer at the University of Indiana Cyclotron Facility demonstrate that this type of sensors can be safely used in BTeV without any important degradation of their performance for at least ten years.

After an absorbed dose of 5 MRad (equivalent to the maximum dose expected in a small annular region surrounding the beam-pipe after ten years of operation in BTeV), the loss of signal is limited to only a few percent, provided the bias voltage is raised to 350 V. The reverse current can be heavily reduced in the range of a few tens of microAmperes, with enormous benefits in terms of noise, if the sensors are run at a temperature around $-10\ ^0C$.

For additional details of our measurements on irradiated sensors we invite the reader to refer to the specific R&D section at the end of this chapter.

The general layout of the sensors we intend to use in BTeV is given in Fig. 9.2 and the details of the strips and the guard-rings in Fig. 9.3.

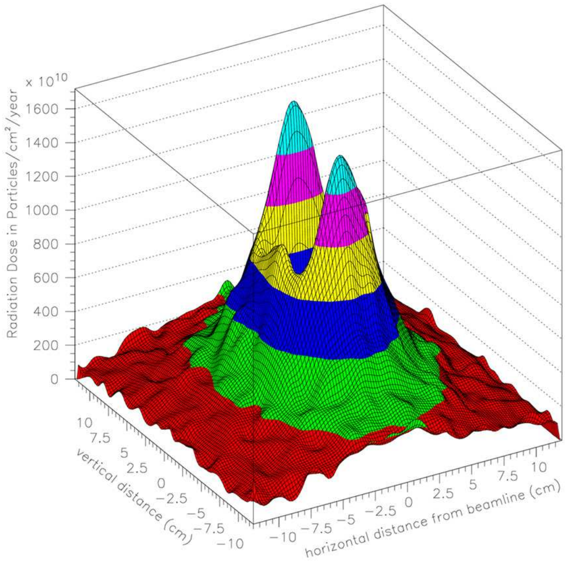

Figure 9.4: Radiation dose as a function of position in Forward Silicon Tracker Station # 1. The horizontal magnetic field concentrates more particles above and below the square central beam hole than on either side.

9.4 Electronic Readout

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. The ICs consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping are compared to a preset threshold. To achieve the required position resolution, the channels have to provide only a binary information (hit / no hit), generating a logic 1 at the output if a signal exceeding the threshold is detected. The dimensions of the readout IC are expected to be about 7.5 x 4.5 mm^2, while the power dissipation will be about 4 mW/channel. For each channel with a signal above threshold, the strip number, the chip identification number, and the related bunch crossing number will be read out and transmitted to a Power/Data Splitter Board and afterwards to the Data Combiner Board The readout chips use the same programming and data output interface as the pixel readout ICs, so the same DAQ system can be used. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit above a suitably chosen threshold.

9.4.1 Readout chip

Requirements

The micro-strip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the micro-strip sensors. AC coupling is assumed between the strips and the readout electronics.

- **Binary Readout:** The micro-strip readout should be binary with a threshold of about 0.2 MIP.
- **Time Resolution:** Time resolution of the micro-strip system has to be such that the output signals are latched in the right bunch crossing (even at 132 *ns* bunch crossing period).
- **Efficiency:** At design luminosity, the micro-strip readout must have a hit efficiency of at least 99% during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.
- **Readout bandwidth:** The micro-strip readout should be very fast and data-driven. This means that (on average) all hit strip data have to be read out and be available to the trigger processor every bunch crossing.
- **Radiation Tolerance:** All the components of the micro-strip readout system must remain operational up to 10 years of BTeV running at the nominal luminosity.
- **Dynamic Range:** The dynamic range of the front-end chip should cover up to 2 MIP's.
- **Peaking Time:** The peaking time of the front-end signal at the shaper output should be less than 100 ns and, in any case, such as to ensure that the comparator output be latched in the correct bunch crossing.
- **Noise:** The equivalent r.m.s. noise of the front-end electronics has to be $\sim$1000 e^- at C_D=20 pF and should not increase significantly after irradiation.
- **Threshold and Dispersion:** Each micro-strip channel will be read out in binary mode by comparing its signal to a settable threshold. This analog threshold shall be adjustable via digital control for each channel. Typical settings shall be from 2000 to 5000 equivalent electrons at the input. Threshold dispersion must be low enough that the noise figure of the analog section of the front-end, $\sim$1000 electrons, would not be significantly degraded. Typically, this should be 400 electrons at most and should be stable during its entire operational lifetime.

- **Comparator Time Resolution:** The comparator must be fast enough to guarantee that, for $\sim$100 ns input signal peaking time, the output can be latched in the correct bunch crossing (at 132 ns bunch crossing period)

- **Masking, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.

- **Cross-talk:** Must be less than 2%

- **Power Consumption:** The power consumption of each readout channel must be less than 4 mW

- **Time Stamp:** Each micro-strip hit must be given a correct timestamp

  which identifies the beam crossing number.

- **Control of Analog Circuitry on Power-Up:** Upon power-up, the readout chip shall be operational at default settings.

- **Memory of Downloaded Control of Analog Circuitry:** Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.

- **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.

- **Data Sparsification:** The data output from the micro-strip detector shall only consist of those channels that are above the settable threshold.

- **micro-strip output data content:** The micro-strip hit data must include the beam crossing number, chip identification number, and the micro-strip hits for that beam crossing.

Implementation

The Fermilab Silicon Strip Readout (FSSR) chip is a mixed-signal circuit occupying an area of about 7.5$\times$4.5 mm^2. It can be described as including four logic sections, as shown in Fig. 9.5. They are the core, the programmable registers and digital-to-analog converters, the programming interface and the data output interface. The chosen architecture is called pseudo-Pixel. It is essentially identical to the architecture of the pixel readout chip FPIX. The 128 strips serviced by one chip are sub-divided into 16 sets of 8 strips. Each set is made to behave like a single column in the FPIX architecture. While FPIX is a 22$\times$128 array of pixels, FSSR will look like a 16$\times$8 FPIX. The same programming interface and data interface implemented in FPIX is used again in the FSSR. This implies that there will be a 24 bit data word output by the FSSR. Four bits will be necessary to encode the strip number; 5 bits will be used to encode the set number; 8 bits will be used for the BCO number and 1 bit will be used for the sync bit. This leaves 6 extra bits.

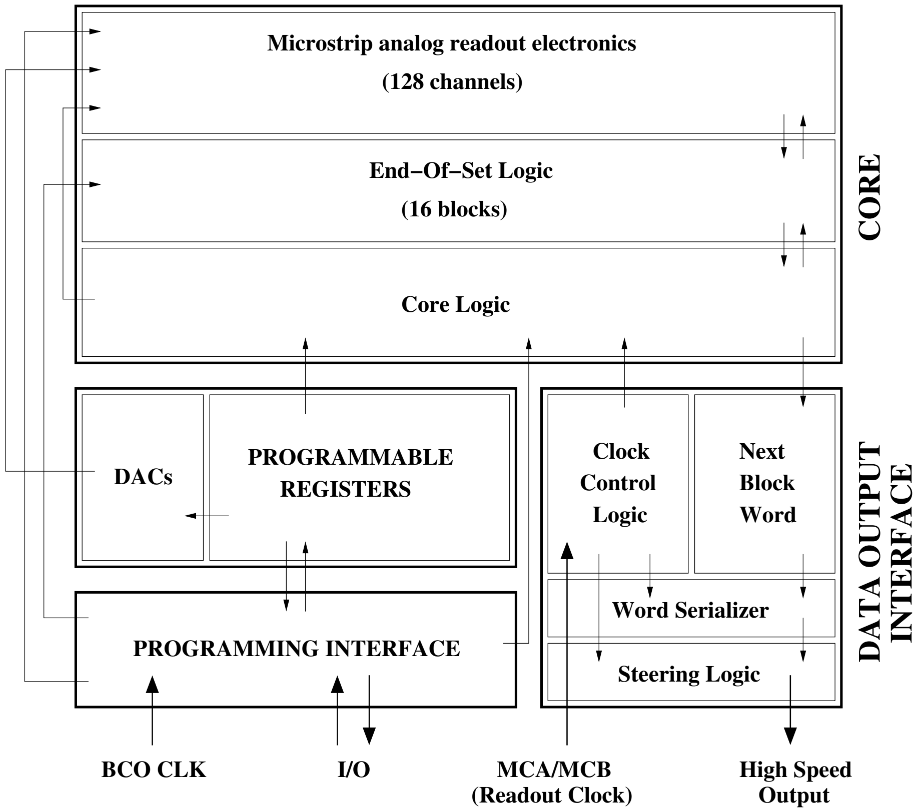

Figure 9.5: FSSR chip block diagram. Arrows represent control and data flow.

The FSSR core consists of 128 analog readout channels, logically subdivided in 16 sets of 8 channels each, the end-of-set logic (16 blocks, one for each set of front-end channels) and the core logic, which controls the data flow from the core to the data output interface. The programming interface accepts commands and data from a serial input bus and, in response to a command, provides data on a serial output bus. The programmable registers are used to store input values for DACs that provide currents and voltages required by the core, for instance the threshold levels for the discriminator in the analog channel. They also have additional functions, such as controlling data output speed and selecting the pattern for charge injection tests. The data output interface accepts data from the core, serializes the data and transmits them off-chip, using a point-to-point protocol. All I/O (except the test signal injection) is differential and is fed by means of Low Voltage Differential Signaling (LVDS). Analog bias is fed to the analog channel blocks, with the exception of the discriminator.

The analog section of the FSSR Core consists of 128 channels, each including a charge preamplifier, an integrator, a shaper and a discriminator. A symmetric baseline restorer may be added in the final version of the chip in order to achieve baseline shift suppression. The block diagram of the analog channel is shown in Fig. 9.6.

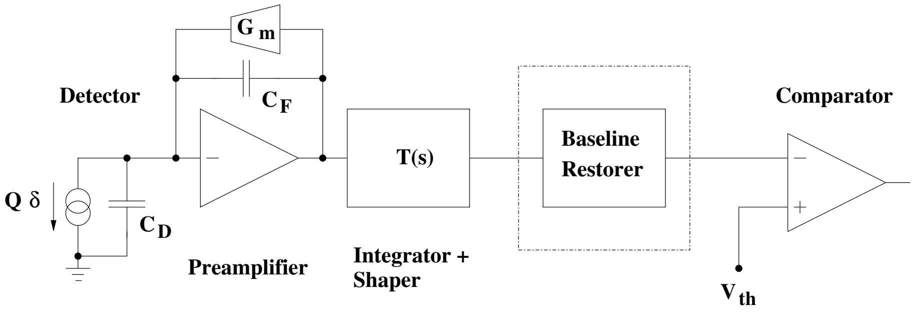

Figure 9.6: FSSR analog channel block diagram. G_m is the preamplifier transconductor, C_F is the preamplifier feedback capacitance, C_D is the detector simulating capacitor and V_{th} is the discriminator threshold voltage. For the sake of simplicity, integrator and shaper are represented by a single block, whose transfer function is $T(s)$.

The Core communicates with the other FSSR logical blocks through the Core Logic. The 128 front-end channels are subdivided in 16 sets of eight channels each. Each of the 16 blocks composing the End-Of-Set Logic deals with one of the eight channel sets. Operation of the FSSR Core is similar to the FPIX Core and is schematically represented in Fig. 9.7. The ChipHit and ChipHasData lines shown in the picture are two diagnostic signals. In particular, ChipHit goes high whenever a discriminator fires while ChipHasData goes high every time the core has data to output.

The Programming Interface is the same as in FPIX. It provides a means for the user to control the operation of the FSSR chip, and to load and read back the contents of any of the Programmable Registers.

R&D

The R&D to support the development of the FSSR chip has begun in 2002.

The chosen technology for integration is a deep submicron CMOS process, which can be made highly radiation resistant with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. In particular we are considering the TSMC (Taiwan) process with 0.25 μm minimum feature size, which has been successfully used for the implementation of the FPIX pixel readout chip. This allows to use FPIX as a prototype for the FSSR back-end, reducing the number of needed prototypes and the overall cost.

The readout architecture[11], with the 128 front-end channels subdivided into 16 sets of eight channels each, was tested with realistic data created by Monte Carlo analysis of the interaction region, assuming 132 ns beam crossing period running with a back-end clock

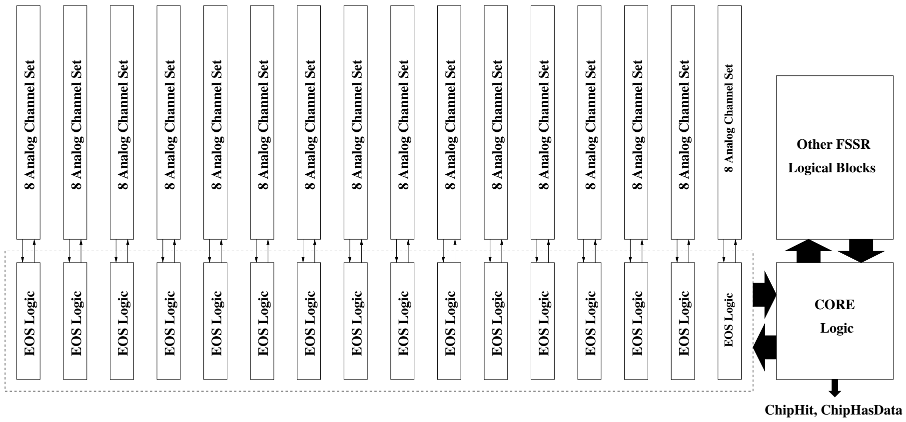

Figure 9.7: Block diagram of the FSSR Core.

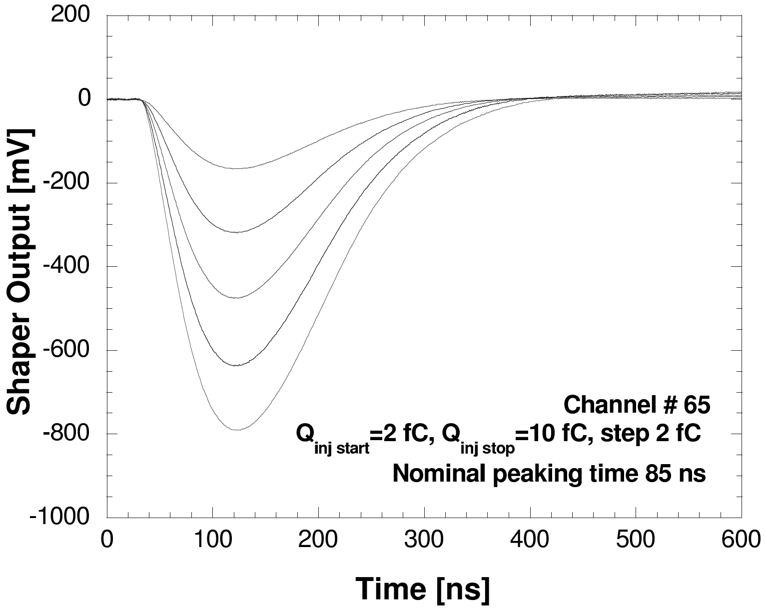

Figure 9.8: Waveforms at the output of the shaper in the FSSR prototype at a peaking time setting t_P=85 ns.

equal to 4 times the BCO clock frequency. Verilog simulations indicate the chip will be able to operate with the required 99% efficiency.

The analog section of the chip [9] [10] was simulated and optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. Table 9.2 shows the main parameters of the analog section as obtained from the simulations.

It is possible to select the peaking time of the signal at the shaper output (60 ns, 85 ns, 125 ns) by changing the value of capacitors in the integrator and in the shaper. In this

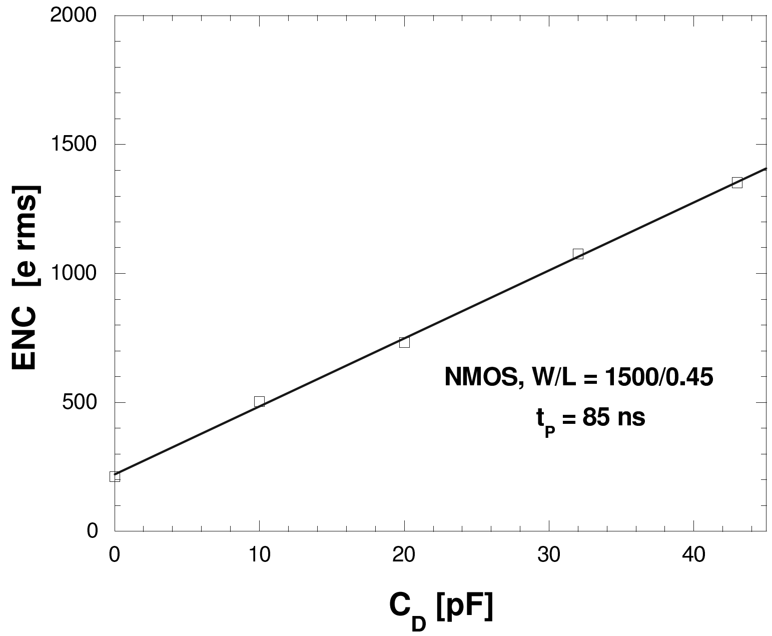

Figure 9.9: Equivalent Noise Charge ENC as a function of the detector capacitance CD at a peaking time setting t_P=85 ns in the FSSR prototype. The preamplifier input device is an NMOS with W/L=1500/0.45.

way the noise performances of the chip can be optimised according to the signal occupancy, preserving the required efficiency. The first FSSR prototype was submitted in July 2003. This prototype has the same structure as the final chip.

It consists of 114 analog channels connected to a full back-end section. The prototype was successfully tested. Both the analog front-end and the digital back-end were found to function properly. Fig. 9.8 and Fig. 9.9 show the measured signal waveforms at the shaper output and the Equivalent Noise Charge ENC as a function of the detector capacitance CD. These data are in very good agreement with simulations, and noise performances are inside the specifications. ENC values for channels with different input device differ by 10-15 %. Work is under way to perform tests with strip detectors. Given the successful results of the first prototype, the submission of a full-scale, 128-channels chip prototype is foreseen in late spring 2004.

9.5 Hybrids and Flex cables

Fig. 9.10 provides a sketch of the organization and cabling of the electronics of the micro-strip detectors.

The Data Combiner Boards are the interfaces to the BTeV DAQ. The Junction Card, located outside the acceptance region, repeats the signals between the readout chips and the

Power dissipation	P=3.5 mW (including bias networks)		
Preamplifier input capacitance	C_{in}=2.7 pF		
Preamplifier input device	NMOS, W/L = 1500/0.45		
Charge sensitivity	G_Q=75 mV/fC		
Comparator rms threshold dispersion	σV_{th}= 3.5 $mV\ rms$		
Signal peaking time at the shaper output	t_P=60 ns	t_P=85 ns	t_P=125 ns
Equivalent Noise Charge at C_D=20 pF	870 $e^-\ rms$	710 $e^-\ rms$	590 $e^-\ rms$

Table 9.2: Simulation parameters of the analog section of the FSSR chip.

Power dissipation	P=4.0 mW (including bias networks)
Preamplifier input capacitance	C_{in}=2.7 pF
Preamplifier input device	NMOS, W/L = 1500/0.45
Charge sensitivity	G_Q=75 mV/fC
Equivalent Noise Charge at C_D=20 pF, peaking time t_p=85 ns	ENC=750 e^- rms

Table 9.3: Measured parameters of the analog section of the protoype FSSR chip.

Data Combiner Board and distributes the power to the chips and the sensors. Silicon sensors are connected to the readout chips on the hybrids via pitch-adapter circuits, whose function is to provide a correct matching between the different granularity of the wire bonding pads of the hybrid and the micro-strip; hybrids, in turn, are connected to the Junction Card through very low-mass flex cables, whose first short portion, the *pig-tail*, can be detached thanks to miniaturized connectors; and, finally, the Junction Card is connected to the power supplies and to the Data Combiner Board by means of regular cables. The actual modularity of the electronics is that indicated in the sketch: one Data Combiner Board serves one Junction Card, which, in turn, serves four hybrids, i.e. four half-ladders. The hybrid substrate is composed of Beryllium Oxide, a very reliable technology which was successfully employed for the proposed RUN IIb upgrade of the CDF Silicon tracker. Details of the hybrid circuit, the pig-tail flex cable and the flex cable are given in Fig. 9.11, Fig. 9.12 and Fig. 9.13 respectively.

In the present prototype version of the hybrid, see Fig. 9.11, we used and connected to the flex-cable all the serial data outputs and controls of the readout chips. These sum up to 56 differential signals or 112 lines. In the final layout, both for the hybrids as well as for the flex-cables, we will use only the lines required by our expected data-rate.

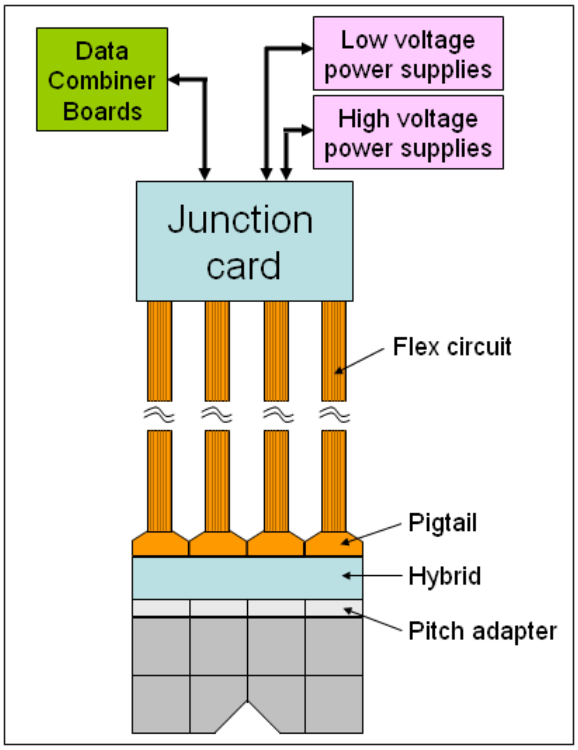

Figure 9.10: Organization and cabling of the micro-strip detector electronics: the Junction Card, located outside the acceptance region, repeats the signals between the readout chips and the Data Combiner Board and distributes the power to the chips and the sensors. The electrical connection between the Junction Card and the detectors is provided by very low-mass flex cables.

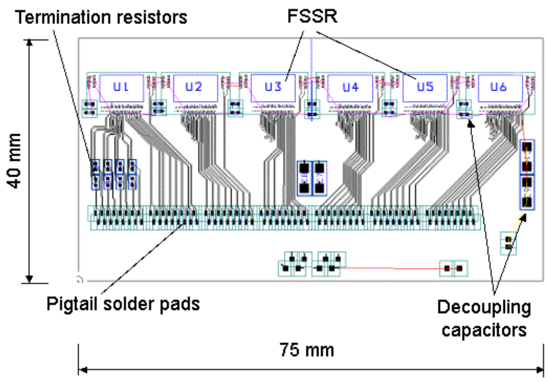

Figure 9.11: Layout of the hybrid circuit lodging six FSSR read-out chips.

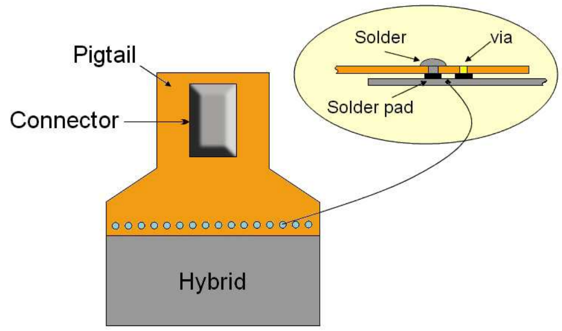

Figure 9.12: Schematics of the *pig-tail* which connects the hybrid circuit to the flex cable.

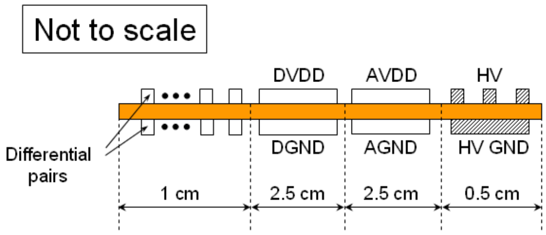

Figure 9.13: Cross section of the flex cable. Signal differential pairs, digital (DVDD) and analog (AVDD) low-voltage power supply as well as high-voltage power supply (HV) are shown. The mean radiation lenght of these cables is about 0.2 %.

9.6 Mechanical support and cooling system

9.6.1 Requirements

The mechanical structure of of the micro-strip detector system and the embedded cooling system have to fulfill the following requirements.

9.6.1.1 Mechanical Support System

Each micro-strip detector plane must be divided in two halves to allow for the assembly around the beam pipe. Since each half could be pre-assembled with extreme accuracy in a properly equipped lab and even the relative alignment between the two halves of a plane could be guaranteed by an adequate mechanical design, particular attention should be devoted to define requirements for the final assembly procedure in the experimental hall. Proper alignment marks should be provided both on the mechanical structure of the system and on some fixed reference of the hall. Proper survey instrumentation should be available for the final assembly. Once the detector stations are assembled with a precision of $100\ \mu m$, fine alignment can be established offline by a conventional track-residuals minimization procedure. The main requirement is to ensure sufficient stability of the system to maintain the alignment. Alignment monitors should be included in the design to maintain online control of the most critical points of the structure and eventually to set alarms.

- **Low Mass**: the micro-strip detector mechanical support structure should have low enough mass to meet the previous general requirements.
- **Division in halves**: the mechanical structure of each plane should be divided in two halves to allow for the final assembly around the beam pipe and to permit maintenance without breaking vacuum.
- **Alignment Marks**: The micro-strip system must provide suitable alignment marks for surveying during each phase of the assembly.
- **Alignment on the halves**: The alignment accuracy between components and relative to the reference marks on each half of a plane should be better than 5 μm.
- **Alignment of the two halves**: The alignment accuracy between the two halves of the same plane should be better than 10 μm and should be guaranteed by a proper mechanical design.
- **Alignment of different planes**: The relative alignment accuracy among different planes within the same station should be better than 20 μm.
- **Alignment of different stations**: The alignment of different stations should be better than 100 μm with respect to the external reference marks.
- **Operating Temperature**: The design must take into account that the operating temperature of the detector will be around $\sim -10\ ^0C$ and $-5\ ^0C$. Thermal stress must be considered so that the mechanical stability of the system will not be affected.
- **Alignment Stability**: The alignment stability should be in the range of a few microns in the real experimental conditions.
- **Alignment Monitor**: The alignment of the system must be monitored during the operation by means of a suitable device which allows for a better than 10 μm precision.

9.6.1.2 Cooling System

The amount of heat dissipated by the readout electronics is expected to be 12 W per half plane and is concentrated on the hybrid circuits where the chips are located. The micro-strip detector is expected to operate at a temperature around $-10\ ^0C$. The effects of radiation damage are minimized by maintaining these temperatures even when the devices are not in use. Thus, a cooling system must be designed to operate within this temperature range. Since the heat load is concentrated in a few spots of the system it is practically impossible to achieve a good uniformity of the temperature across the whole detector. Nevertheless a suitable cooling system should be designed to maintain a sufficient temperature uniformity in the whole structure and even on the sensors to avoid any appreciable degradation of the detector performance. The temperature must be controlled and reproducible. Since the operation is well below the temperatures at which the devices will be assembled, the coefficients of thermal expansion must be considered in the mechanical designs.

- **Thermal Uniformity**: the maximum temperature excursion in all the system but the front-end chips, once equilibrium is reached, shall not exceed $\pm$ 5 ^0C on any plane.
- **Thermal Stability**: the temperature stability in all the parts of the system must be better than $\pm$ 1 ^0C during its operational lifetime .
- **Temperature Reproducibility**: the average temperature of the system shall be reproducible (under active control) to $\pm$ 1 ^0C.
- **Temperature Read-back**: The temperature of each ladder hybrid shall be readable to a precision of $\pm$ 0.5 ^0C.

9.6.2 Implementation

The support structure we are elaborating with a specialized Italian company consists of several practically identical elements, which must be combined together to assemble a station.

The basic element of the system is a *ladder*, depicted in Fig. 9.14, consisting of a thin carbon fiber support and capable of holding four silicon strip sensors and the read-out hybrid circuit at the two opposite ends.

The element of the structure, which serves as support for a half plane, is sketched in Fig. 9.15. It consists of a very light composite structure made of a sandwich of two thin carbon fiber layers with Rohacell inside. The two ladders of the half plane are attached on the opposite sides of this structure, one on front plane, the other on the back plane. A cooling duct is located inside the structure and reaches the regions where the hybrid circuits are located and the heat load is concentrated. The total material on each plane, including the support, the ladders with sensors, hybrids and pitch adapter is about 0.4 % of a radiation length (averaged over a 30 cm radius circle around the beam pipe), thus meeting our requirements.

The structure is designed in such a way that two half-planes can be coupled together to form a plane and three planes can be stacked to form a station. The relative positioning of the six elements comprising the station is guaranteed by suitable pins, such to provide a relative alignment of the two halves of a plane to within 10 μm and that of different planes to within 20 μm.

By covering the bottom and the top of the stack with a very light material, having some additional care for the interface with the beam pipe (see Fig. 9.19), we naturally define a station enclosure, in which we can improve the temperature uniformity. Indeed, once

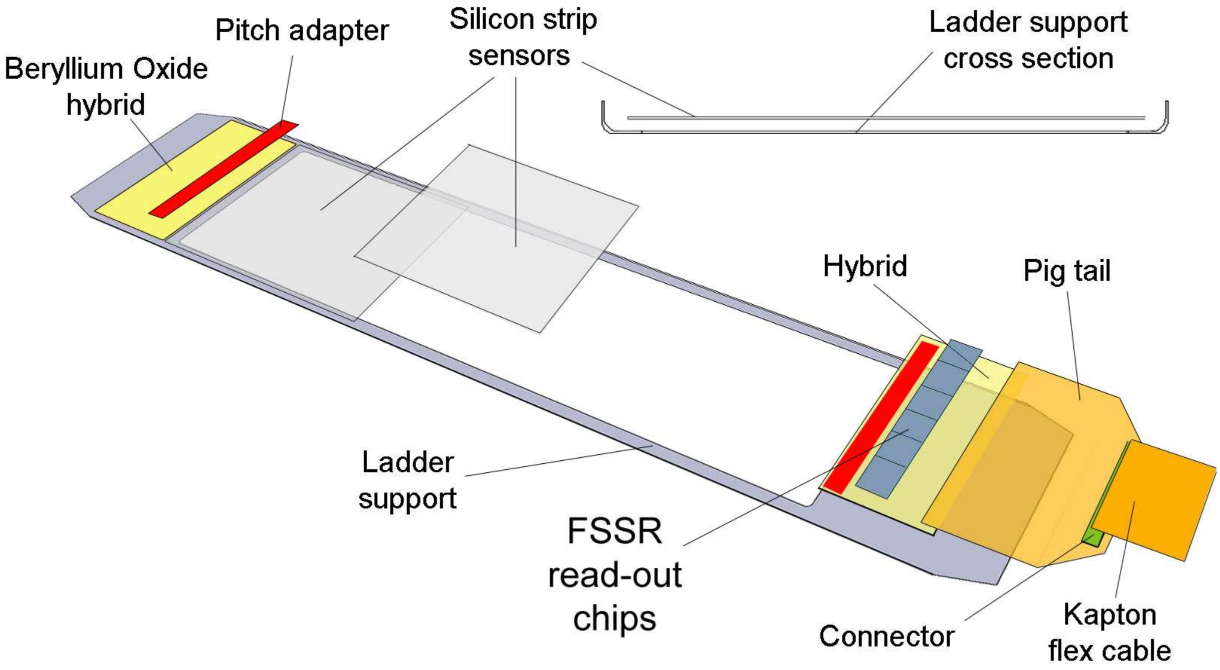

Figure 9.14: Sketch of a ladder support and the relative placing of silicon strip sensors, hybrid circuit, pig-tail fan-out and kapton flex cable.

the stack is immersed in a dry-air atmosphere, the gas exchange with the outside will be drastically reduced and even the dry gas filling the enclosure will be efficiently cooled by the inner walls of the carbon fiber structure, which are in close contact with the embedded cooling ducts.

The support structure described above, constitutes what we call the *"micro-strip inner support"* since an additional structure, *"the outer support"*, is required to hold the stations in their final position around the beam pipe. For this additional support we developed a solution designed to reduce as much as possible the amount of material in the acceptance. Since the straw tubes in this region are interrupted because of the presence of the beam-pipe and thus require a support which can take their tension, we designed a structure which serves as support both for the straw tubes and the micro-strip station. This additional support is directly integrated in the straw structure as shown in Fig. 9.17. The straws of the two central modules (Module-0 straws) of the X-view are assembled inside a carbon-fiber Rohacell composite strut, which provides them with the adequate tension and has a central disk to support the micro-strip station. This solution avoids any duplication of unnecessary material in the experiment acceptance cone. The central disk and the underlying strut have a radial slot to allow for assembly around the beam pipe. The micro-strip inner supports are

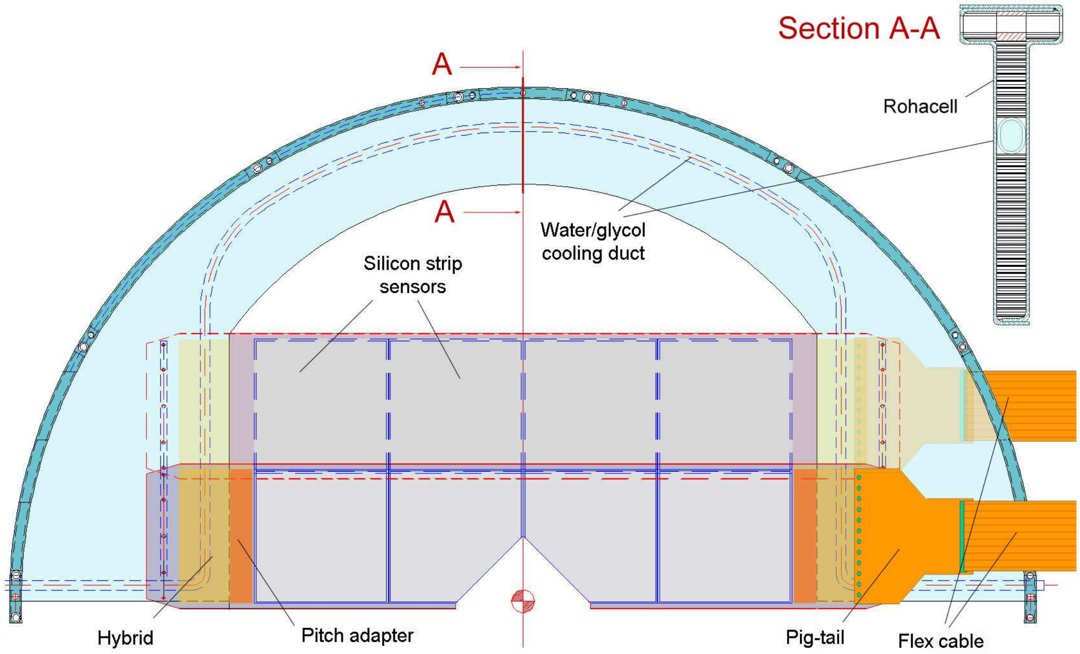

Figure 9.15: Sketch of the mechanical support of a micro-strip detector half-plane. It consists of a very light composite structure made of a sandwich of two thin carbon fiber layers with Rohacell inside. The two ladders of the half plane are attached on the opposite sides of this structure, one on front plane, the other on the back plane. A cooling duct runs through the structure and reaches the regions where the hybrid circuits are located and the heat load is concentrated.

assembled directly on the disk as illustrated in Fig. 9.18. On the same figure we also show how this structure couples with the nearby standard straw chambers. The disk also serves as the bottom cover of the station enclosure once complemented with a proper insert to fill the slot.

At this point, the only missing pieces of the mosaic are the station top-cover and the interface with the beam pipe. In Fig. 9.19 we give a possible solution: once a tube of very light material, such as Rohacell, is fit into the hole of the outer support disk, then a cover with the same shape of the previous disk, but much lighter, can be put on the top of the structure to obtain an ideal enclosure to run the micro-strip detectors. Clearly, this structure should be immersed into a dry-gas atmosphere at room temperature, which must be purged with high enough flow to avoid condensation on the external walls of the inner support and to prevent from cooling the nearby regions.

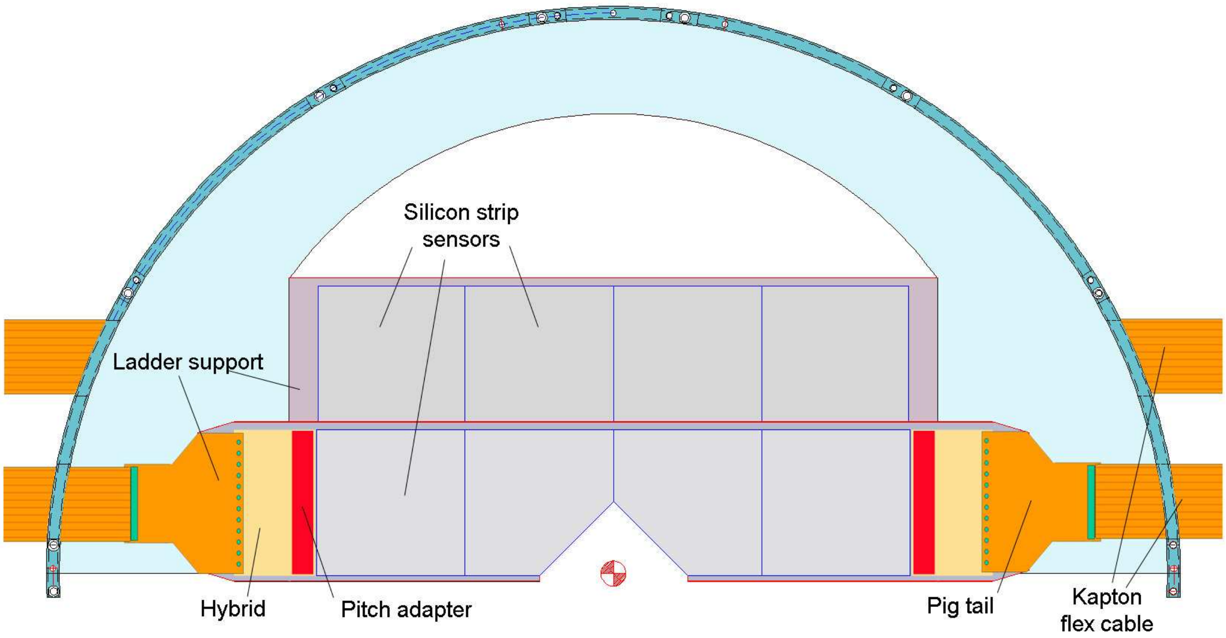

Figure 9.16: Sketch of the micro-strip support showing the organization of flex-cables, which cross the structure through dedicated slots.

9.6.3 Fiber grating positioning monitor

A series of Fiber Bragg Gratings (FBGs) will provide a real time position monitoring of the Microstrip detector support. As already described in the pixel detector chapter, FBG sensors are optical strain gages placed inside the optical fiber core and consequently will not add any additional mass to the one of the fiber. The fiber diameter is about 200 microns including the acrilate coating. It is possible to multiplex several of them in the same fiber.

In Fig. 9.20 we have considered a number of sensors per fiber that varies from a minimum of three to a maximum of six. The sensors are capable of measuring strain along the fiber direction. Using these information it is possible to reconstruct the elastic displacement of the structure. The FBG colored in blue in the picture are mainly devoted to determine the bending of the support along the X-Y plane while the green ones are devoted to determine the bending of the support along the Y-Z plane. There are also four more sensors, reported in red in the picture, that measure the strain in the orthogonal direction with respect to the others (in order to avoid confusion only two sensors have been drawn). These will contribute to the reconstruction of torsional deformations. Finally the sensors in pink are required to monitor the deformation of the plate. As can be seen, the sensors are positioned in such a way to be able to separate bending from pure traction. In fact all sensors are

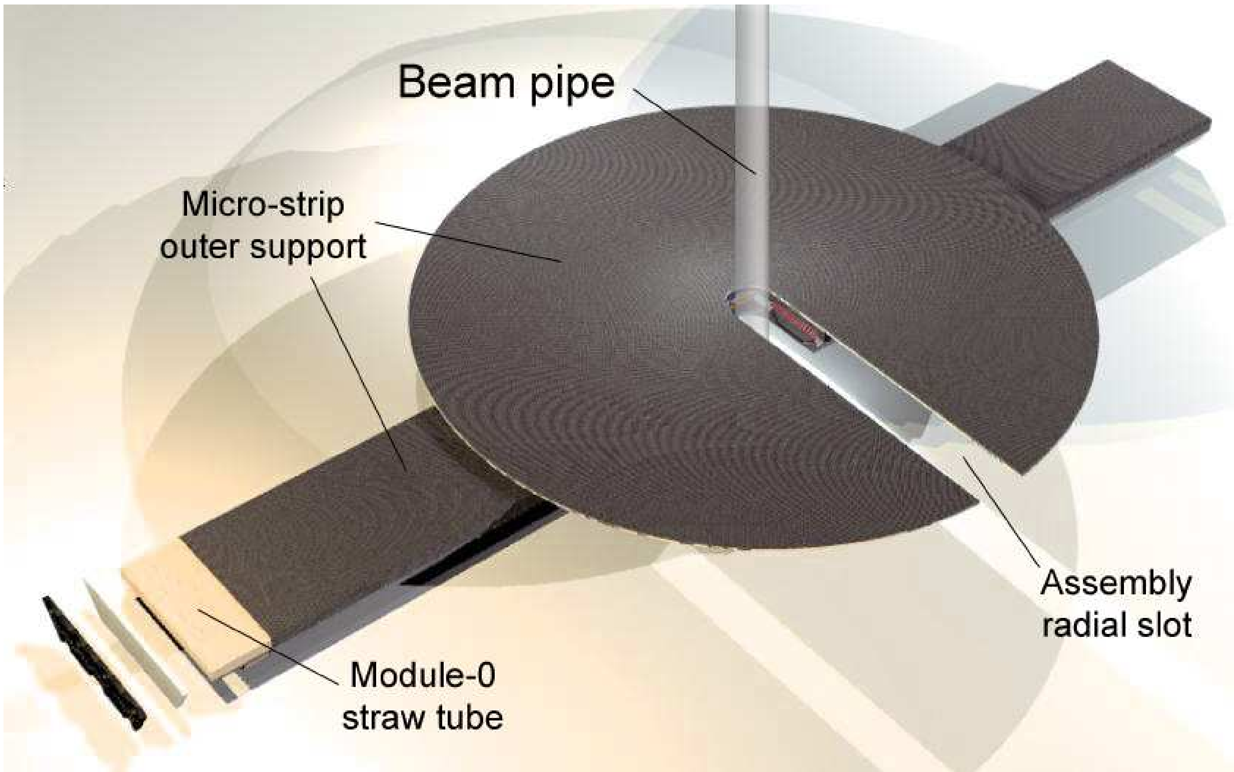

Figure 9.17: The micro-strip outer support structure. It is directly integrated in the nearby X-view straw structure and provides support for the micro-strip stations and the straws themselves. The central disk and the underlying strut have a radial slot to allow for assembly around the beam pipe.

organized in couples. For instance, for each blue sensor on the left, you will have another blue sensor on the right, that allows the separation of pure traction in the Y direction from the bending in the X-Y plane. Analogous considerations can be performed for the other sensors. The blue sensor on the upper left is in the same fiber as the green ones so that this fiber will contain 5 sensors. The other three blue sensors are in an independent fiber. The four red sensors are in another independent fiber. Finally in a fourth fiber six more sensors are considered for monitoring the plate deformations. So with this configuration we have 12 sensors for monitoring deformed shapes of the vertical support and 6 sensors for the plate. The total number of sensors required is 18×6 stations = 108 sensors. Actually at the present stage of study this number of sensors seems underestimated if a high resolution deformation monitoring is required, for this reason the requested number of sensors is 168 typically organized in strings of four sensors per fiber.

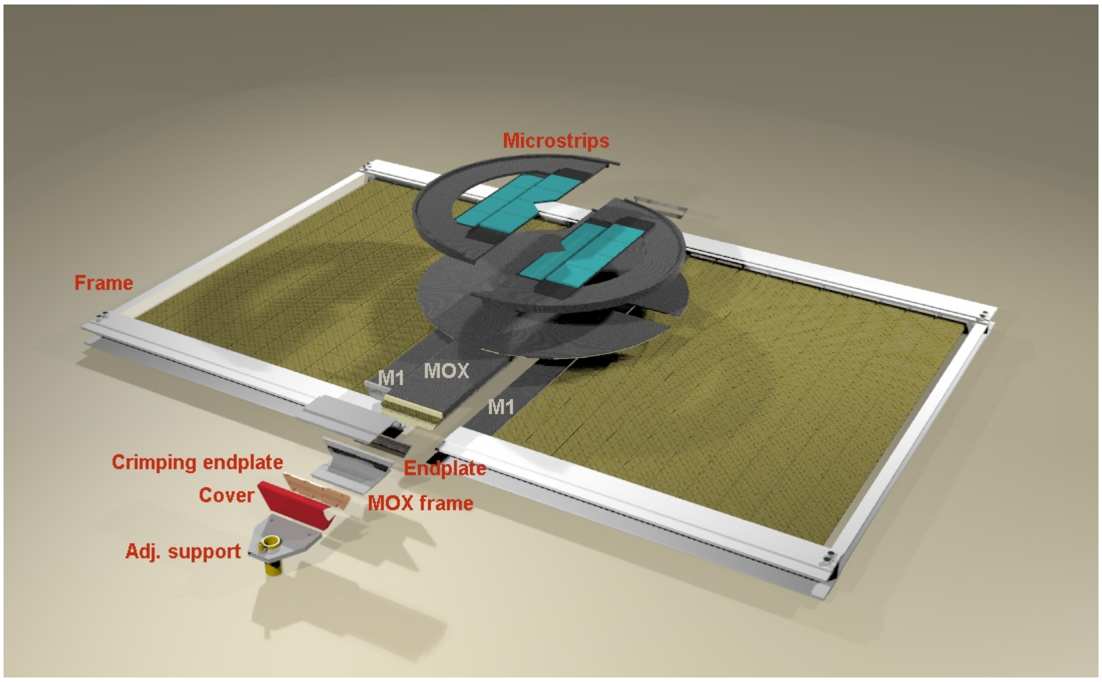

Figure 9.18: Assembly of the micro-strip planes on the outer support structure. The expanded view shows the regular straw tubes in the proximity of the central gap, the micro-strip outer support, which contains the straws to fill the gap, and the two halves of the first micro-strip plane to be assembled on the central disk.

9.6.4 Cooling system

The cooling system for the micro-strip detectors employs a water-glycol liquid mixture flowing in a closed loop circuit at $-20\ ^0C$ and sub-atmospheric pressure. It is designed to absorb the heat generated by the readout electronics. In addition, another system is required to ensure a dry-gas environment to run the micro-strip detectors and to prevent them from cooling the regions around the station enclosures.

In designing and costing these systems we heavily used the analogous project developed for D0 RUN IIb upgrade.

The total power dissipated by our electronics will be in range of 500-600 W; including the heat coming from external sources, such as power dumped into the coolant by the circulation pump, the warm dry-gas flowing outside the station enclosures and the losses along the lines, the total power to absorb should not exceed 1 KW.

The coolant distribution system consists of a closed-loop line which starts from an open reservoir, crosses in parallel all the support elements of the stations, enters the chiller/pump unit and finally goes back to the initial reservoir. The pressure in the loop is set by the open reservoir: it starts from 1 Atm and progressively drops until it reaches the minimum value at the input of the chiller pump. The coolant reaches all the station locations through a

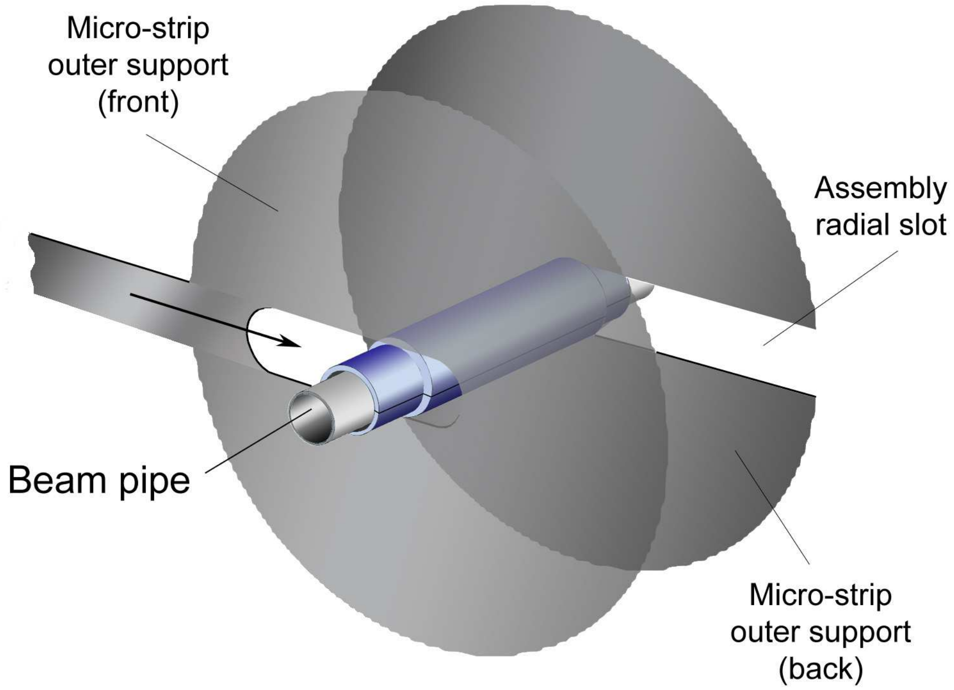

Figure 9.19: Sketch of the beam-pipe interface for micro-strip stations. A tube of very light material, such as Rohacell, is fit into the hole of the outer support disk; a cover with the same shape of the previous disk, but much lighter, is then put on the top of the station structure to create the micro-strip station enclosure.

vacuum-jacketed supply pipe; it is distributed through manifolds to each duct embedded in the station structure and it is recollected on a vacuum-jacketed return pipe. An air-separator tank is inserted on the line just before the chiller. The system is provided with a backup chiller unit and a backup vacuum pump for the air separator.

The dry-gas distribution system employs dry-air at room temperature to purge all the sections of the acceptance cone along the beam axis where the stations are located. These sections can be easily delimited by very light Mylar foils placed on both sides of the external frame carrying the Junction Cards, to which the flex cables are connected. The dry-air enters the sections from the sides and leaves from a narrow annular opening around the beam-pipe. Given the substantial lack of any sealing, important flows of dry-air will be required to guarantee an adequate purge of the sections.

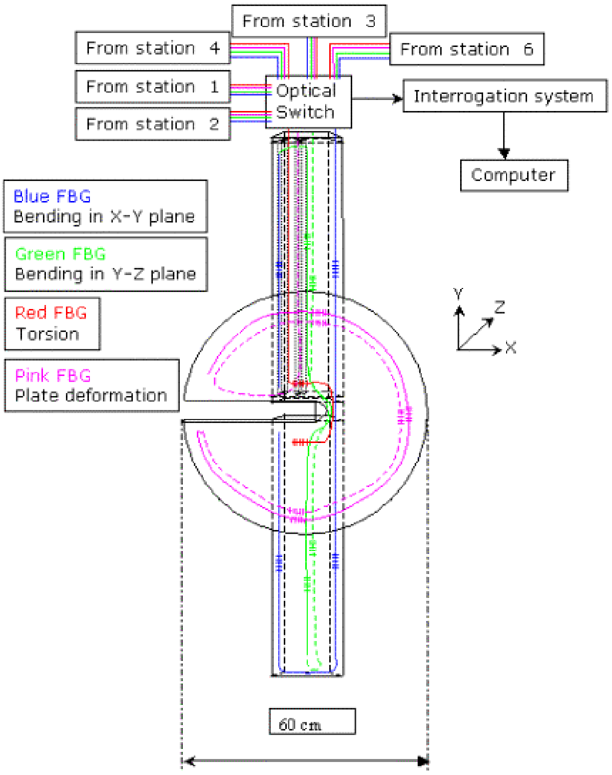

Figure 9.20: Sketch of the FBG positioning monitor system

9.7 R & D

9.7.1 Sensors characterization and irradiation tests

We bought three sensors from CMS (CMS IB2 sensors, $61 \times 116\ mm^2$ active area, 120 μm pitch, 320 μm thickness, $30\mu m$ implant width, $< 100 >$ crystal type) and have recently purchased another sample of ten to study their characteristics and performance. In particular we are interested in understanding the behavior of these sensors when only a small region of them is just going through *type-inversion* process.

This represents a kind of steady situation for the sensors during their operation in BTeV. Indeed, the *type-inversion* will be initially located on the inner edge of the sensors and then, will slowly move toward the opposite edge. Operating the sensor in this situation is particularly critical since strips will cross regions characterized by a continuous change of the doping, from a n type bulk, essentially equal to that of non irradiated sensors, to a p type bulk, passing through a condition where the bulk has no effective doping. The depletion voltage will consequently vary over a wide spectrum of values, reaching a minimum where the *type-inversion* is taking place.

This summer we have irradiated two CMS sensors at the Indiana University cyclotron

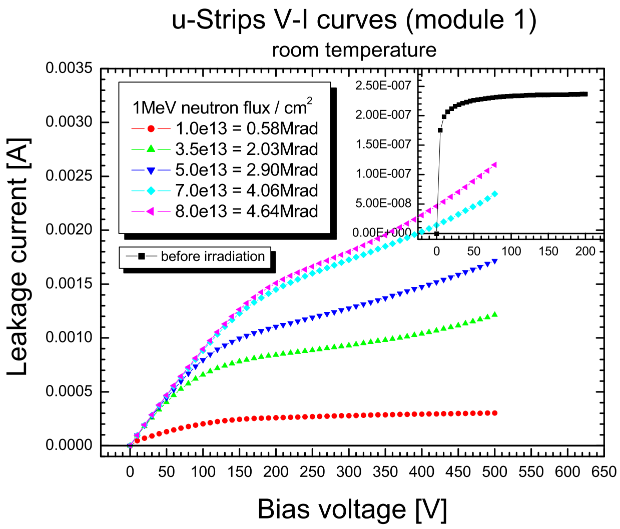

Figure 9.21: V-I curves for different values of the irradiation dose. The histogram in the inset shows the same characteristics curve before the irradiation.

up to a dose of about 5 MRad. This dose corresponds to what we expect to accumulate in BTeV in 10 years of operation.

The sensors were exposed to a 200 MeV proton beam having roughly a gaussian profile with a $\sigma \sim 1\ cm$. The beam was centered on the middle point of one edge of the sensors to reproduce the conditions of the irradiation they will receive in BTeV. In Fig. 9.21 we show the *V-I* curves at different doses for sensor 1. The inset shows the behavior before the irradiation. The measurements were taken at 26 ^0C (room temperature).

Fig. 9.22 compares the V-I characteristics just after the irradiation with that measured the following day, once the sensor was cooled down to $-17\ ^0C$ the leakage current became more than two orders of magnitude lower.

In Fig. 9.23 we quote the measured leakage current as a function of the absorbed dose at a fixed bias voltage, $V_B = 400\ V$, and compare measurements with what we should expect from the theory. The agreement is very good at high temperature; at $-17\ ^0C$ the measured values are a little lower than expectations probably because the actual temperature of the sensors in the refrigerator was lower than that reported by a thermometer which was placed above them but not in direct contact.

Two different setups have been used to fully characterize the sensors before the irradiation tests:

- *A laser test-bench*: an XY micrometric table with a collimated laser source mounted on the Z axis (Nd:YAG laser, $\lambda = 1064\ nm$, $\sim 2\ mm$ absorption length in Silicon).

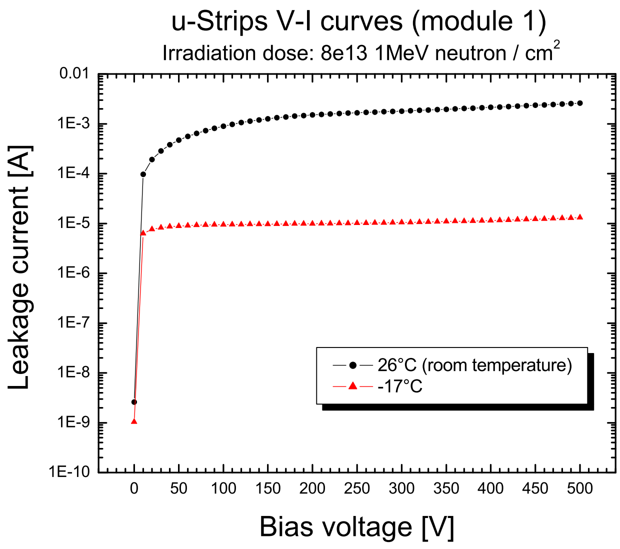

Figure 9.22: The V-I characteristics of the irradiated detector at two temperatures. The black curve at room temperature, $+26\ ^0C$, just minutes after the irradiation, the red line the next day, after cooling the detector down to $-17\ ^0C$.

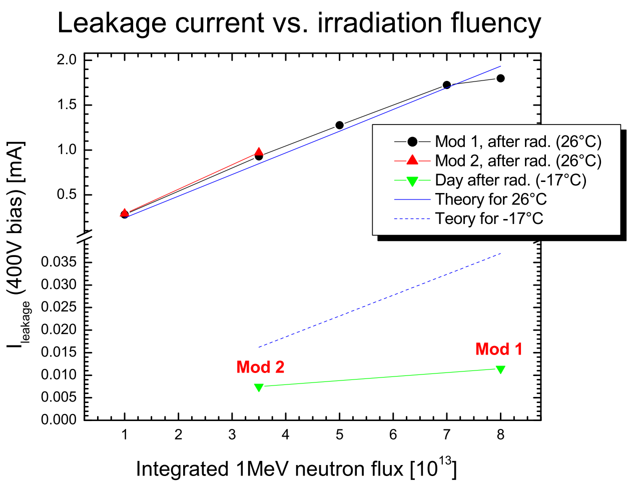

Figure 9.23: Leakage current as a function of the absorbed dose at a fixed bias voltage of $400V$ and for two different temperatures. Theoretical expectations are superimposed as indicated in the figure.

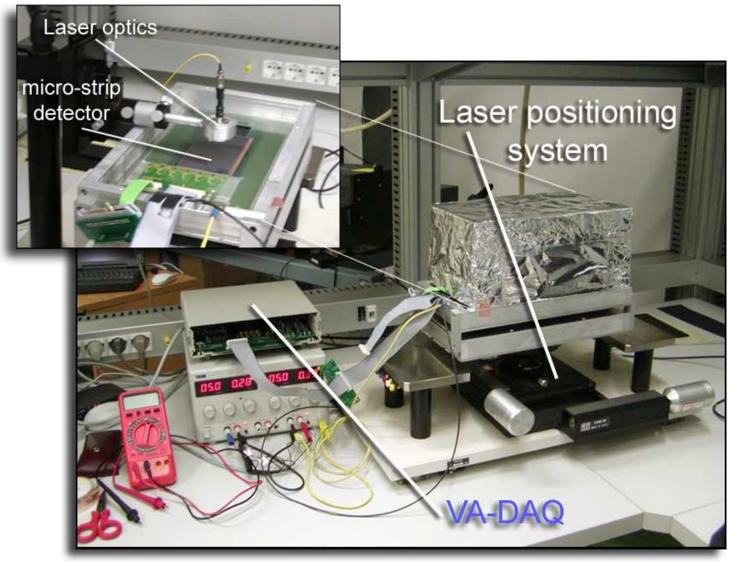

Figure 9.24: The laser test-bench, used to characterize the detectors, as described in the text.

Measurements are carried out with a PC-based commercial data acquisition system, VA-DAQ, manufactured by Integrated Detector & Electronics (IdeAs), Fig. 9.24.

- *A cosmic ray telescope*: a telescope of 6 micro-strip stations, each featuring two 384 channel detectors for X and Y measurements. Measurements are carried out using a custom DAQ (borrowed from the AGILE space-borne experiment). The DAQ is based on a VME system and uses the TAA1 chips, also manufactured by IdeAs, Fig. 9.25.

The readout chip were the VA/TA chips manufactured by IdeAs.

We will comment on some of the measurements we performed. In Fig. 9.26 we show the result of scanning a sensor with the laser source.

The total collected charge by the illuminated strips is reported as a function of the position on the sensor. The gain of all channels was equalized by measuring the MIP peak of cosmic rays with the second setup. The projection of the previous plot along the strips is given in Fig. 9.27.

On this particular sensor, we observe a drop of about 5% in the collected charge from the end of the strip nearest the readout chip to the opposite end.

A final step in the characterization of the detectors has been the analysis of data taken using the irradiated detector (5 MRad).

A setup very similar to the non-irradiated one was used, but the whole system was placed in a thermally controlled environment to keep the temperature constantly down to $-13\ ^0C$ and thus, to slow down the reverse annealing effect. (See Fig. 9.28)

We first accumulated a set of measurements on a non-irradiated detector, in order to set a reference, and then repeated that same set on the irradiated one. The various positions

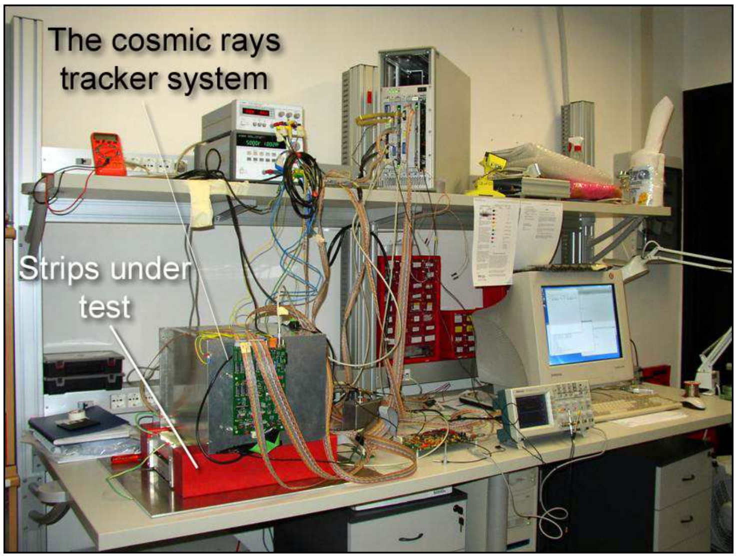

Figure 9.25: The cosmic rays tracker system, used to characterize the detectors, as described in the text.

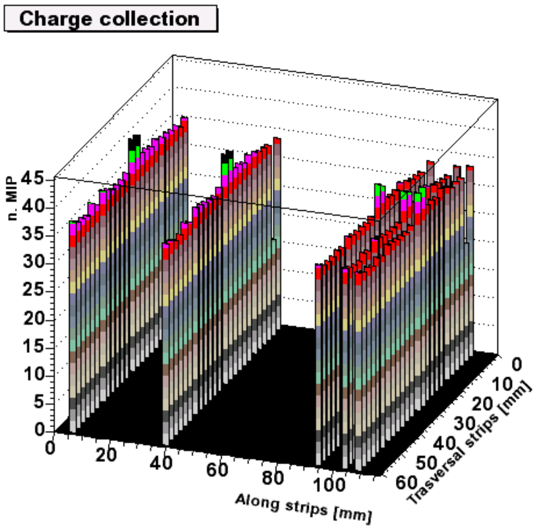

Figure 9.26: Scan of a CMS sensor with the laser source before the irradiation. The total collected charge by the illuminated strips is reported as a function of the position of the laser on the sensor.

of the laser spot are presented in Fig. 9.29, corresponding to a scan of the sensor along a central strip, whose end point was centered in the highest irradiation area of the incoming

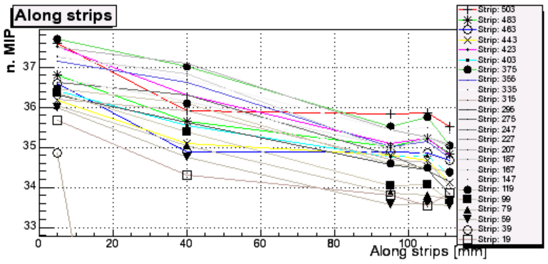

Figure 9.27: Total charge collected as a function of position of the laser source along the strips.

Figure 9.28: The setup used to measure irradiation effects. a) The irradiation target of the Indiana University Cyclotron Facility. b) The aluminum cage lodging the irradiated sensor. c) The hut containing the measurement setup: visible is the laser and the alignment camera. d) The coolant refrigerator, used to maintain the detector at a constant $-13\ ^0C$. e) The rack with the laser control system.

beam. The voltage bias was $160V$ for the non-irradiated detector, above the full depletion, and $350V$ for the irradiated one.

The results are shown in Fig. 9.30a; the blue points, corresponding to the non-irradiated

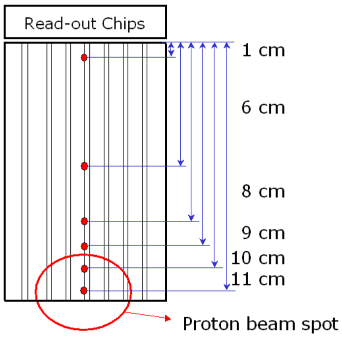

Figure 9.29: Laser spot positions for several charge collection measurement along a strip in the central region. The end point was centered in the highest irradiation area of the incoming beam.

detector, feature a drop in charge collection of about 7% moving away from the readout chip. The red points, corresponding to measurements on the irradiated detector, shows an additional drop in charge collection of about 5%, entirely due to irradiation damage.

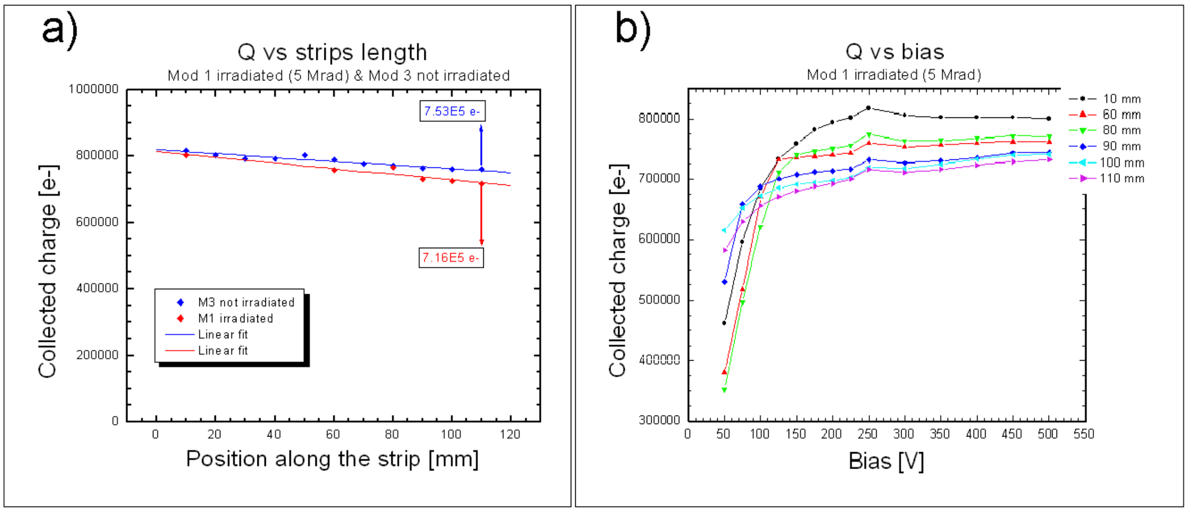

Figure 9.30: Charge collection along the strip. In fig. *a*, showing the collected charge vs. position along strip, the blue points are relative to the non-irradiated detector, red points to the 5 MRad irradiated one. Fig. *b* shows collected charge vs. bias voltage for different positions along the strip.

In Fig. 9.30b, we show the collected charge as a function of the bias-voltage for each position on the irradiated sensor.

These results are very preliminary since we still need a check for systematic effects, but they are certain enough to demonstrate that these sensors can be safely employed in BTeV for at least ten years, without any important degradation of performance. The measured loss in charge collection is limited to a few percent even operating them at a bias-voltage value of 350 V which is well below the breakdown region.

In conclusion, these measurements confirm the excellent performance of the CMS sensors and make us confident that they represent the best choice for BTeV.

9.8 DAQ system for tests and production

9.8.1 Introduction

This section describes the DAQ system we developed for tests and diagnostics during the R&D and the production phase of the Silicon Strip Detectors. The same DAQ system will be used also by other BTeV groups for beam-test activities. During the design and implementation process of the DAQ, several modern computing techniques have been tested and employed; we will certainly make fruitful use of the expertise acquired at this stage for the design of many aspects of the final DAQ system.

This rather sophisticated read-out system has been successfully used to make extensive laboratory tests with the pixel detector and is installed and operational at the test beam (we remind readers that the digital read-out chip is the same for both pixels and silicon strips).

9.8.2 Description

The DAQ design is based on the PCI bus protocol, a widespread standard in the computing industry, which offers several benefits, one being its relatively low cost and another the large amount of available core software to develop custom applications. The digital part of the silicon micro-strip detector front-end is designed to be practically the same as that of the pixel detector, thereby allowing for a common read-out scheme for these two detectors.

In their final configurations, both the pixel and the silicon strip detectors will be read out in a sparsified mode, with no external trigger to drive the incoming data flux. Any system devised to read the data from of these detectors must be able to cope with two different clocks, the one used by the read-out chips and the one used by the read-out processes on the host computer (usually the CPU clock). The different pace of these clocks, along with possible rate fluctuations due to varying beam intensities, can create bottlenecks in the transition of data from the detectors to the final mass storage on the host computer. This problem has been kept the central focus of our design of the DAQ, in order to allow the system to operate in an efficient and lossless way under a continuous sustained data rate.

In our design each detector is connected to a PMC (Programmable Mezzanine Card) [7] featuring a suitably micro-programmed FPGA (Xilinx Virtex II) in charge of taking care of formatting and time-stamping the data produced by the detector. The PMC is then connected to a PTA (PCI Test Adapter) board [8] featuring an Altera FPGA (for data-flow and initialization control) along with two 1 Mb memories. Several PTA boards are lodged together on a PCI bus extender and finally connected to a host DAQ PC (Fig. 9.31 shows a schematic representation of the data flow).

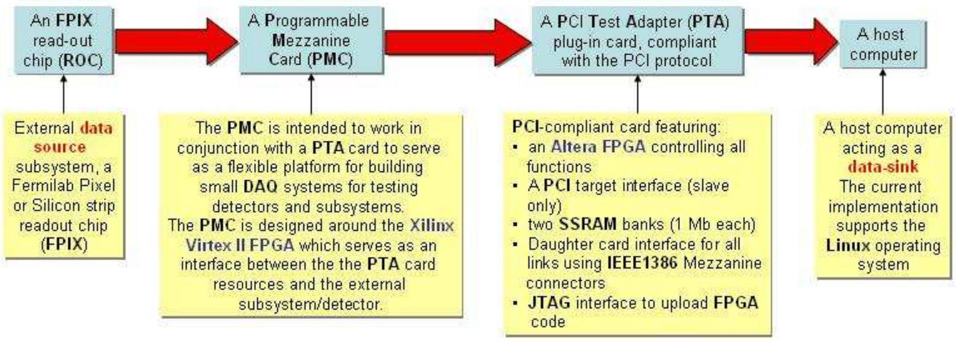

Figure 9.31: Schematic representation of the data flow from the detectors to the mass-storage, through the PMC mezzanine and the PCI cards.

Each time a strip generates data above threshold, the address, along with time-stamp information (and pulse height in the case of pixels), suitably formatted, are sent to a PTA board to be stored in one of its two local memories. The FPGA's are programmed to handle the swapping between these two local memories and the synchronization with the external read-out process (running on the host DAQ PC) to smoothly handle a sustained data rate, adequate to the beam test requirements.

The principle of operation of this read-out scheme is the following (Fig. 9.32):

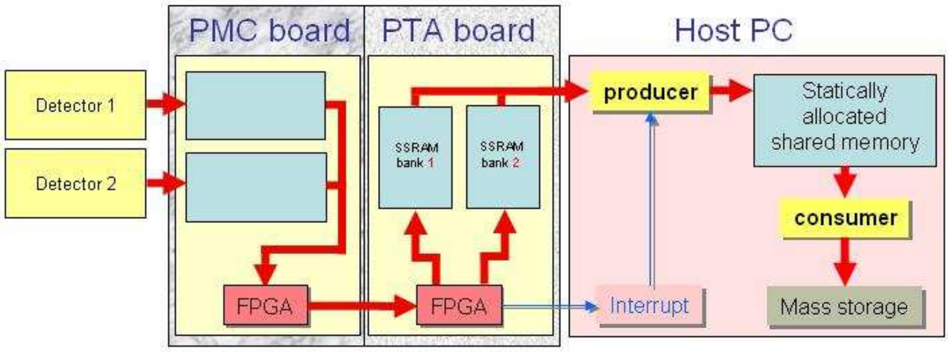

Figure 9.32: Schematic representation of the main components of the read-out chain. Producer and consumer, described in text, are the processes responsible, respectively, for reading out the FPIX chip into the shared memory and from there to the host computer.

- data are received from a detector by the corresponding PMC card and fed into one of the two internal memories of its sibling PTA board.

- as soon as any memory in the system is full, all PTA boards are synchronously commanded to swap the data-flow to their memories: those used so far are frozen and immediately made available for read-out by the host computer, while the others are used to continue reading events from the detectors without any data loss. The memories on the PTA boards, therefore, act as a first level compensation buffer to account for rate fluctuations (Fig. 9.32)

- events are then fed, by a producer process, to the host computer on a statically allocated shared memory, implemented as circular buffer (this is accomplished by a specialized process). This shared memory, usually much larger than the memory banks on the PTA boards, by a factor 50 at least, acts as a second level compensation buffer. While the PTA memories compensate rate fluctuation for an individual detector, the global shared memory does the job for all the detectors together.

- data are then continuously flushed from this memory to mass storage by a *consumer* process, which builds events on the fly and makes them persistent.

A crucial aspect of this design is to keep the event-builder algorithm as simple and efficient as possible. An event, defined as *the set of all hits marked by the same time-stamp*, is in general spread out over several PTA boards which can in principle receive data at different rates. In absence of a specifically defined strategy to synchronize the flushing of these memories, this sparse read-out makes the event builder extremely cumbersome and inefficient, since hits of an event will be located at progressively more distant locations in the shared memory. The event builder sorting algorithm will then need to explore larger and larger sections of the memory in order to assemble all the hits of an event. Moreover, should the distance between the locations of all hits of an event become larger than the available shared memory we could start loosing events, since the pointer in the circular buffer will be reset and old locations will be overwritten.

We have therefore designed the mechanism of memory-swap synchronization to restrict the components of an event to be contained in a limited amount of memory, taking advantage of our ability to program the FPGA to generate interrupt signals. Interrupts are used to alert the read-out process that a memory on one of the PTA cards is full, in order to force a swap of all the memories in the other cooperating PTA boards (Fig. 9.33)

This is an event-driven scheme: data are collected as soon as they are produced by a detector, and no burden is placed on the DAQ software to generate signals to start and synchronize a read-out chain. This is important, since it allows testing the full functionality of the detector in an environment similar to the one envisaged for the final data taking, where no trigger is used to read out events.

Several components of this read-out have already been implemented, on a Linux platform:

- the PTA board and the microprogramming of the FPGA to send and generate control signals and interrupts. This stage required acquiring considerable expertise in using the Quartus software, used to generate code for the Altera FPGA.

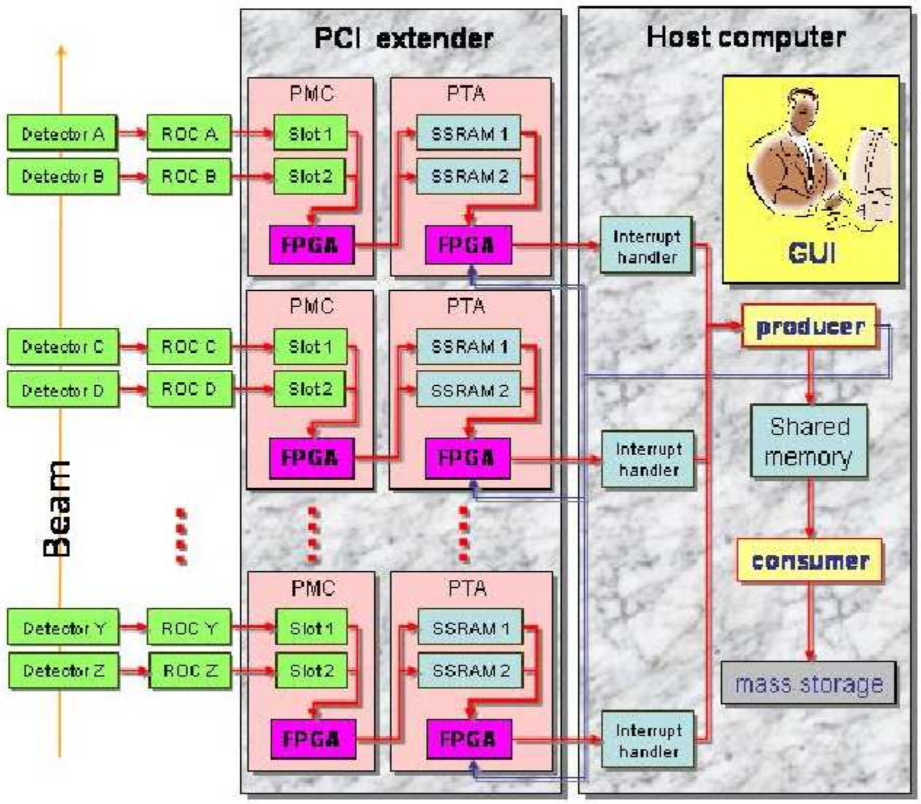

Figure 9.33: Schematic representation of a complete test-beam setup.

- an abstract interface to the underlying PCI driver; we started using a commercially, license-bound PCI driver by Jungo, and later developed our own version. The abstract interface allows the DAQ code to be formally and factually independent of the particular choice of driver, enhancing its widespread portability.

- the interrupt-handler processes, in charge of starting the read-out of a PCI memory, synchronizing the memory-swap and the read-out of all other boards and transferring data to the external shared memory.

- the read-out process, owner of the shared memory and responsible for synchronizing with the consumer process to event-build the outcoming data and flush to a storage media. The event builder also has been implemented as a virtual class, in order to allow for different read-out schema at run-time and thus for different kinds of detectors to be read-out, greatly enhancing the potential use of this read-out DAQ.

- a package for message transmission among cooperating processes (based on the native Linux IPC system V protocol)

- a complete graphical user interface to allow users to drive the read-out process, both in a test-bench environment and in a more complex test-beam environment.
- a set of diagnostic and monitoring tools: these gather data from the DAQ by sockets on the network, where the read-out processes make information available for remote processes to use. This allows people to monitor all aspects of the test-beam progress from remote institutions in a very efficient way, without placing any computation burden on the CPU which is driving the read-out.

9.9 Silicon Strip Detector Production Plan

9.9.1 Introduction

This section describes how we plan to organize the production of all the micro-strip detectors once the final design is defined and proven to satisfy all the requirements by means of tests of suitable prototypes, and before the installation at C0.

9.9.2 Logical Organization of the Production

The Production will start once the plane and station prototypes are tested and approved. We expect this to happen in the first half of fiscal year 2009.

The main deliverables of the micro-strip production are:

- the Half-Planes, which will be mounted around the beam pipe during the installation at C0;
- the External Support Mechanics, which will hold the stations in the right position along the beam pipe;
- the Cooling System, which will feed the cooling ducts embedded in the plane supports;
- the External Cables, which will carry signals, controls and power supplies in the region outside the acceptance cone of the apparatus;
- the Low & High Voltage Power Supplies;
- the Junction Card;
- the Data Combiner Boards.

All these deliverables are produced in a completely independent and parallel way, since none of them require progress in any of the other areas. It is clear that as soon as the deliverables become available during the production process they can be installed at C0 without waiting for the completion of the production. In the following sections we describe the organization of the production of each deliverable. A database will keep track of all the production steps of the deliverables. It will contain all the test records and shipping logs and will be accessible on the web. Its structure will be defined on the basis of the experience gained building the prototypes.

9.9.3 Half-Plane Production

The Half-Plane Production consists of the production of the ladders and the plane supports, which can proceed in parallel, followed by the assembly of the ladders on the supports. Several tests during the production process require test stands equipped with DAQ to readout the FE chips. These test are required to check the full functionality of the bare FE-chips, the Hybrids and the ladders before and after the assembly on the supports.

9.9.3.1 Ladder Production

The main components of a ladder are

- **Sensors**
- **Readout Chips**
- **Hybrids**
- **Flex Cables**
- **Mechanical Structure**

They will be provided by external companies and sent to SiDet for acceptance tests. Once accepted, the parts will be used to assemble the ladders.

- **Sensors**

  Responsible Institutes: **Colorado U., INFN-Milano**

  The main checks we plan to execute on sensors are to monitor their production process and to certify the radiation tolerance. They will be performed on 5-10% only of the total wafers. They include measurements of the test structures inserted on each wafer and a complete characterization of a sensor on the same wafer, strip by strip, before and after a high irradiation dose with protons. We think that once these checks have been performed, we can safely rely on the measurement data provided by the vendor for the remaining detectors. In any case, all sensors will be I-V and C-V characterized to be accepted. A probe station and a clean room will be required for this kind of measurements. The test and shipment records of all the wafers will be stored in the database.

- **Readout Chips**

  Responsible Institutes: **Fermilab, INFN Milano, INFN Pavia**

  The readout chips will be delivered to us on 8 inch wafers. All the wafers will be probed at Fermilab, Milano and Pavia before further assembly. One or more wafers will be diced up so that we can carry out characterization tests to check on functionalities and performance. A probe station and a test stand with DAQ are necessary for these tests. The known good dyes on each wafer will be marked. The test records and shipment records of all the wafers will be stored in the database.

- **Hybrids**

  Responsible Institute: **Fermilab**

  Hybrid Production requires the preliminary production of the micro-strip readout chips, which will then be assembled on the hybrid boards together with all the other required electronics, such as by-pass capacitors and temperature monitors. The readout ICs will be selected by us before being sent to the vendor for the hybrid production. Once delivered at SiDet, Hybrids will be tested for acceptance. For these tests we plan to develop a test stand, which automatically checks the functionality and performance of all the channels. The test records, shipment records and reference to the used readout chips of all the hybrids will be stored in the database. Also in this case, a probe station and a clean room are required. We will later fix the tolerance in terms of percentage of channels not properly working on a single Hybrid. It will largely depend on the quality of the sensors, meaning that the higher the sensor quality, the lower the tolerance on Hybrids. Recent CMS experience with similar Hamamatsu sensors is very promising to this extent, since they measured an effective 100% yield of working strips.

- **Flex Cables**

  Responsible Institute: **Fermilab**

  Flex Cables will be supplied by a vendor with the required connectors mounted on both ends and with certified characteristics in terms of impedance between lines and resistance. We plan to execute some checks of the characteristics on 10% only of cables for each delivery. The test records and shipment records of all the flex cables will be stored in the database.

- **Mechanical Structure**

  Responsible Institutes: **Colorado U., INFN Milano**

  The mechanical structure of the ladders will be provided by the same company producing all the carbon-fiber supports of the micro-strip system, with a certified degree of planarity to avoid any torsion effect during the ladder assembly. We do not plan to execute any check on these structures, but an accurate visual inspection.

- **Ladder Assembly**

  Responsible Institutes: **Colorado U., Fermilab, INFN Milano**

  Once a sufficient number of components are received and accepted, the ladder assembly process can begin. We plan to assemble 50% of the ladders at SiDet and have the other 50% assembled by an Italian specialized company. How to tune the minimal amount of parts necessary to start an assembly run will be decided later on, when enough experience has been gained in this job. The assembly will require the development of special mounting jigs to ensure the alignment of strips within few microns and special bonding tools to wire-bond sensors and FE chips. The micro-strip alignment should be referred to some reference marks placed on the hybrid circuits (at least two per hybrid), which are used to position the hybrids themselves and serve as general reference for any successive alignment of the ladder. Assembled ladders will be extensively tested both in pulse mode and with laser at SiDet using a test stand with DAQ to readout all the channels. We will define a ladder acceptance procedure, which will also specify the maximum tolerable amount of broken channels per ladder. The test records of all the ladders and reference to the used hybrids, flex cables and sensors will be stored in the database.

9.9.3.2 Plane Support Production

Responsible Institutes: **Colorado U., INFN Milano**

Plane Supports will be provided by the same company producing all the carbon-fiber supports of the micro-strip system, with the required certified accuracy. They will be tested at SiDet by measuring the relative accuracy when two halves are joined together to form a plane support and when three plane supports are stacked to form a station. These tests will be performed by measuring the relative positions of the reference marks present on each half of the plane supports by means of a high precision XYZ table with a microscope on the Z-axis. Plane Supports will be tested also to check the cooling duct embedded in the structure. It has to be leak checked and pressure tested. The test records and shipment records of all the plane supports will be stored in the database.

9.9.3.3 Half-Plane Assembly

Responsible Institutes: **Colorado U., Fermilab, INFN Milano**

When two ladders and one half-plane structure are tested and declared accepted, a Half-Plane can be assembled. The assembly requires the alignment of the reference marks on the ladders with those on the half-plane structure. It will be performed at SiDet on a high precision XYZ table with a microscope on the Z-axis. Once two half-planes are assembled, they will be joined together to form a complete detector plane and will be tested, using a test stand equipped with a DAQ, in pulse mode and with laser in the final plane configuration with the proper cooling system. Temperature in the most critical spots will be monitored to check the efficiency of the cooling system. Structure deformations will be monitored as well on a XYZ table. The test records of all the half-planes and reference to the used ladders and plane supports will be stored in the database.

9.9.3.4 Test Stands

Responsible Institutes: **Fermilab**

To carry out full electronic test of the readout chips, the hybrids and the ladders, test stands will be set up at INFN Milano, INFN Pavia and SiDet. It is assumed that the test stands will be common to all sites, sharing the same hardware and software platform. The test stands will use the DAQ developed by FNAL and Milano for the pixel test beam.

9.9.4 External Support Mechanics

Responsible Institute: **INFN Milano**

We have not yet decided if the External Supports for micro-strip Stations will be integrated into the structure of the nearby Straws or if they will be independent structures just for holding the stations in the proper positions around the beam-pipe. The solution that will minimize the amount of material will be chosen. In the present base-line design they are independent carbon-fiber supports, which will be provided and certified by the same company producing all the supports of the micro-strip system. Once delivered at SiDet, they will be measured on an XYZ table to check for the accuracy of the main support points. The embedded pipes, which, together with the cooling ducts in the plane structures, form the cooling circuit, will be leak checked and pressure tested. The test records and shipment records of all the external supports will be stored in the database

9.9.5 Cooling System

Responsible Institutes: **INFN Milano, INFN Pavia**

The cooling system, excluding the ducts embedded into the support structures, consists of the chilling fluid units, the station enclosures and all the instruments and probes to monitor temperature and coolant flows. The station enclosures provide the proper dry-gas atmosphere around the detectors in each station. The chilling fluid units produce the fluid to cool the electronics and the gas flowing in the enclosures. The major components of the system will be assembled by the Pavia group and transported to FNAL for the final assembly in C0. During the production in Pavia, all the components will be tested before the transport to FNAL. The test records and shipment records of all the parts of the cooling system will be stored in the data-base. The prototype cooling system developed during the R&D phase will be used to test the ladders and the planes during their production at SiDet.

9.9.6 External Cables

Responsible Institute: **Fermilab**

The Fermilab group will be responsible for the procurement and testing of the external cables with relative connectors.

9.9.7 Low & High Voltage Power Supplies

Responsible Institute: **Colorado U.**

Both low and high voltage power supplies have to be floating. We assume we will buy commercially available Power Supply Systems.

9.9.8 Junction Cards

Responsible Institute: **Fermilab**

The Junction Card repeats the signals between the readout chips and the Data Combiner Board and distributes the power to the chips and the sensors. These boards will be developed, tested and produced by the Fermilab CD group.

9.9.9 Data Combiner Boards

Responsible Institute: **Fermilab**

The micro-strip Data Combiner Boards will be used to assemble the data from the micro-strip ladders and sort them according to time-stamps. They are exactly the same as the pixel DCBs. One data combiner board will be needed per micro-strip half-station. Procurement, assembly, testing and installation of these boards will be done by the Fermilab group in conjunction with the production of pixel DCBs.

9.10 Installation, Integration and Testing Plans (at C0) for the micro-strip Forward Tracker

9.10.1 Introduction

This is a general description of the Installation, Integration and Testing Plans for the micro-strip Forward Tracker. As explained in the Production section, once micro-strip half planes are assembled and checked at SiDet, they are ready for the final installation at C0. It is worth noting that micro-strip half planes are already internally aligned to ensure a sufficient relative precision when combined to form a plane and even a station. This means that the most crucial operation during the installation is to position the first plane, on the basis of which the station is built. Micro-strip installation should be coordinated with that of straw tubes since micro-strips can be installed only once the straws of the same station are already installed. The installation of the full micro-strip system consists of seven almost identical procedures of single station installation. We estimate that each installation will take about one week, including a full check of all the station functionality and performance. Note that in real time, this will take roughly one calendar year, as we plan to install stations as their parts become available and as opportunities exist to gain access to the experimental hall for extended periods. The first station should be installed in early 2009. In the present baseline design, we foresee an independent support for each micro-strip station, but are trying to investigate the possibility to directly integrate the micro-strip support in the straw structure of the same station.

9.10.2 Summary of Testing Prior to Moving to C0

All the possible tests and adjustments will be done at SiDet before transportation to C0. Half planes are completely checked for functionality and performance using the final DAQ, if ready, or the PCI-based version developed for the pixel test beam. Even the mechanical structure of the stations have been designed to minimize the alignment operations during the final installation. Half planes can be simply combined to form a plane and planes can be stacked to form a station in such a way that the relative internal alignment within the required precision is guaranteed. Only checks with optical instruments are necessary to verify that nothing unexpected happened.

9.10.3 Transportation of Level 2 Subproject Elements to C0

9.10.3.1 Equipment Required

Special boxes with shock absorbers will be prepared for half plane transportation to C0. A small truck or even a car will be enough for this transportation.

9.10.3.2 Special Handling

Particular attention should be paid during the transportation to avoid shocks that could destroy the internal alignment. The material is extremely fragile.

9.10.3.3 Personnel Required

If possible, our micro-strip group will personally take care of the transportation to C0.

9.10.3.4 Time Required

We foresee seven distinct transportations to C0, one for each station installation. We do not intend to move any component from SiDet if not necessary. Each transportation will not require more than four hours.

9.10.4 Installation of Level 2 Subproject Elements at C0

9.10.4.1 Installation Steps

The installation sequence for a single station consists of the following steps:

- Installation of the station support and all the connections to power supplies
- cooling system, and DAQ & control
- Installation of the first plane
- Installation of the second plane
- Installation of the third plane
- Installation of the station enclosure

9.10.4.2 Equipment Required

High accuracy survey equipment is required to measure the position of the fiducials on the station support and on the half plane structures, and to align them with respect to the external fiducials.

9.10.4.3 Special Handling Issues

All the components of the system are extremely fragile and should be assembled in a pretty clean environment.

9.10.4.4 Potential Impact on Other Level 2 Subproject Elements

Micro-strip installation is strictly correlated with that of the straw tubes. We plan to install micro-strips only once the straw tubes of the same station are already installed. Presumably both micro-strips and straws will share the same external mechanical structure, which can slide into the final position on high precision rails.

9.10.4.5 Personnel Required

The Micro-strip group will take care of the installation process. In addition, we need an expert to properly setup and check the links to the monitor/control system. Also we need the assistance of a survey crew during the installation to measure the position of the fiducials.

9.10.4.6 Time Required

We estimate that three days are enough to physically install one station and to carry out the obvious checks for continuity of the connections. Presumably the survey crew would need one day more to setup all the instruments. As stated in the introduction, it is worth noting that the real duration of the complete installation would be roughly one calendar year.

9.10.5 Testing at C0

During the station assembly we plan to execute only some tests to check for the continuity of all the connections; cooling lines, in particular, have to be leak checked and pressure tested. Once the station is completely installed and sealed inside its enclosure, it can be turned on and run. Cooling circuit parameters, such as flows and temperatures, will be continuously monitored while the system is approaching its stationary regime. An extensive check of all the functionality and performance of the station detectors will be carried out by electrically pulsing the FE chips and reading it out through the final DAQ system. Particular care will be devoted to establish a clean grounding of the system. Once the station is fully checked, it will be ready for the final positioning. The station will be smoothly rolled into the final position together with the straw chambers. A final survey of all the fiducials on the station support will be done before to declare the station *installed & operational*.

9.10.5.1 Stand-Alone Subsystem Testing

The station will be tested as a stand-alone subsystem by electrically pulsing the FE chips. The major requirements to carry out this test are described in the following subsections.

- **Mechanical:**

  We will take care of the installation, debugging and running of all the cooling system needed for micro-strip stations. We will prepare it well before the installation of the first station. We require that the external water circuits to dump the heat of the main chiller units, be installed and operational. Piping from the remote chiller units to the distribution panels in the experimental hall should be installed and leak and pressure checked. Obviously, the mechanical structure to roll both the micro-strip and straw stations into the final position, should be ready and calibrated.

- **Electrical/Electronics:**

  The final quiet AC mains power should be installed and tested. The power supply systems should be operational both for high and low voltages. The Data Combiner Boards should be installed and fully checked for readout. The final bunch crossing clock should be available, or at least a fake one should be generated. All the alarms and monitors should be in place and operational (readable).

- **Software:**

  The final DAQ should be ready and operational, or at least a part of that, which would allow us to read out the system through our Data Combiner Boards. It should accept and process in `OR` mode a variety of calibration triggers synchronized with the main bunch crossing frequency. Event builders should be ready for each subsystem. We will take care of all the specific software development to test and calibrate our system.

- **Personnel Required:**

The micro-strip group will take care of all these stand-alone tests. In addition, we need the assistance of a DAQ expert and a monitor/control expert for the duration of these tests.

- **Time Required:**

  We plan to execute all these tests on each station in about four days.

9.10.5.2 Multiple Subsystem Testing

As described above, our *stand alone* tests will also be integration tests with the DAQ and other systems, such as the trigger and the monitor/control system. We will continue to refine this kind of test during all the micro-strip installation period.

- **Software:**

  We plan to refine and update our software as required by the debugging process.

- **Personnel Required:**

  Certainly the micro-strip group and the availability of the DAQ and trigger experts.

- **Time Required:**

  The duration of these multiple subsystem tests will last during the entire installation period which should be roughly one year.

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