March 8, 1999

Silicon Subsystem Report

February 1999

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are currently within allocated amounts. The cost of the prototype program for the support frame is now known to be about $40K plus materials. The materials cost is still somewhat uncertain, since the final carbon-fiber material has not been selected. We expect to make this selection in March. Italy has agreed to purchase graphite-fiber honeycomb for the prototype. The first design review of the FE-D prototype was held successfully and submission for fabrication is projected for April. There have been no significant changes in the last month in the schedule for the remainder of the system. In general, the mechanics, sensors, hybrids and module activities are on or close to on the baseline schedule except for those activities tied directly to the delivery of the rad-hard IC prototypes. The critical rad-hard IC milestone (vendor selection) is currently projected to be delayed by 5.5 months compared to the baseline. This implies a 3-4 month delay in the pixel baseline construction review. The Technical Assistance Agreements(TAAs) between Honeywell and Marseille and Bonn are still held up and Honeywell is working to resolve this with the State Department and DOD. The projected delays assume this situation will be favorably resolved by about mid-April. We are attempting to add additional IC design manpower to reduce or eliminate the delays but realistically the feasibility of doing so will only be known by about the end of April.

1.1.2 Silicon Strip System

Costs are within allocated limits. There are further delays in the submission of the ABC and ABCD beyond those reported last month. There are no fundamental problems with the ABC and the additional delays are caused by the limited manpower and the need to complete detailed, and duplicate, simulations to ensure a good submission. The additional delay in submitting the ABCD has been caused by lack of complete understanding of the stability of existing prototypes when connected to detectors. This was reviewed in mid-February and considerable insight was obtained from measurements and simulations. Resubmission reviews of the ABC and ABCD are scheduled for March 23 and 24, respectively. The hybrid schedule is linked to the schedules for the ABC and ABCD and thus additional delays are now expected.

1.1.3 ReadOut Driver System

Costs are within allocated limits. The combined approach agreed to in November has failed. There exist largely "philosophical" differences between the DSP-based approach from Irvine and the FPGA approach from Wisconsin and the two design groups have been unable to converge upon a single design approach. An ATLAS review, chaired by A. Seiden, with broad representation from the pixel and SCT groups, and from outside these groups, will take place on March 25-26 to review the approaches and make a selection.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (D. Bintinger, M. Gilchriese)

Milestones	Baseline	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	1-Feb-99	Complete
Select materials for frame proto.	15-Mar-99	15-Mar-99	On Schedule
Complete fab 1st prototype ring	1-Apr-99	1-Apr-99	On Schedule
Complete frame Phase I	1-Jul-99	1-Jul-99	On Schedule
Complete fab 1st prototype disk	1-Jul-99	1-Jul-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule
Complete frame Phase II	1-Oct-99	1-Oct-99	On Schedule
Complete frame Phase III	1-Feb-00	1-Feb-00	On Schedule

Milestones for the frame prototype activities have been added this month.

LBNL

1.1.1.1.1 Design

The disk support ring prototype concept was selected. Completion of design details and FEA calculations on the prototype ring continue. Drawings were sent to ESLI, San Diego in preparation for fabrication. Preliminary layout drawings of services (electrical and cooling) were done by LBNL in preparation for testing service routings and system assembly on a full scale five disk model.

A fabrication vendor, ALLCOMP, Inc near Los Angeles, was selected as the fabrication vendor for the support frame prototype. A detailed, three-phase program was defined in a statement of work and a bid requested and supplied by ALLCOMP. Phase I is materials evaluation. Phase II is prototype panel and joint fabrication. Phase III is the fabrication of a complete prototype of the end frame section. A purchase order is expected to be in place by the end of March through LBNL. The design of the support frame was advanced by

Hytec, Inc. Finite element studies were done to compare different carbon-fiber materials for the facesheets of the panels making up the frame and for different conditions of stiffening the ends of the structure. We expect to select a carbon-fiber material by mid-March. Graphite-honeycomb fiber from YLA Cellular Products will be ordered for the prototype and paid for by Italy.

1.1.1.1.2 Development and Prototypes

TV Holography test results on out-of-plane distortion vs. temperature for the mockups of aluminum tube sector 4 were received from Hytec, Inc. The test mockups were fabricated with stiffer core-to-facing adhesives (including a low temperature cure cyanate ester adhesive) to investigate why the original Aluminum tube sector 4 displayed excessive distortion vs. temperature change. The test results showed the mockups had much lower distortion (approximately 0.1 microns per degree C) than the original construction of Aluminum tube sector 4 (approximately 2.0 to 5.0 microns per degree C). Aluminum tube sector 4 was rebuilt based on the test results with the cyanate ester adhesive and with a stiffer core material. This core material was reticulated vitreous carbon foam that had been densified by carbon vapor deposition.

Sector 9 was received from ESLI, San Diego. This sector has a flattened glassy carbon coolant tube to increase thermal conductivity between facings and coolant tube. Thermal tests are underway.

Aluminum tube sector 3 which was irradiated to 22.3 MRads at the LBNL cobalt 60 source was tested by Hytec, Inc. using TV Holography for distortion vs. temperature and vibration modes after the irradiation. The out-of-plane distortion per degree C after irradiation was approximately 2 microns per degree C, similar to distortion before irradiation. The peak vibration frequency after irradiation was 230 Hertz vs. 220 Hertz before irradiation. Thus the mechanical performance of aluminum tube sector 3 is quantitatively the same as before irradiation. This result combined with the similar thermal performance before and after irradiation reported last month indicates that the aluminum tube sector prototypes can withstand the expected radiation dose for ten years of ATLAS operation.

Tests of shear moduli continued on silicon module-to-sector structure adhesives. These tests included shear modulus testing of UV cure epoxies to be used for the possible tacking of silicon modules to the support structures.

1.1.1.1.3 Disk Production

No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Current	Status
*Start market survey	2-Nov-98	1-Dec-98	Completed

*2nd prototype PDR	1-Dec-98	1-Dec-98	Completed
*Complete market survey	5-Mar-99	12-Feb-99	Completed
*2nd prototype FDR	29-Mar-99	29-Mar-99	On schedule
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99	On schedule
*Compl. 2nd prototype design	27-Apr-99	27-Apr-99	On schedule
*Compl. Fab of 2nd prototypes	21-Sep-99	30-Aug-99	On schedule

1.1.1.2.1 Design

No activity.

1.1.1.2.2 Development and Prototypes

The Market Survey for the Second Prototypes was concluded, and the Price Enquiry was initiated with the 4 qualified vendors. The price enquiry concerns 250 micron devices only as detailed design of the (200 micron) B-layer sensors was deferred until physics simulation of a bricked B-layer is complete. This staging of the design is not expected to impact the milestones for project completion since the B-layer will be constructed last. The Second Prototype wafers will include 3 Tiles, each of which examines a slightly different bias grid structure in order that the design may be optimized for yield. GDS-2 files for the wafers were made. Characterization of sensors utilizing “modified p-spray” indicated improved radiation hardness, so the plan to include standard and modified p-spray as well as normal and oxygen-diffused silicon in the Second Prototype baseline was ratified.

At New Mexico, capacitance measurements of First Prototype sensors were finalized and a draft note was produced. The DAQ test stand was interfaced with x-y linear positioning stages so that automatic scanning of pixel arrays can be handled through LabVIEW.

1.1.1.2.3 Production

No activity.

1.1.1.3 Pixel Electronics (K. Einsweiler)

Milestones	Baseline	Current	Status
Compl. Design HSOI test die	16-Apr-98	1-Nov-98	Completed
Compl. Fab HSOI test die	26-Aug-98	31-Mar-99	Delayed
Compl. Design DMILL test device	15-Dec-98	15-Dec-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known
1st design review of DMILL proto	25-Jan-99	23-Feb-99	Completed
*FDR DMILL 1st prototype	25-Jan-99		May not occur
*Compl. Design DMILL 1st proto.	26-Feb-99	15-Apr-99	Delayed
Compl. Fab DMILL test device	30-Apr-99	30-Apr-99	On schedule
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule

Compl. Eval. DMILL test device	1-Jul-99	1-Jul-99	On schedule
Compl. Eval. HSOI test die	1-Jul-99	1-Jul-99	On schedule
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Oct-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	15-Aug-99	Delayed
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	15-Feb-00	Delayed
*Compl eval. DMILL prototype	9-Dec-99	1-Jun-00	Delayed
*Compl eval HSOI prototype	15-Feb-00	1-Jun-00	Delayed
*Review design approach	19-Jan-00	15-Jun-00	Delayed
*Select rad-hard vendor	29-Jan-00	15-Jul-00	Delayed

Additional milestones have been added this month to better track progress. We are currently projecting a 5.5 month delay in selection of a rad-hard vendor. This in turn implies a delay of about 3-4 months in the baseline construction review. We are working to shorten these delays and restore the schedule but a realistic assessment of the possibility to do so will only be ready by the end of April.

LBNL

1.1.1.3.1 Design

Our highest priority remains the DMILL front-end chip submission (“FE-D”). We spent several days in Bonn in mid-Feb to go over all aspects of the design, and begin to integrate the different portions of the layout. This went well, but further work remains. We also had a full-day first design review of this submission on Feb. 23 at CERN, with a committee of three engineers, joined by the ATLAS FE Electronics Coordinator. The review went well, but we have yet to receive the follow-up comments from the reviewers. We continue to progress on the verification of our deliverables for this submission. A major problem has developed since the lead engineer on this effort at LBL gave his notice at the end of Feb. He is presently working to finish up contributions only he can make, and we are transferring his responsibilities to another senior engineer (Gerrit Meddler) who is presently largely occupied with the SCT ABC submission. We hope to lose no more than a few weeks out of our schedule due to this major disruption, since most of the difficult work had been completed. However, it remains to be seen whether as we complete the simulation and verification process, we run into additional unforeseen problems that could be more difficult to solve in the absence of the original designer. We believe we are still on schedule for submission by April 15, but many small details could intervene to delay that by some weeks.

The principle effort at the moment on FE-D is to complete the last few buffer sizing and pitch matching issues in the layout, and to improve the quality of the Verilog simulation. After this is complete (about 1 week), we will be able to run complete simulations of the column pair and end of column logic with fair accuracy in Verilog, and good accuracy using SPICE. We are also preparing simulations of the entire digital portion of the chip. We will concentrate on making some specialized simulations of these parts using SPICE, while the Bonn group will do the overall Verilog simulations. We are producing annotated Verilog libraries with the typical pre-rad, fast-fast pre-rad, and slow-slow post-rad models in order to study the performance under process variations. The “fast” and “slow” above refer to the performance of the NMOS and PMOS transistors in the process.

1.1.1.3.2 Development and Prototypes

The Honeywell SOI multi-project submission which we made in Nov. 98 is also approaching completion. We expect to receive 30 pieces by the end of March. These test devices include complete front-end designs (improved over that of the FE-B chips), and will allow us to make a detailed evaluation of the use of the HSOI process for analog design. We will irradiate several of these devices, along with the associated single transistor PM bars, in order to make sure we understand the behavior of the circuit designs and their analog performance under irradiation. The evaluation of these devices is a critical next step towards the submission of a complete pixel array later this year in the Honeywell SOI process.

Finally, we have already delivered four of the new PLL boards (the LBL/Wisconsin-designed VME board used for all lab test work) which we received in Jan. 99. We will continue to work on debugging more of these cards until the whole set of nine is delivered to our collaborators.

1.1.1.3.3 Production

No activity.

1.1.1.4 Pixel Hybrids (R. Boyd)

Milestones	Baseline	Current	Status
*Compl. 1st proto. Design	1-Sep-98	15-Mar-99	Delayed
*Compl. Assembly of 1st proto.	14-Jan-99	15-Jul-99	Delayed
*1st prototype design review	18-Feb-99	20-Feb-99	Complete
*Compl. Tests of 1st protos.	15-Apr-99	17-Sep-99	Delayed
*Select hybrid type	15-Apr-99	22-Feb-99	Complete
*2nd proto design review	28-Apr-99	15-Jun-99	Delayed
*Compl. 2nd proto design	25-May-99	15-Aug-99	Delayed

An additional prototyping step has been added, prototype 1.x, which is an improved version of the 1st prototypes. Additional milestones will be added next month to reflect this situation and to delineate better the prototype program.

Oklahoma
1.1.1.4.1 Design

The Pixel Detector Steering Group selected flex as the baseline for all elements of the Pixel detector except the B layer. This allows to development of a detailed plan for Flex Hybrid and Module design, prototyping, and testing, leading into production (June 99).
Another vendor has been identified for Flex Hybrid prototype fabrication. Dyconex (Zurich) has quoted approximately $33 per piece. They have previous experience in fabrication for D0 at Fermilab.
The floor plan sketch for the version 1.x prototypes has been reviewed in an informal meeting between UOK, LBNL and Genova at CERN. Comments and suggestions from this meeting have been compiled and circulated among these groups. The final floor plan and design parameters are to be set by mid-March. The most significant change is from a "U" buss topology to an "H" buss topology. This, along with some other changes, allows room for mounting the first prototype Optical Link, due by the end of summer, 1999. Other changes enhance usability and development flexibility, as well as providing the opportunity to test the module with a full length power cable. This version also corrects some (nonfatal) omissions from the first version and implements several improvements by taking advantage of all the substrate area for routing.

1.1.1.4.2 Development
A 16 chip, FE only module is under construction to try to understand some of the electronics problems, particularly the "high current" problem and the increased noise observed in the full modules. Completion is expected by late March, results should be available soon afterward.
Waveform tests on the full module show no problems, in fact, they look very good. We have also removed the terminating resistor from one end of an LVDS buss on the four chip module to look for transmission line problems as a result. There does not seem to be any discernible difference in waveform quality, as is to be expected given the length of the buss. Since the "H" buss topology effectively halves the buss length, we are proceeding with this scheme for the 1.x prototypes. We are also performing simulations in Maxwell SpiceLink to verify our expectations.
Langston University has assembled a PixelDAQ test stand consisting of a WindowsNT PC, VXI crate with controller and PC interface, GPIB interface and a PCC. They are still awaiting a PLL.
Flex circuit production and testing (Albany) for CLEOIII, Si3 has been completed. Extrapolating from the CLEOIII design and yields, it should be reasonable to expect at least an 80% yield for the present Flex Hybrid design in the case of fabrication by General Electric Corporate Research and Development.
Wire bonding studies by Purdue and Cornell have shown that wire bond pull strengths of 8 gmf are consistently obtainable for flex wire bonds. Further, they have shown that the quality of flex wire bonds can be evaluated visually.

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, M. Gilchriese)

Milestones	Baseline	Current	Status

*Compl. 1st proto. Design	29-Oct-98	1-Mar-99	Delayed
*1st proto. Design review	18-Feb-99	18-Feb-99	Complete
*Compl. Tests of 1st protos.	18-Mar-99	17-Sep-99	Delayed
*Select module type	18-Mar-99	22-Feb-99	Complete
*2nd proto. Design review	17-Sep-99	10-Sep-99	On schedule

We are projecting additional delays this month for the completion of the 1st prototype design, which is directly tied to the completion of the flex hybrid design. Although a 1st generation prototype design has been completed, and modules assembled, we have decided to implement a 1.x generation design that includes improvements but is not yet a 2nd prototype. See the discussion under 1.1.1.4.1. A more detailed set of milestones will be available next month

1.1.1.5.1 Design/Engineering.

No activity.

1.1.1.5.2 Development and Prototypes

LBNL
As much of this month we were on travel for the ATLAS week, not as much work was done in the lab. The major advance has been to put together the first solder-bumped module with our chips. The multi-chip assembly was built by IZM (Berlin), and shipped to us in mid Feb. We have mounted this on the new generation of support cards, which includes a number of improvements over the original support card. Although we continue to have significant difficulties in wire-bonding assemblies that we receive from IZM, we eventually succeeded in getting the module wire-bonded properly. We are discussing this particular problem with IZM, and expect to carry out detailed surface analysis on the next sets of assemblies we get from them, prior to wire bonding. We will compare the surface analysis of bare electronics die and the solder-bumped assemblies to determine what the differences are and what could be altered to improve the wire bonding of these assemblies.

This new module behaves significantly differently than all previous modules (which were bumped by Boeing using Indium bumps). The performance of the module is very close to that of single chip assemblies, and all signs of instability or anomalous noise have disappeared. This situation was somewhat anticipated after making detailed comparisons of single chip assemblies with the same detector type, one bumped by Boeing and one by IZM. These assemblies contain internal guard rings that (by accident) are included in the bumping masks. This means that all pixels in certain regions of the chip are bumped to a common metal region. In the IZM assembly, as one would expect after shorting large numbers of DC-coupled channels, they all appear dead under charge injection. In the Boeing assembly, they appear alive, but just somewhat noisy. This would imply that they are connected together by some moderately high resistance (10’s of Kohms) in order to remain alive. This provides strong evidence that the residual oxide layers in the Indium bumping process are not being properly “punched through” during normal operation. The bumps themselves then provide a large series resistance to the detector capacitance, and act as a new (and probably unstable) source of series noise. Since the resistance is provided by an oxide layer, it may have rather peculiar time variations and non-ideal I-V characteristics that contribute to the poor behavior of our modules.

We have already made several threshold and noise scans of the new solder module, and it operates very nicely at 3Ke threshold, with 170e threshold dispersion over the complete module (within ATLAS specs for a module) and 140e noise (well within ATLAS specs). This is the first module built which meets these specifications. It also appears to operate nicely in “readout all” mode, used for source scans, and also in the testbeam, with a modest number of hot pixels, but no sign of the instabilities or coherent effects seen in the Boeing modules. IZM should be producing a large number of modules for ATLAS over the next 6-9 months (a total of 50-100), and we look forward to verifying whether the present indications of acceptable performance can be confirmed with higher statistics. In addition, at the module level, this vendor has also shown problems with quality control. The present module has over 1% bad channels due to merged bumps, and also shows signs of many unconnected pixels when exposed to a source. These effects have been seen at well below the 10^{-3} level in single chip assemblies, and now the vendor must put greater emphasis on high quality multi-chip assemblies. IZM has implemented X-ray inspection after seeing our results and has obtained a low defect rate in one module fabricate after the ones sent to us. Work is in progress to implement a QA plan with IZM.

In preparation for ramping up to fabricate the larger number of modules we expect to produce this year, we have probed an additional two wafers of FE-B chips, and will send them off to IZM. This will provide enough chips for an additional five modules. We also expect to receive our first single chip and multi-chip assemblies fabricated using backside plated electronics wafers. This will allow us to make a high-quality substrate contact to the backside and could lead to improved noise behavior in the modules. It is one of the open design issues for the module, as to whether we have to make such connections in the final modules for installation in the detector.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	Done

*Submit 2nd CAFÉ-M	30-Oct-98	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	15-Apr-99	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Done
*Submit 2ns ABCD	27-Jan-99	15-Apr-99	Delayed
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	On Schedule
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	16-Jun-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	31-Aug-99	Delayed
*Test systems complete	26-Apr-99	26-Apr-99	OnSchedule
*1st ICs avail. For 2nd proto hybrid	18-May-99	30-Sep-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	31-Aug-99	OnSchedule

1.1.2.1.1 Design/Engineering

LBNL & UCSC

Simulation and verification work is still proceeding with the ABC design. Simulations have turned up several bugs in the digital logic, which have been fixed. Also, a few potential speed limitations in the layout have been improved. The goal agreed to at the Design Review in January is to have all components of the circuit working at 80 MHz to 100 MHz with nominal models in order to guard band for slow-downs due to process and radiation effects.

Work is still continuing to understand and correct the oscillation problem with the ABCD. Much progress was made in understanding the effects of AC coupling to the substrate material. Simulations still do not reproduce exactly the measured effects but unstable behavior can be observed in the simulations under some conditions. Several changes have been made in the layout to mitigate these problems. The critical question now is if the changes are sufficient. The SCT collaboration agreed to have a design review towards the end of March with all involved engineers and physicists in attendance to review present understanding and decide if the chip is ready for submission.

Work on the CAFE-P wafer testing is proceeding. This month it focused on a probe card design that will be compatible with UCSC and Maxim test equipment and will provide necessary response and noise immunity.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

Some CAFE-M chips and DMILL test structures were irradiated at the LBNL 88" cyclotron to further study radiation damage effects. For this run, the beam was purposely defocused to reduce the dose rate to 10 krad/hour. This is an attempt to understand if dose rate effects can partially explain the differences in Co^{60} and proton data from last year. This low proton dose rate is close to the highest Co^{60} dose rate used previously. At month end, we were still waiting for the parts to "cool down" so that they could be handled.

1.1.2.1.3 Production

No activity.

1.1.2.2 Silicon Strip Hybrids (C. Haber)

Milestones	Baseline	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97	Complete
Complete fab of 1st prototype	2-Feb-98	23-Mar-98	Complete
Preliminary design review	3-Aug-98	1-May-99	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	15-May-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	15-May-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	15-May-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Aug-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Aug-99	Delayed
*Compl. 2nd proto assembly	17-May-99	15-Aug-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	1-Sep-99	Delayed

The hybrid design delays have increased since they are linked to the completion of the layout of the ABC/ABCD chips and to the fabrication schedule for these chips.

LBNL

1.1.2.2.1 Design

A meeting was held at CERN with ASIC and hybrid designers to discuss design issues which could effect noise and stability. A number of suggestions for tests and possible features were made. One significant point concerns the use of a single ground plane instead of the present split analog and digital planes. A test of this is being made a CERN in the next few weeks.

1.1.2.2.2 Development and prototype fab

A meeting was held at CERN to discuss further plans for prototype fabs and usage. All such fabs still await final redesigns of the ABC and ABCD chips.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98	Complete
Prototype tooling complete	1-Apr-99	1-Aug-99	Delayed
*Compl. Design of proto assy/test	14-Jun-99	14-Aug-99	Delayed
*Compl. Fab of tooling for proto	14-Jun-99	14-Aug-99	Delayed

As noted below the tooling workshop will be held in late May. The module construction and evaluation activity is hostage, in part, to the lack of good front end ASICs. The delay indicated above reflects the slip in the time of the tooling workshop as well as the requirement to have built prototype modules with chips from the next submission.

LBNL
1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

A tooling workshop will be held at the Rutherford Lab in the UK the week of May 24, 1999. This was originally planned for March of 1999.

Design of a new calibration plate was completed last month. Work began to prepare the GDS-2 files needed for fabrication. The design was also reviewed in a meeting at CERN and approved by the interested groups.

A visit from the Smart Scope representative occurred and the new software was evaluated in December. We received a quote for the upgrade last month. The order was placed.

Design continued on a folding fixture for the hybrids.

Another dummy module was fabricated with the wrap around hybrid set included this time.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford/R. Jared)

Milestones	Baseline	Current	Status
*Select PreROD implementation	30-Oct-98	4-Nov-98	Complete
*Requirements review	30-Nov-98	18-Nov-98	Complete
*Compl. System design	28-Dec-98	28-Dec-98	Complete
*System design review	11-Jan-99	26-Mar-99	Delayed
*Compl. PreROD design	29-Jan-99	31-Mar-99	Delayed
*Compl. PreROD layout	15-Feb-99	15-Apr-99	Delayed
*Compl. PreROD procure	1-Mar-99	30-Apr-99	Delayed
*Compl. PreROD PCB fab	16-Mar-99	16-May-99	Delayed
*Compl. PreROD 1st assemble	30-Mar-99	31-May-99	Delayed
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	15-Jul-99	Delayed
*PreRODs complete	20-Aug-99	20-Aug-99	On schedule
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

1.1.3.1.1 Strip Test Beam Support

UC Irvine

Hardware and software support for laboratory and beam tests of SCT electronics and modules continued. A DSP readout system was sent, and technical support was given, to users at Prague to help establish a silicon readout system there. An additional crate hardware setup was sent to users at University of Melbourne. Code was tested for using the DSP in burst mode readout with varying event size. This code allows for more efficient memory use of the DSP for faster data-taking.

1.1.3.1.2 Pixel Test Beam Support

University of Wisconsin

Hardware debugging of the PLL continues. In addition coding of the FIFO for trigging is progressing. The code is written and debugging continues.

1.1.3.2.1 ROD Requirements

Definition of ROD requirements is largely complete. No new requirements were defined in February.

UC Irvine

The Monte Carlo simulation of SCT module occupancy was modified to include more detailed information about correlations between modules. Instead of averaging over all the modules in the detector, independent module-by-module data was stored for entire events. This occupancy data contained long tails with some modules containing over 200 hits. These new distributions are being used to check decoding algorithms.

The latency for delivery of *L1Accept* signals through the ROD was further studied as part of continued studies of the overall level 1 latency through the SCT system.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No significant refinements of the essential model were made during February.

1.1.3.2.3 ROD Implementation Model

Early in February, ROD design effort continued to focus on a combined FPGA/DSP implementation in order to combine the best features of the FPGA-based and DSP-based approaches studied previously. Studies centered on the decoder section, which in the combined approach would utilize both an FPGA and a DSP. Simulation revealed that occupancy of buffers in the FPGA would occasionally become large for buffers of practical size, suggesting that data loss might occasionally occur. Although the amount of data loss would not be large, the frequency of buffer overflow at the very large data rates of the SCT would be difficult to manage in a simple fashion. The difficulties in realizing a practical combined FPGA/DSP implementation led by mid-month to the decision that the combined approach to decoding was not better than either decoding by FPGA or DSP alone. Guidance will be sought regarding selection between a ROD implementation based on FPGA decoding with DSP histogramming and monitoring in the back end or a ROD implementation based on DSP decoding as well as histogramming and monitoring. A review will be held March 25-26.

UC Irvine

The primary focus of activity at UCI in the first half of February was exploring the combined FPGA/DSP implementation model. In the second half of the month, studies of various aspects of the DSP implementation model were resumed, including decoder emulation on a DSP evaluation module. Host DSP issues were also further evaluated, and development of software to simulate DSP host software continued. Work also continued on a ROD software development platform using two cooperating TI DSP evaluation modules for more complete emulation of a ROD system.

A document describing timing at the interface of the ROD and the Back-of-Crate Card (BOC) was completed and posted on the web at:

http://positron.ps.uci.edu/~pier/ROD/pdf/ROD_BOC_Interface0.PDF.

The ROD slot pin assignments were changed to adapt to the 9U VME64x standard being adopted by ATLAS. Updated documentation can be found at:

http://positron.ps.uci.edu/~pier/ROD/pdf/RodPinoutVME64x0.PDF.

These documents are pertinent to both FPGA and DSP implementation models.

Latency calculations

University of Wisconsin

The primary focus was the modeling of the DSP/FPGA ROD. A complete model of the data flow was written and used to simulate the real time behavior of the ROD. The result of the simulation was that the ROD had buffer overflows. No solution was found to the problems. This resulted in the dropping of the DSP/FPGA model.

1.1.3.3.7 Preprototype ROD

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed primarily above under WBS 1.1.3.2.3.

UC Irvine

An initial investigation of DSP data and address busses for ROD99 was carried out using the IBIS simulation package.

Wisconsin

The main effort has been to target the FPG based ROD to the newer family of FPGAs. The decoder and gather are the central focus of this effort that is aimed to be sure that there will be on surprises in the future. This effort will continue in March.