Implementation and Algorithms for the FPD DSM Tree

Falk Meissner

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Description: The first two layers of DSM boards build the ADC sum for each of the 8 detector modules. All these sums are available in the third layer, which sets three thresholds on each sum. These thresholds are SIZEORDERED $th0 < th1 < th2$. The thresholds are the same for all 8 modules. A register selects which of the three thresholds is used to trigger STAR, if any of the 8 modules is above it. The three thresholds are coded into two bits indvidually for each module and these 8*2 bits are available in the scaler board.
Find a drawing of the FPD-DSM tree at
http://www.star.bnl.gov/STAR/html/fpd_l/fy03/electronics/index.html

1 FPD-layer0, FPD-FE/W-001, 002, 003, 005, 006, 007

Input: 14x8bit ADC values from North/South Modules

Registers: None

LUT: Pedestal subtraction

1st. Clock: Add 3*4 and 1*2 PMT ADCs to intermediate ADC-Sums (adding 14 channels needs two steps)

2nd Clock: Add intermediate sums to 12 bit ADC sum

Output (0-11) ADC sum, (12-15) empty

2 FPD-layer0, FPD-FE/W-004

Input: 2x7 8bit ADC values; split module
North and South are swaped for East and West crate
ch0-6 East-North; West-South
ch7-13 East-South; West-North

Registers: None

LUT: Pedestal subtraction

1st. Clock: Build intermediate ADC-Sums

2nd Clock: Add intermediate sums to 11 bit ADC sums seoarately for North and South

Output (2 cables)
Lower bits East-North; West-South
(0-10) ADC sum, (11-15) empty
Upper bits East-South; West-South
(16-26) ADC sum, (27-31) empty

3 FPD-layer0, FPD-FE/W-008-010

Input: 15 8bit ADC values from Top/Bottom modules

Registers: None

LUT: Pedestal subtraction

1st. Clock: Intermediate ADC-Sums

2nd Clock: Add intermediate sums to 12 bit ADC sums

Output (0-11) ADC sum, (12-15) empty

4 FPD-layer0, FPD-FE/W-008-010

Input: 10 8bit ADC values from Top/Bottom modules

Registers: None

LUT: pedestal subtraction

1st. Clock: intermediate ADC-Sums

2nd Clock: Add intermediate sums to 12 bit ADC sums

Output (0-11) ADC sum, (12-15) empty

5 FPD-layer1, FPD-FE/W-101, North-South modules

Both clock ticks are needed to combine 3*12 bit and 1*11bit numbers to the 14bit ADC sum of a detector module.

Input: 8xADC sums ch0-3 E-N/W-S and ch4-7 E-S/W-N

Registers: None

LUT: 1:1

1st. Clock: Intermediate ADC-Sums

2nd Clock: Add intermediate sums to 14 bit ADC sums

Output (2 cables)
Lower bits East-North; West-South
(0-13) ADC sum, (14-15) empty
Upper bits East-South; West-South
(16-29) ADC sum, (30-31) empty

6 FPD-layer1, FPD-FE/W-102, Top/Bottom

Input: 4*12bit ADC sums ch0-1 Top; ch2-3 Bottom

Registers: None

LUT: 1:1

1st. Clock: Build 13 bit ADC-Sums

2nd Clock: Delay output

Output (2 cables)
Lower bits Top
(0-12) ADC sum, (13-15) empty
Upper bits Bottom
(16-28) ADC sum, (29-31) empty

7 FPD-layer2, L1-FP201

Input: One ADC sum per detector module
ch0: East-North
ch1: East-South
ch2: East-Top
ch3: East-Botton
ch4: West-South
ch5: West-North
ch6: West-Top
ch7: West-Botton

Registers: L1: index:11
Thresholds have to be size ordered $th0 < th1 < th2$!
R0: ADC-threshold-0
R1: ADC-threshold-1
R2: ADC-threshold-2
R3: FPD-trigger-threshold-select: '0'-th0; '1'-th1; '2'-th2; '3'-off R4: FPD Mask 8bits, 0-off; 1-on
mask 7-0 is 7=BW, TW, SW, NW, BE, TE, SE, 0=NE
mask 0x0f is east only, 0xf0 is west only

LUT: 1:1

1st. Clock: Place thresholds on all input ADC sums

2nd Clock: Code threshold comparision into scaler bits seperately for all 8 modules. Two bits per module: '00'-ADC<th0, '01'-ADC>th0, '10'-ADC>th1, '11'-ADC>th2. STAR fpd trigger fires if any module is above threshold as selected by R3.

Output (2 cables)
Lower bits to last DSM 301
(0) FPD-trigger East
(1) FPD-trigger West
(2-15) empty

Upper bits to FPD scaler, see below

8 FPD asymmetry scaler

Bit	Name	From DSM	JP6 Bit
1	BBC TAC-Window 0	VT201	0
2	FPD-NE-thbit0	FP201	0
3	FPD-NE-thbit1	FP201	1
4	FPD-SE-thbit0	FP201	2
5	FPD-SE-thbit1	FP201	3
6	FPD-TE-thbit0	FP201	4
7	FPD-TE-thbit1	FP201	5
8	FPD-BE-thbit0	FP201	6
9	FPD-BE-thbit1	FP201	7
10	FPD-SW-thbit0	FP201	8
11	FPD-SW-thbit1	FP201	9
12	FPD-NW-thbit0	FP201	10
13	FPD-NW-thbit1	FP201	11
13	FPD-TW-thbit0	FP201	12
14	FPD-TW-thbit1	FP201	13
15	FPD-BW-thbit0	FP201	14
16	FPD-BW-thbit1	FP201	15
17	CTB multi>N	LD301	1
18-24	bunch id		