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Title:

Viewgraphs:
Consequences and Categories of SRAM FPGA Configuration SEUs

Author(s):

Paul Graham,
Michael Caffrey,
Jason Zimmerman,
Darrel E. Johnson,
Los Alamos National Laboratory, Los Alamos NM
Prasanna Sundararajan, Cameron Patterson
Xilinx Inc., San Jose CA

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Los Alamos NATIONAL LABORATORY

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Michael Caffrey,
Jason Zimmermann,
Eric Johnson

Prasanna Sundararajan,
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Outline

- Why care about FPGA SEU types?
- Methodology for classification
- Design studies
- Conclusions and Future work

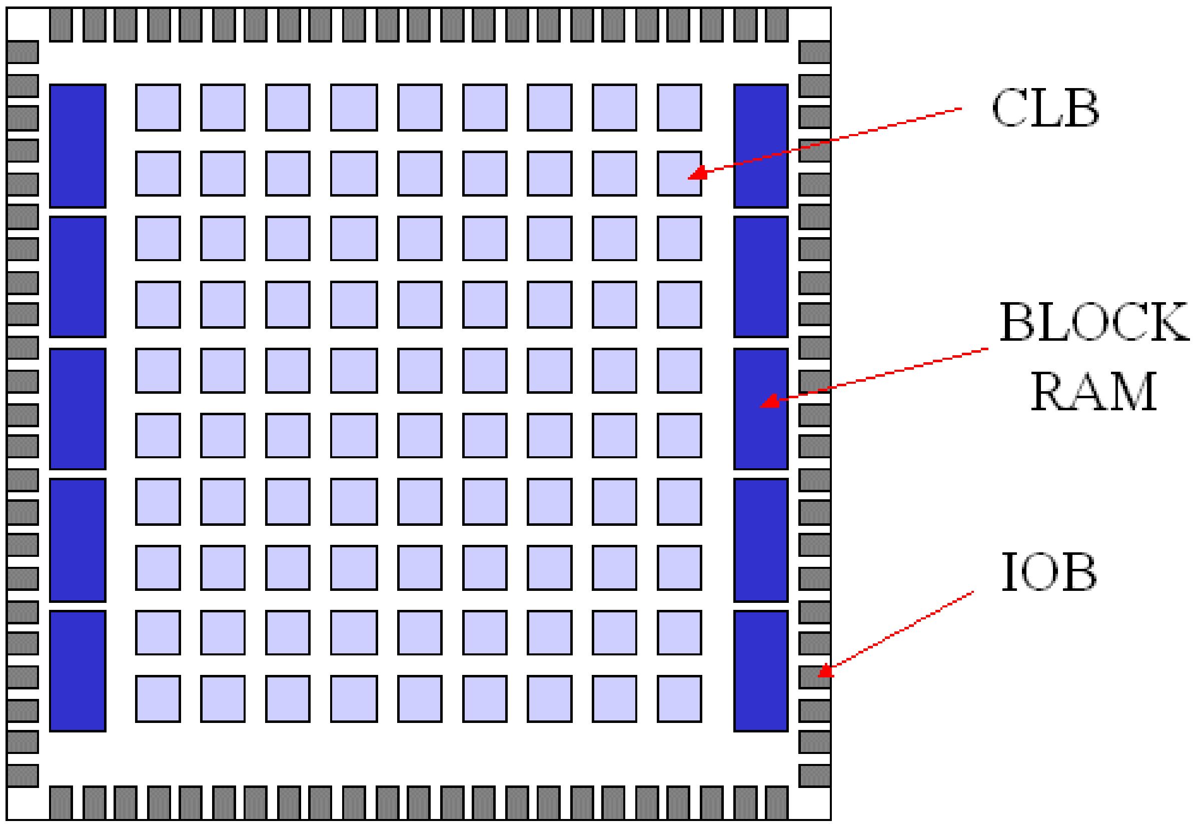
Why care about FPGA SEU types?

- We want to understand what SEU mitigation techniques work while being cost effective.
- *Assumption*: Some designs can allow lower reliability for a reduced mitigation cost.
  - A spectrum of reliability and cost points is possible.

FPGAs aren't ASICs

- Fault models for ASICs don't necessarily apply to FPGAs.
  - SEUs in an FPGA can change the *design*, not just user data.
- Not all SEUs have an effect.
  - Only a subset of resources are used per design.
- SEU mitigation techniques for ASICs may not work for FPGAs.
- FPGA-specific migitation techniques seem possible and may be more cost effective.

Virtex FPGA Architecture: General

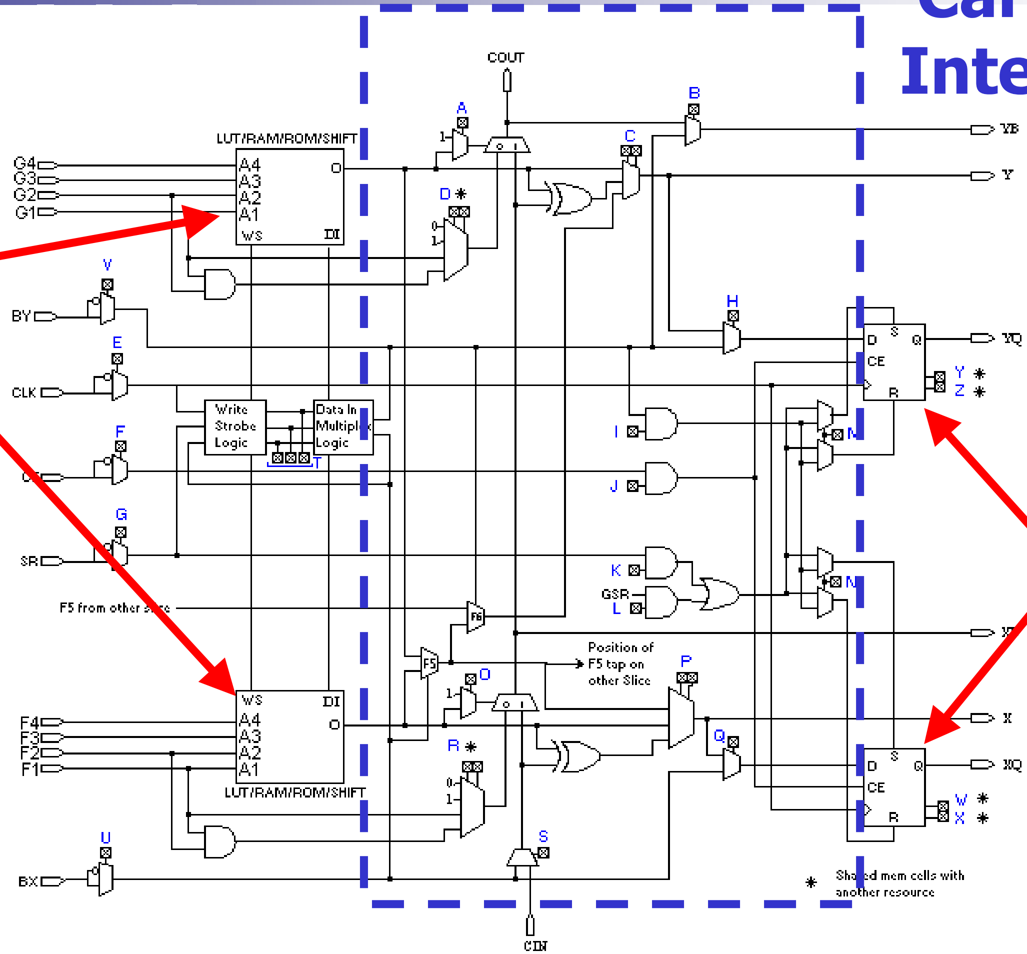


NOTE: Not drawn to scale

Virtex FPGA Architecture: Slice (1/2 of a CLB)

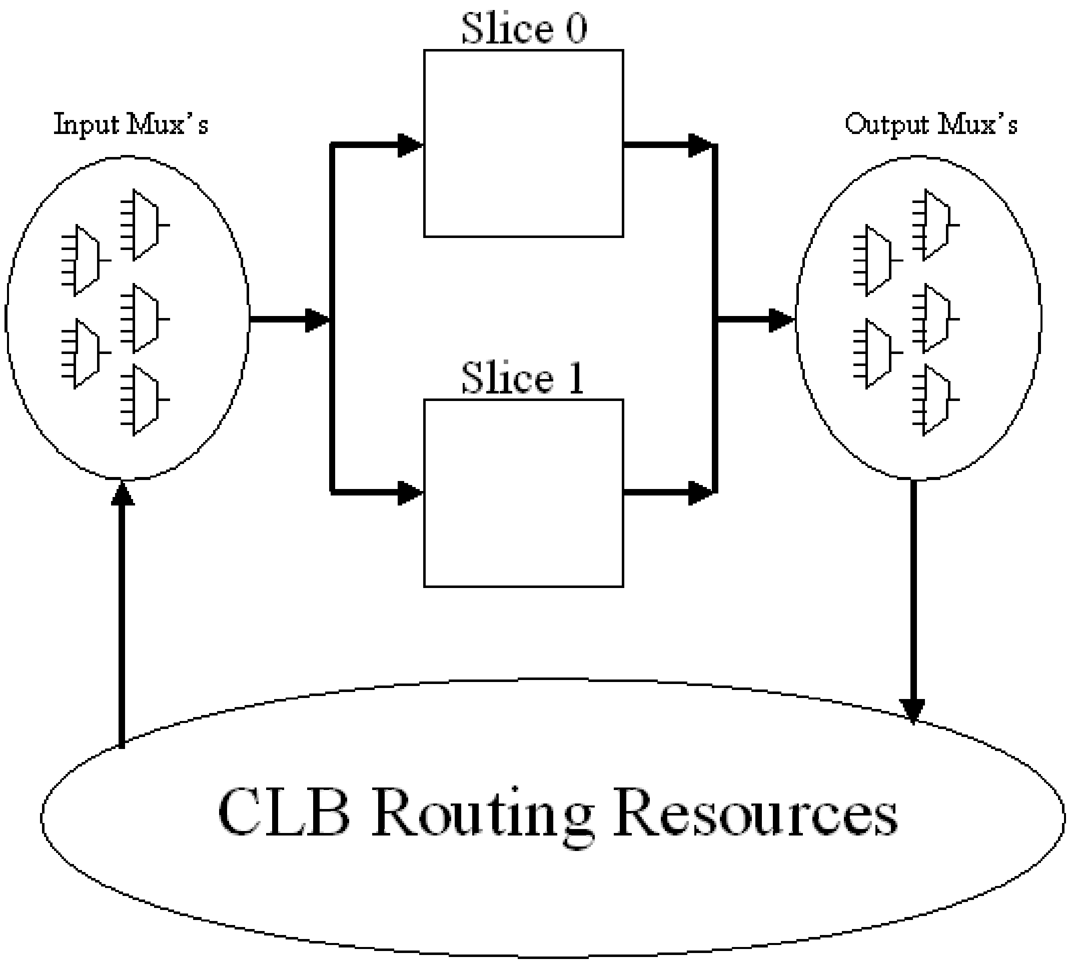
Carry logic and Internal routing

LUTs



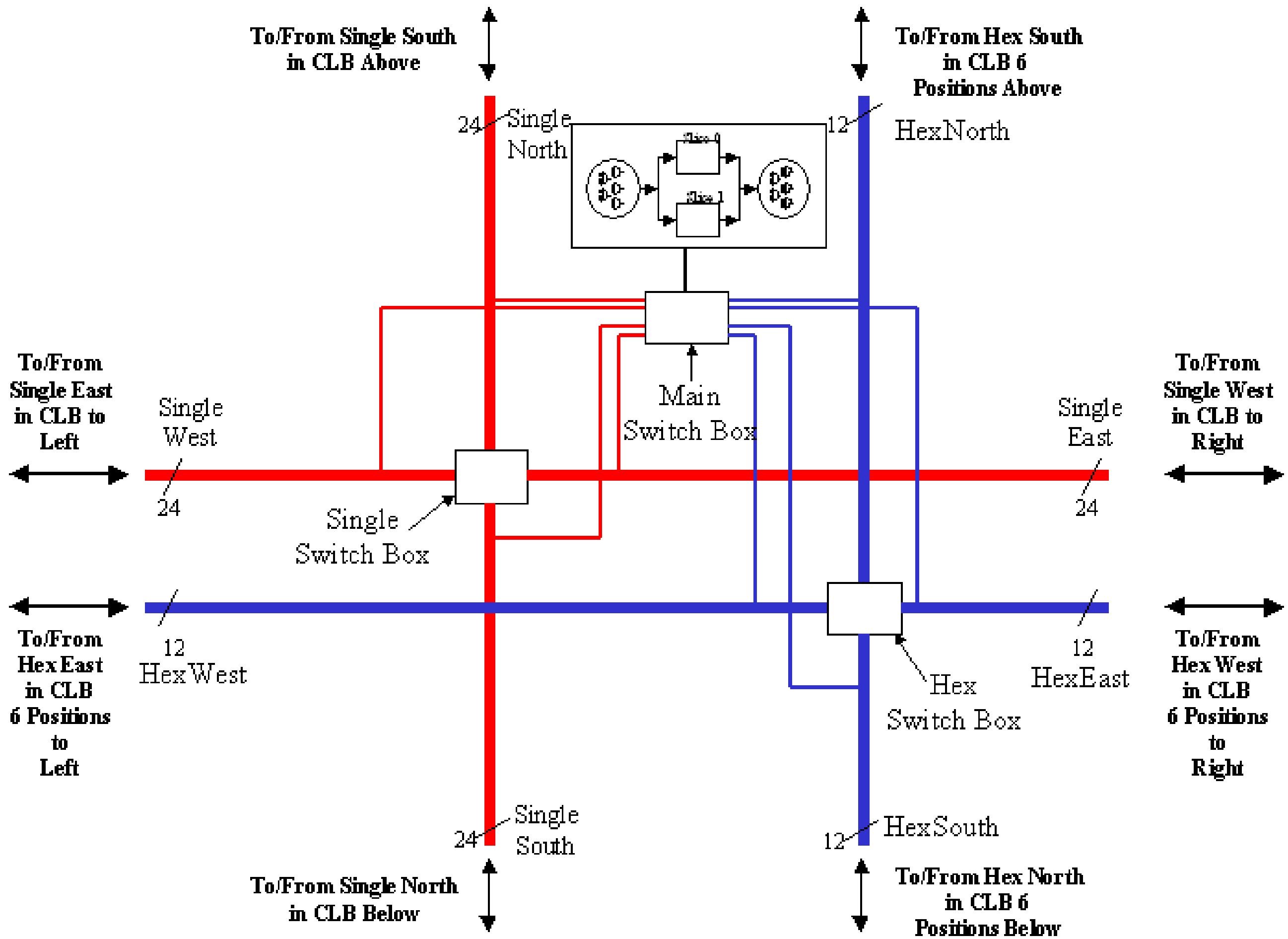
Flip-flops

Virtex FPGA Architecture: Slice Input/Output Muxes



Virtex FPGA Architecture: CLB Routing Resources

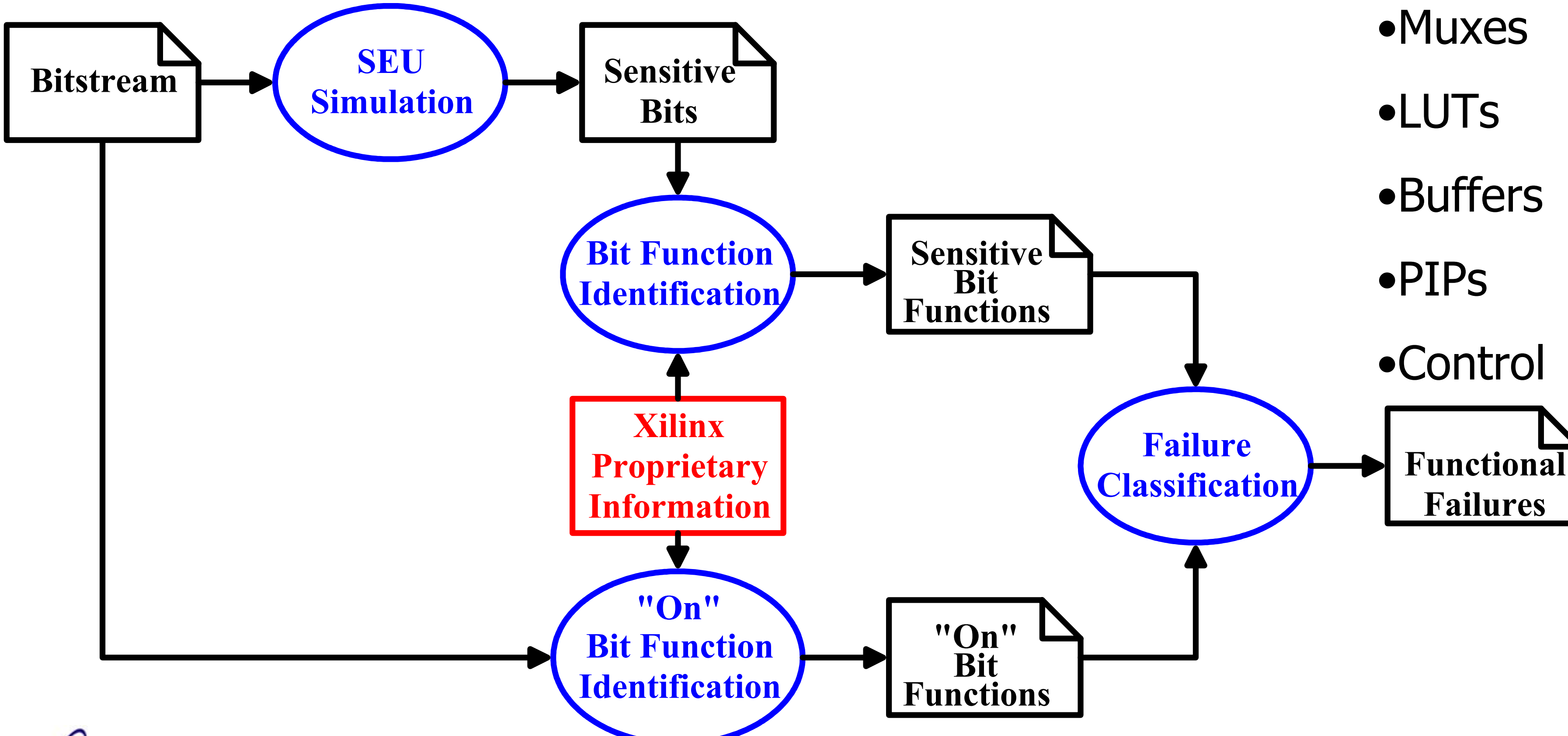
- Single-length wires use programmable interconnect points (PIPs) for switching.
- Hex-length wires use muxes and buffers.
- Resources used for switching *between* routing types varies.



Bitstream SEU Failure Classification Methodology

- Find sensitive bits in a design using SEU simulator
- Identify each sensitive bit's function
- Classify each sensitivity based on
  - Type of resource upset
  - Whether the bit was "on" or "off" in the original bitstream

Bitstream SEU Failure Classification Flow

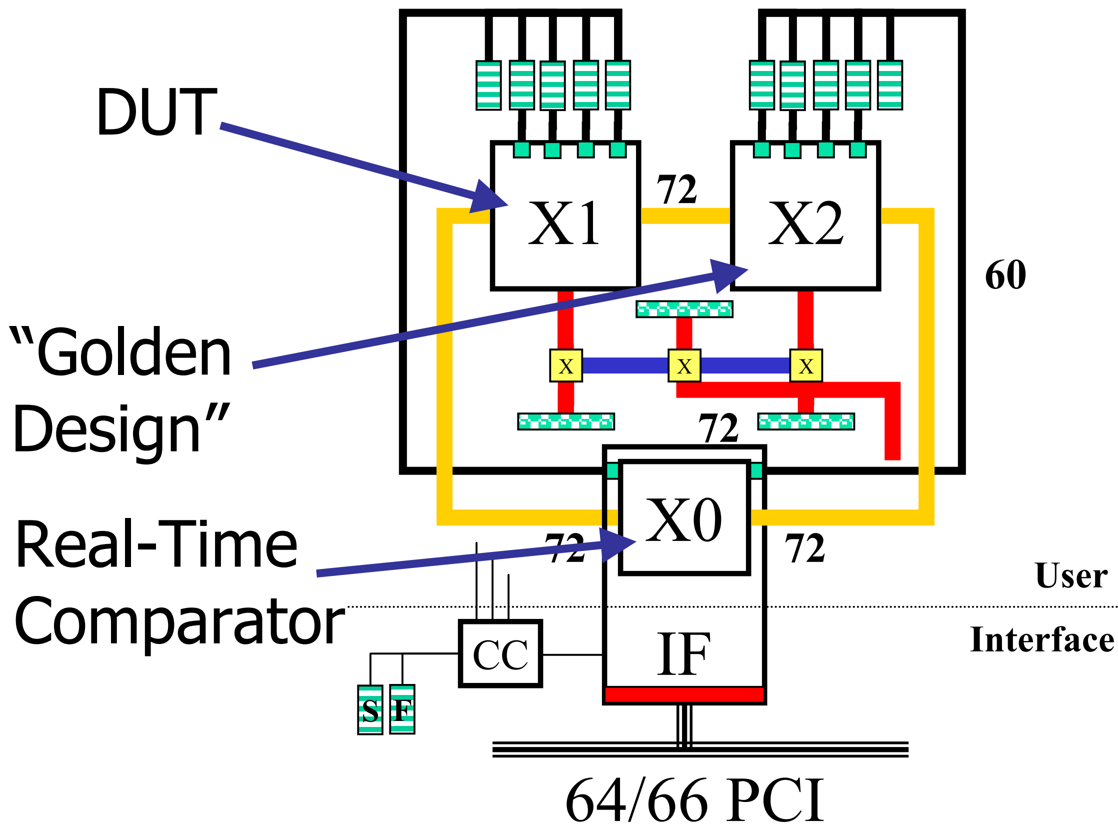


Failures:

- Muxes
- LUTs
- Buffers
- PIPs
- Control

SLAAC-1V SEU Simulation Platform (BYU/LANL)

- Design loaded into *X1* and *X2* and run synchronously
- Inject faults into *X1's* bitstream
- *X0* provides test vectors and compares outputs to identify when a specific bitstream upset affects design operation



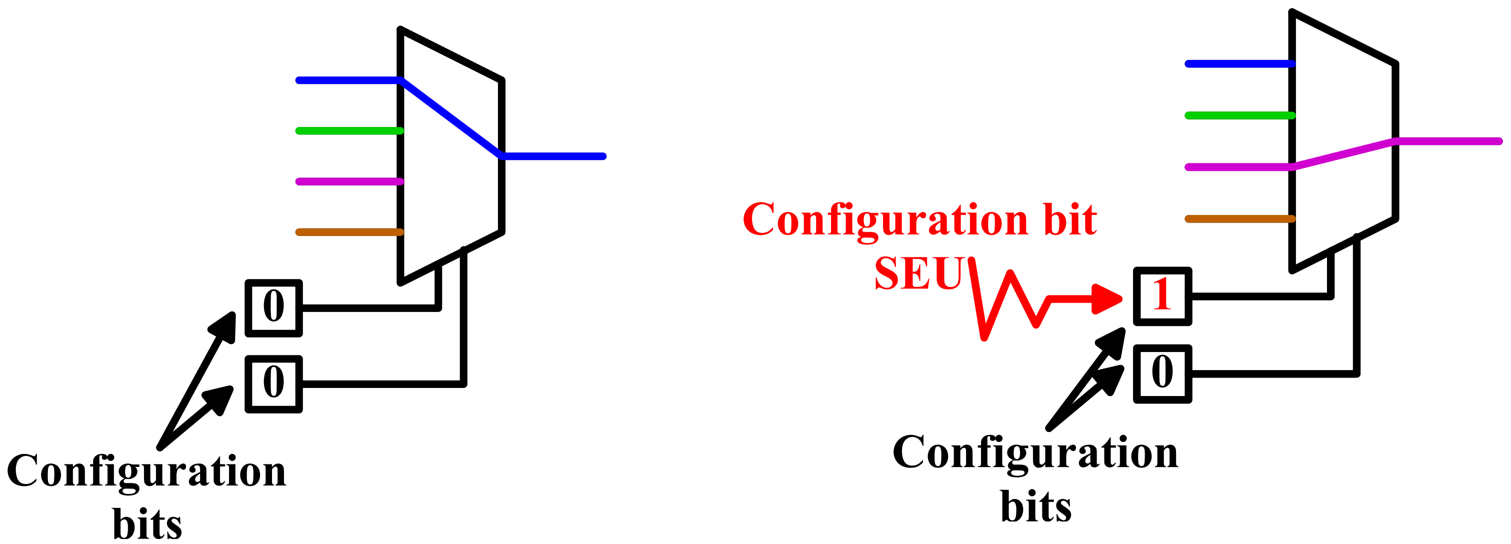
Identifying Configuration Bitstream Functions

- Configuration bitstream function definitions were based on non-disclosure information provided by Xilinx.
- Additionally, JBits' documentation and APIs provided a useful model for understanding the low-level architecture of the Virtex devices.

Classification of circuit failures

- Takes into account the type of resource and the state of the resource in the original bitstream
- Failure modes
  - Mux select upsets
  - Programmable interconnect point (PIP) upsets
    - Opens, shorts, loading
  - Buffer upsets (on/off)
  - Look-up table (LUT) value changes
  - Control bit changes
  - Unclassified (other failures)

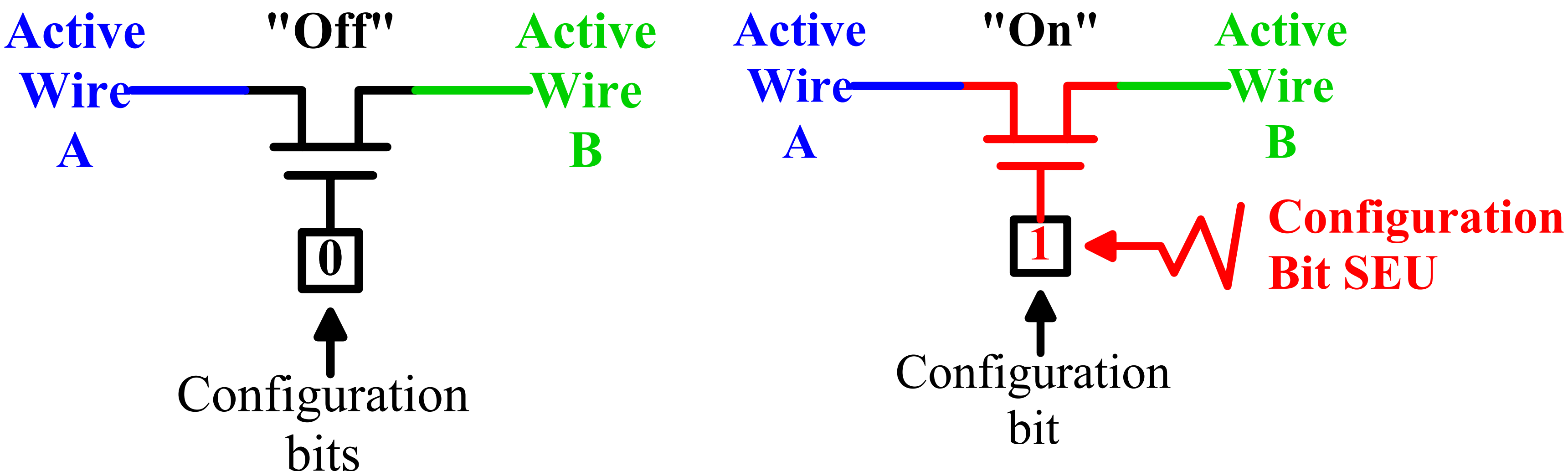
Failure Mode Examples: Mux Select Upsets



(a) Initial mux configuration

(b) Mux after bitstream SEU

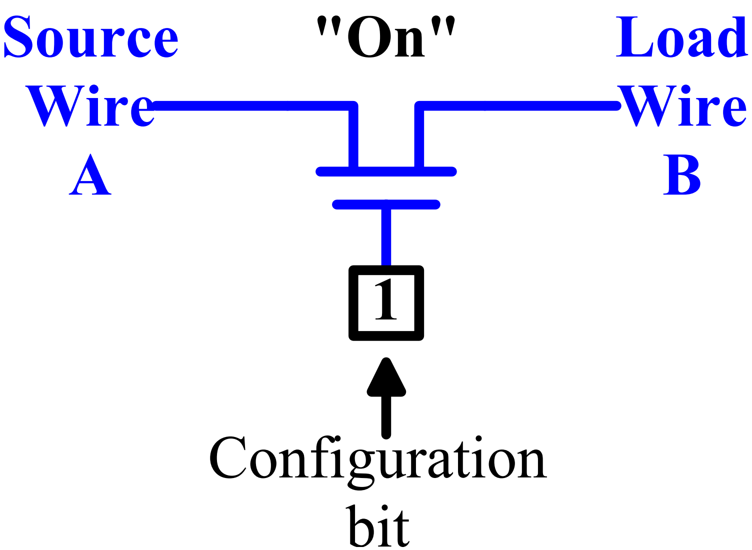
Failure Mode Examples: PIP Short Upset



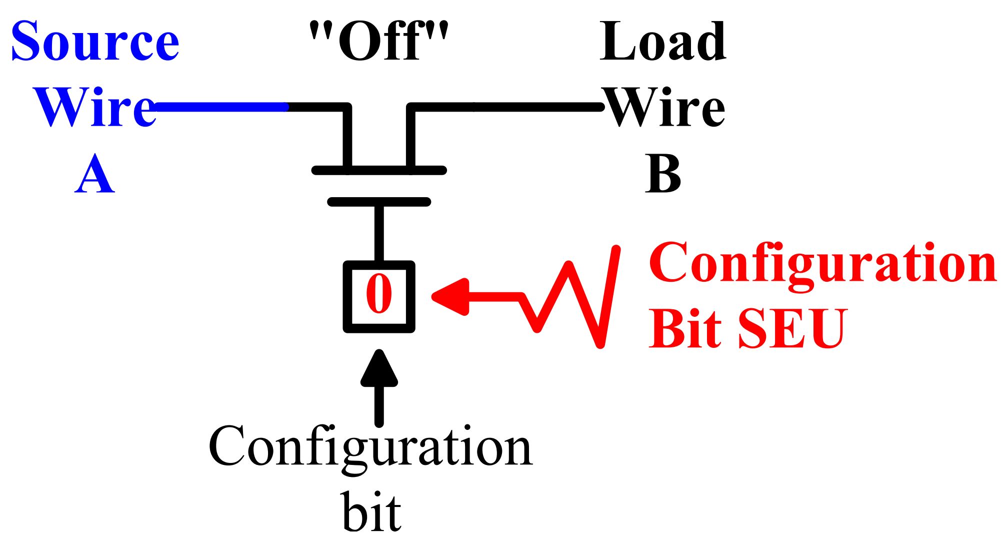
(a) Intended PIP configuration

(b) PIP shorting two independent, active wires

Failure Mode Examples: PIP Open Upset

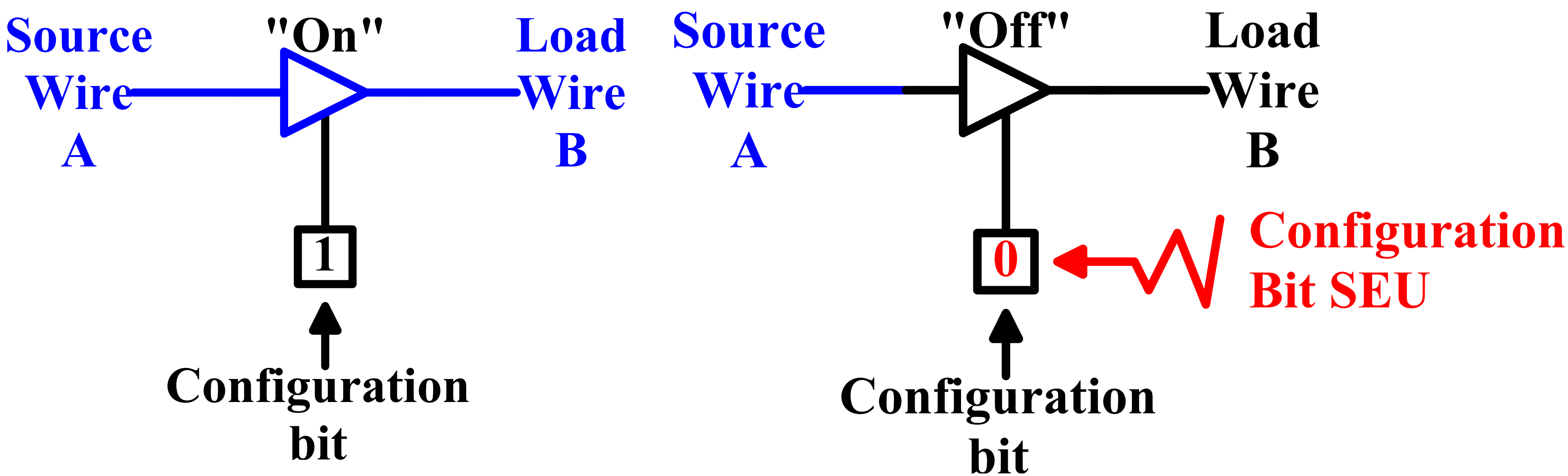


(a) PIP connecting source wire to load wire



(a) PIP upset disconnecting source wire from load wire

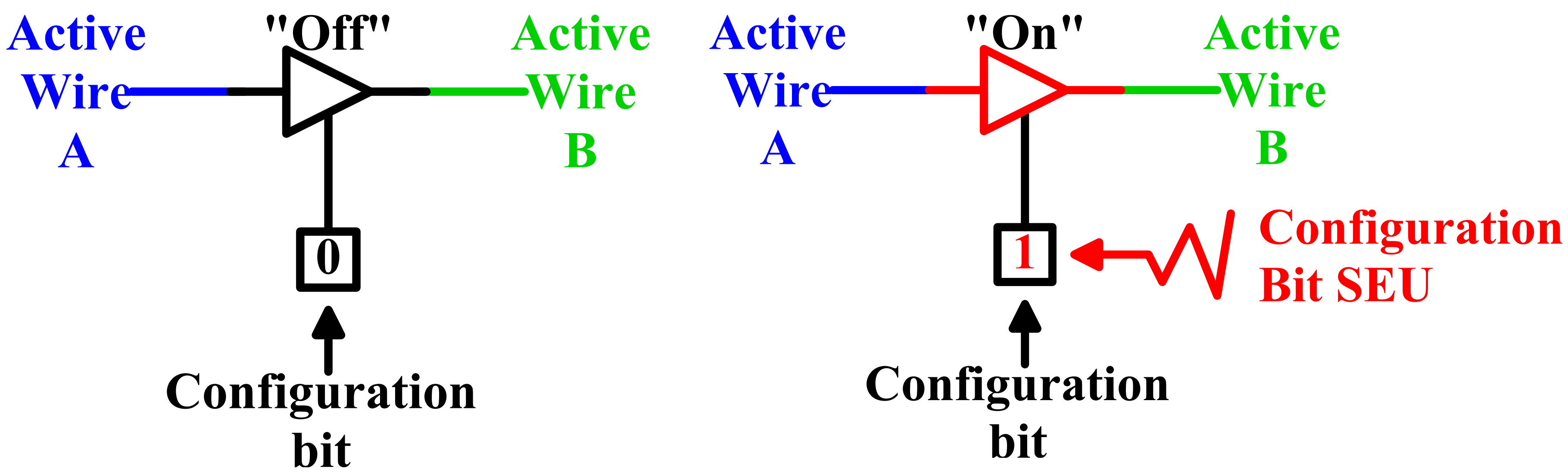
Failure Mode Examples: Buffer Off Upset



(a) Buffer connecting source and load wires

(b) Buffer upset disconnecting source and load wires

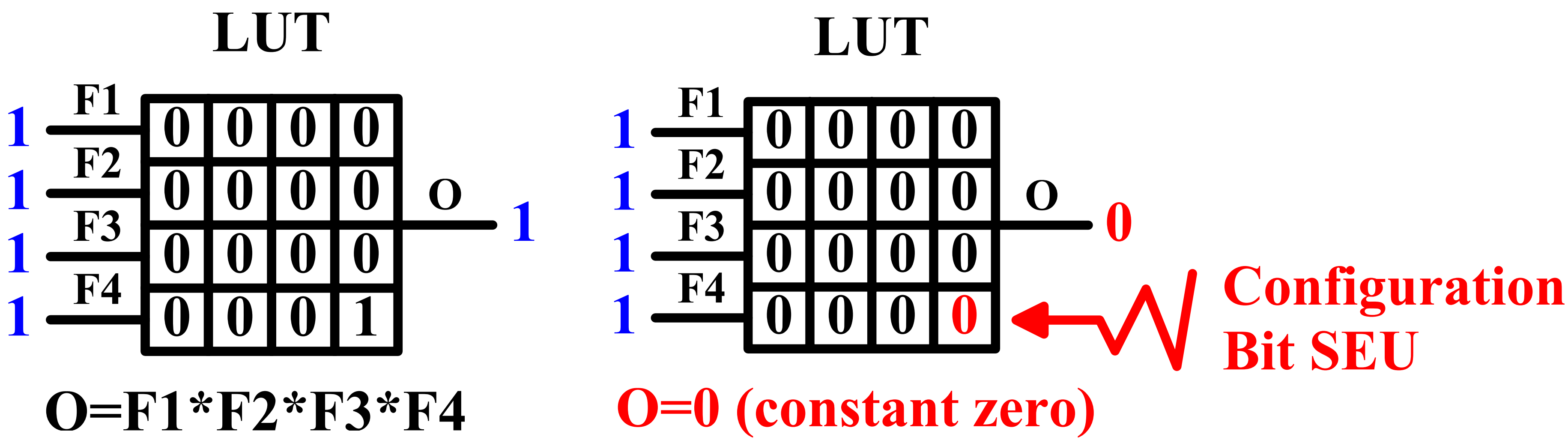
Failure Mode Examples: Buffer On Upset



(a) Unused buffer

(b) Buffer on between two unrelated active wires

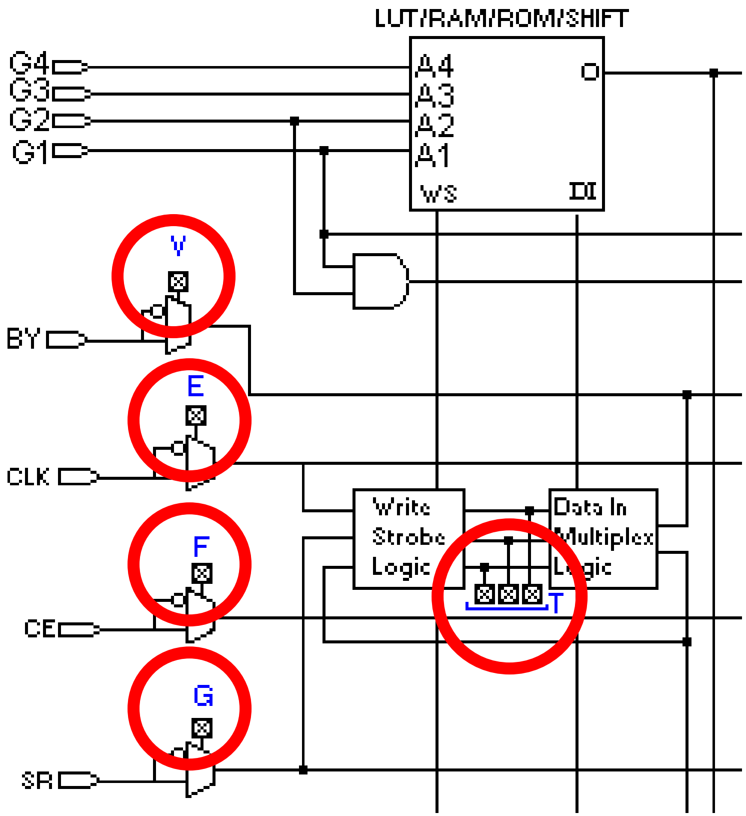
Failure Mode Examples: LUT Value Change



(a) LUT implementing a 4-input AND

(b) LUT bit upset causing the LUT to implement a constant "zero" function

Failure Mode Examples: Control Bit Changes (Slice)



- Bits *V, E, F, and G* control the programmable inversion of inputs
- The *T* bits control whether the LUTs perform as LUTs, RAMs (16x1, dual-ported, 32x1), or shift registers

Examples of Failure Modes Based on Resource Type

Failure Mode	*Resource Type Examples*
Mux select change	Slice/IOB input and output muxes, internal slice and IOB muxes, hex wire routing muxes, etc.
PIP upset	PIPs for single wires, edge routing, etc.
Buffer upset	Bi-directional hex wire buffers, mux output buffers, etc.
LUT change	F and G LUTs in slice/CLB resources
Control change	Slice and IOB control bits (programmable inversions, flip-flop configuration, etc.)
Unclassified	Clock routing and control, configuration register upsets, etc.

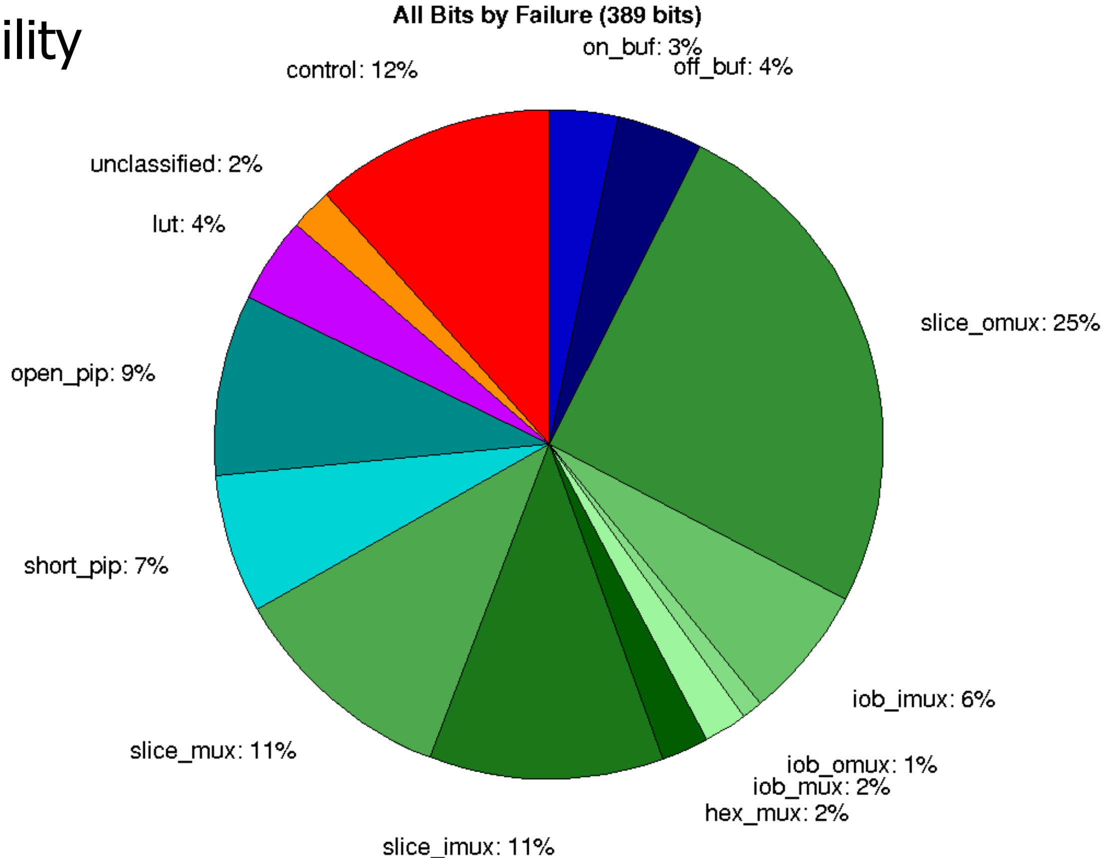
Sample Design Analysis

- Designs
  - Simple: 8-bit counter
  - Control-like: multiple 72-bit linear feedback shift registers (LFSRs)
  - Data Path: 8 36-bit multipliers and a summing adder tree
- Designs do not use IOB flip-flop structures, Block SelectRAM, or advanced clocking features
- Upsets in user-accessible configuration registers were not modeled.

Classification of Failures: 8-bit Counter (unweighted)

- Not weighted by probability of failure
- Control upsets: 12%
- LUT upsets: 4%
- Mux select upsets: 59%
- PIP upsets: 16%
- Buffer upsets: 7%
- Unclassified: 2%

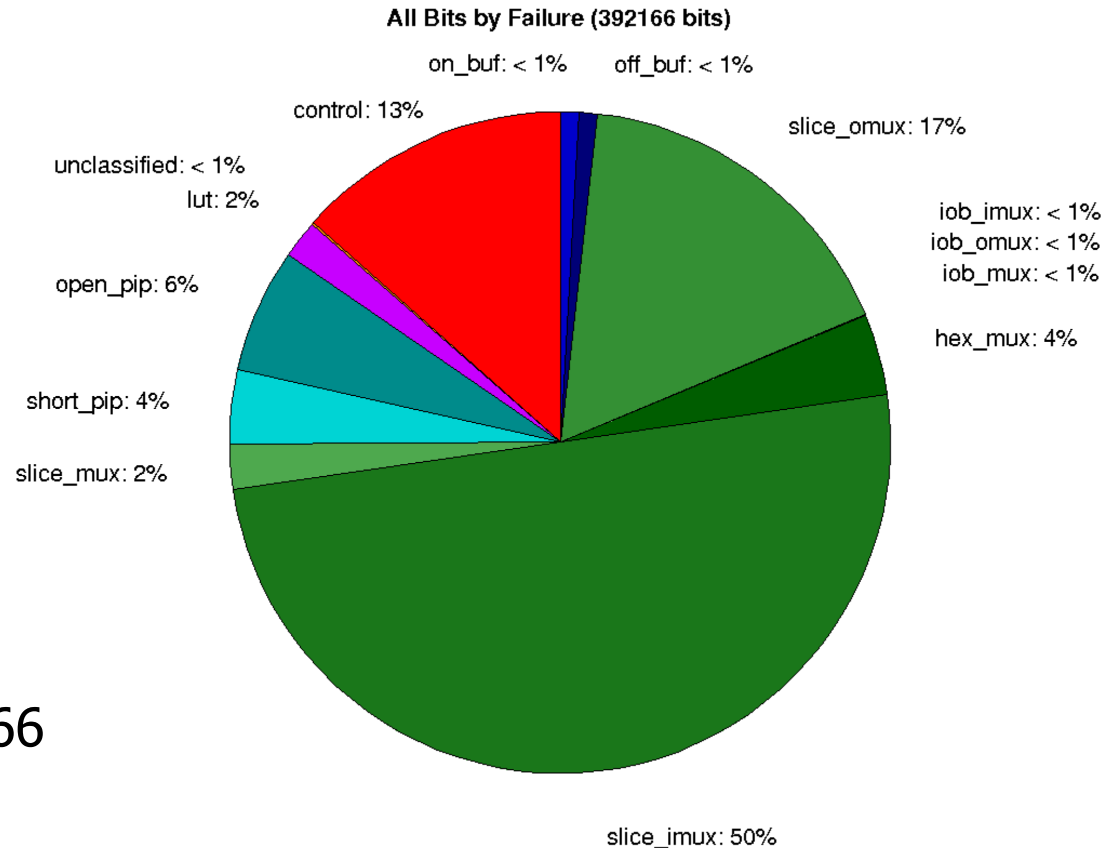
- Routing: 82%
- LUT/Control: 16%
- Total failure bits: 389



Classification of Failures: 72-bit LFSRs (unweighted)

- Control upsets: 13 %
- LUT upsets: 2%
- Mux select upsets: 73%
- PIP upsets: 10%
- Buffer upsets: 1.8%
- Unclassified: <1%

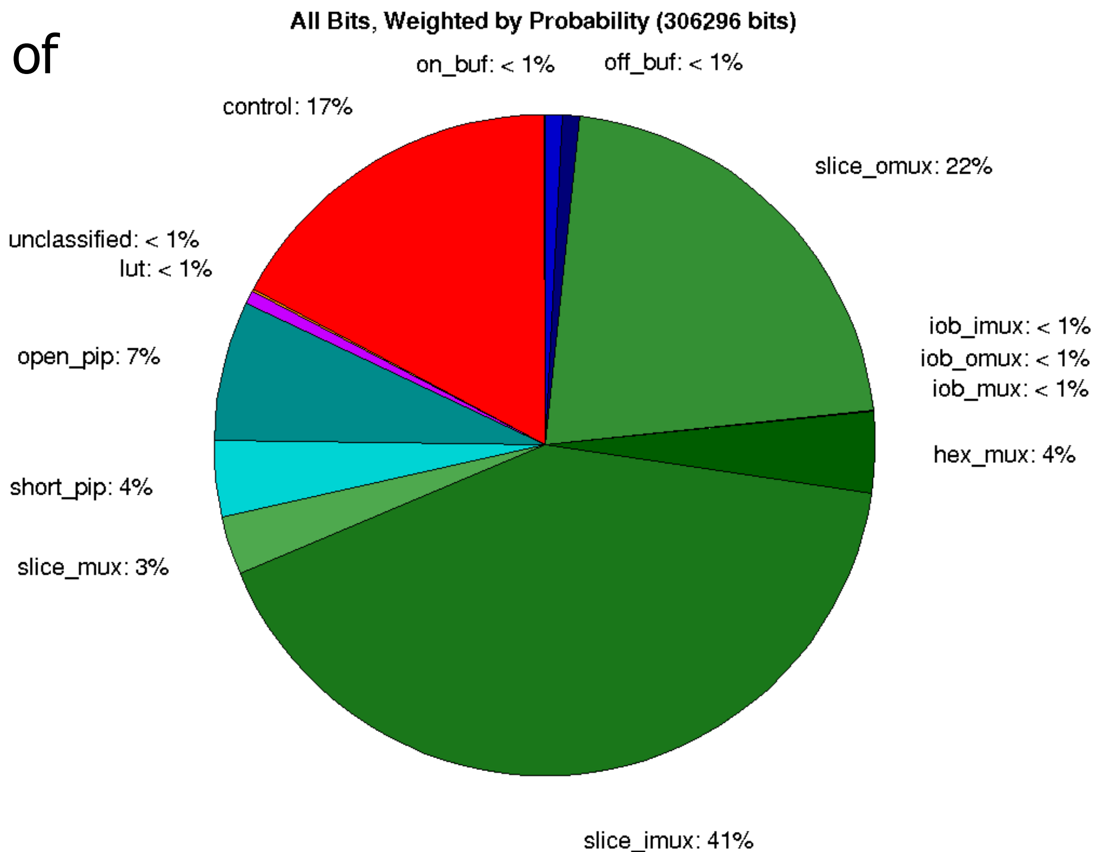
- Routing: 84.8%
- LUT/Control: 15%
- Total failure bits: 392,166



Classification of Failures: 72-bit LFSRs (weighted)

- Weighted by probability of failure
- Control upsets: 17 %
- LUT upsets: <1%
- Mux select upsets: 70%
- PIP upsets: 11%
- Buffer upsets: <2%
- Unclassified: <1%

- Routing: 82%
- LUT/Control: 18%
- Total failure bits: 392,166

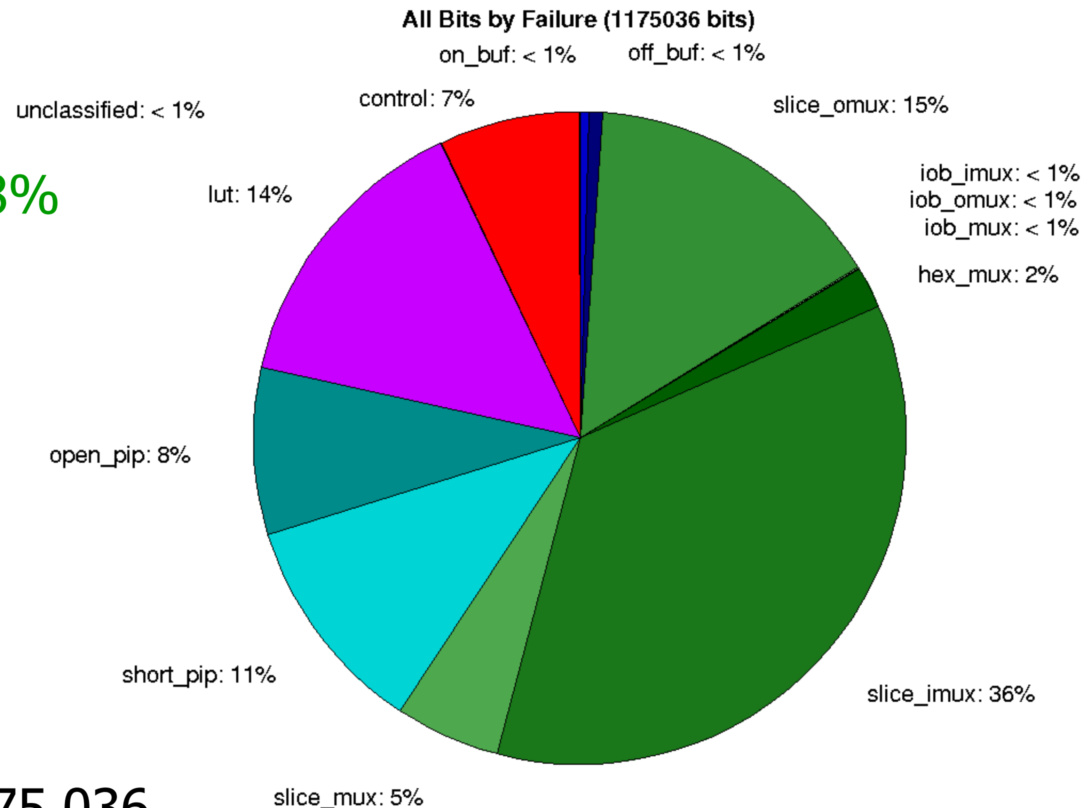


Classification of Failures: Multiply/Add Design (unweighted)

- Control upsets: 7%
- LUT upsets: 14%
- Mux select upsets: 58%
- PIP upsets: 19%
- Buffer upsets: 1%
- Unclassified: < 1%

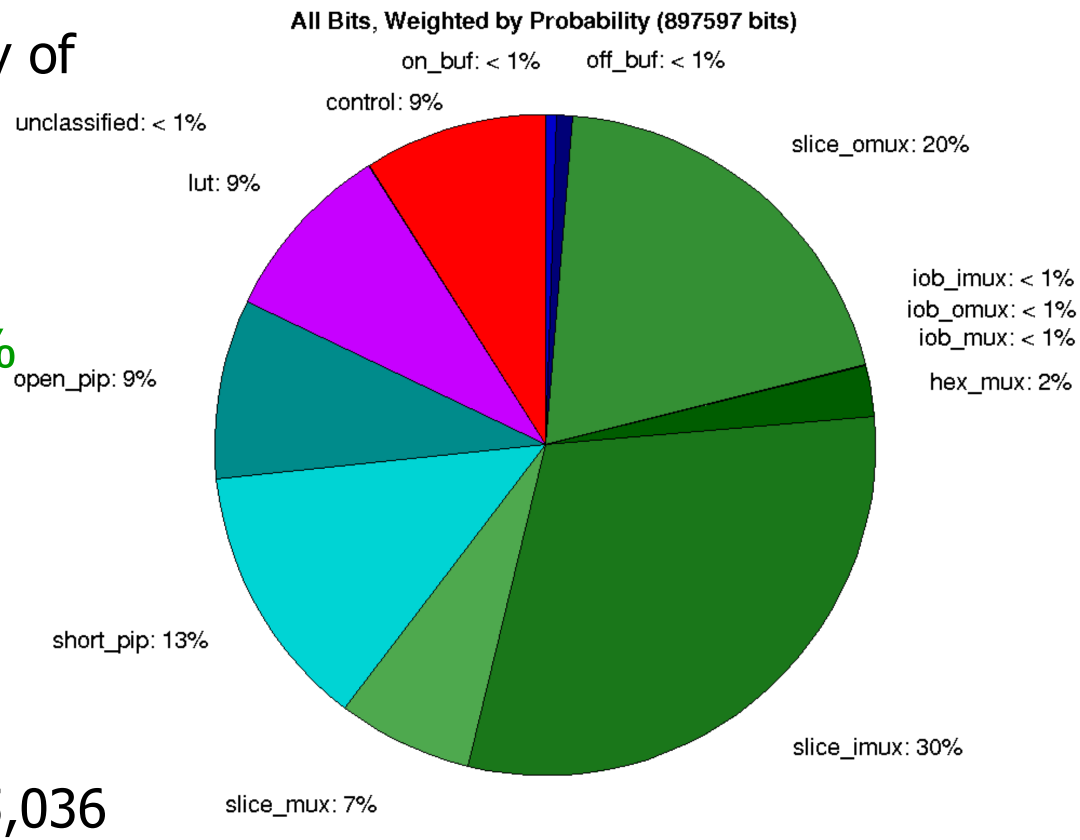
- Routing: 78%
- LUT/Control: 21%

- Total failure bits: 1,175,036



Classification of Failures: Multiply/Add Design (weighted)

- Weighted by probability of failure
- Control upsets: 9%
- LUT upsets: 9%
- Mux select upsets: 59%
- PIP upsets: 22%
- Buffer upsets: <2%
- Unclassified: <1%
- Routing: 82%
- LUT/Control: 18%
- Total failure bits: 1,175,036



Conclusions

- The SEU failure modes for FPGA designs can be complex—more complex than just *stuck-at-1*, *stuck-at-0*, *open*, and *short* failures.
- Mux select change failures dominate the failure types.
  - Muxes are abundant, are often controlled by multiple configuration bits, and are generally affected by a change in any of these bits.
- Eliminating a single class of failures will not lead to an order of magnitude (10x) improvement in reliability.

Future Work

- Low-level, architecture specific mitigation techniques, for example:
  - Use abundant routing resources to create redundant routing
  - Employ unused LUT and slice inputs to provide input redundancy
- Evaluate non-architecture specific SEU mitigation techniques for types of failures

Back-up slides

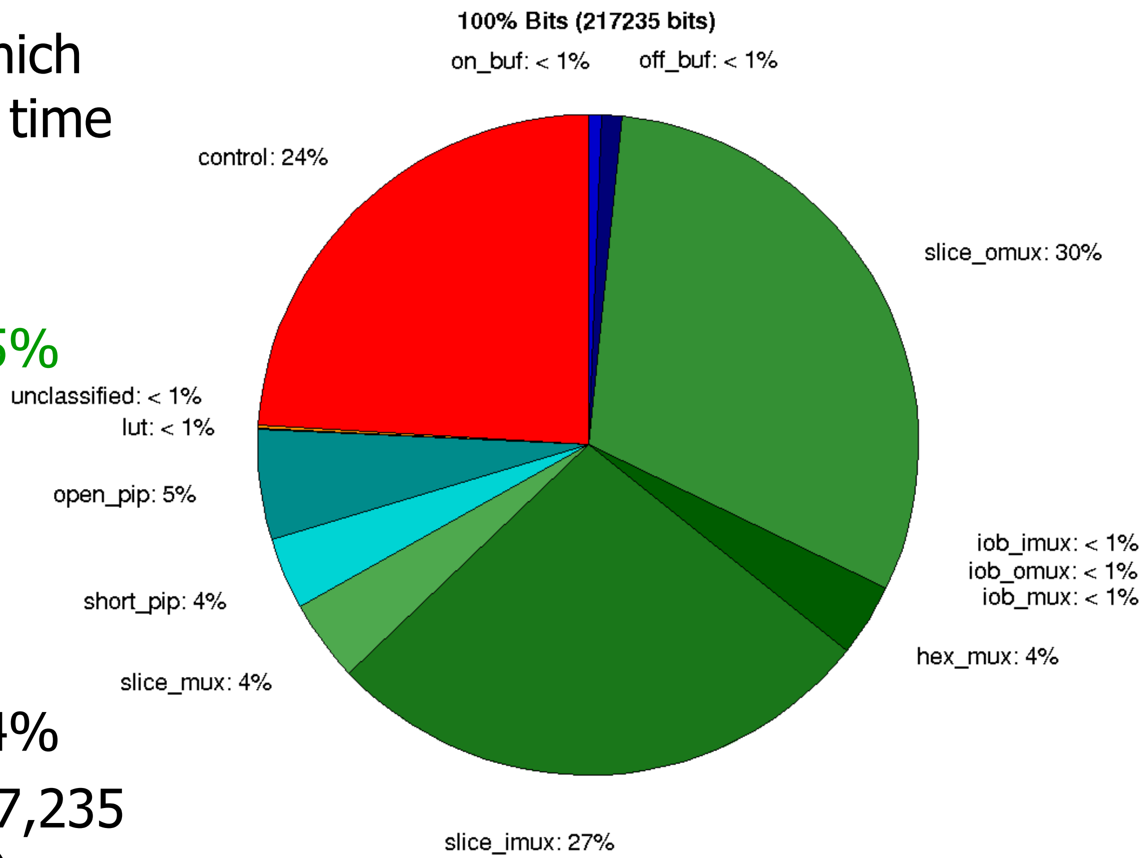
Why Use SRAM FPGAs in Space?

- *Performance*: 100x vs. radiation hardened μP (for fixed volume, power, weight), continuous processing at 100+ MS/s
- *On-orbit processing*: can improve system sensitivity and reduce communication bandwidth
- *On-orbit reprogrammability*: counteract mission obsolescence and on-orbit faults
- *Cost*: cheaper than low-volume ASICs
- *Lead time*: no ASIC design, fab, and test

- Challenge: *SEU sensitivities*

Classification of Failures: 72-bit LFSRs (100% failure bits)

- Distribution of bits which caused failures every time
- Control upsets: 24 %
- LUT upsets: <1%
- Mux select upsets: 65%
- PIP upsets: 9%
- Buffer upsets: <2%
- Unclassified: <1%
- Total Routing: 75%
- Total LUT/Control: 24%
- 100% failure bits: 217,235 out of 392,166 (55%)



Classification of Failures: Multiply/ Add Design (100% failure bits)

- Distribution of bits which caused a failure every time
- Control upsets: 11%
- LUT upsets: <1%
- Mux select upsets: 66%
- PIP upsets: 21%
- Buffer upsets: <2%
- Unclassified: <1%
- Routing: 88%
- LUT/Control: 11%
- 100% failure bits: 705,734 of 1,175,036 (60%)