DSM Memory Map
E. G. Judd
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Memories and Look-Up Tables

Memory Block	Starting Address	Ending Address	Number of Addresses	Data Mask (i.e. valid bits)
Input Buffer 1 Bits 0-15: Channel 0 Input Data Bits 16-31: Channel 1 Input Data	0xYY000000	0xYY03fffc	0x10000 = 2^{16}	0xffffffff
Input Buffer 2 Bits 0-15: Channel 2 Input Data Bits 16-31: Channel 3 Input Data	0xYY040000	0xYY07fffc	0x10000 = 2^{16}	0xffffffff
Input Buffer 3 Bits 0-15: Channel 4 Input Data Bits 16-31: Channel 5 Input Data	0xYY080000	0xYY0bfffc	0x10000 = 2^{16}	0xffffffff
Input Buffer 4 Bits 0-15: Channel 6 Input Data Bits 16-31: Channel 7 Input Data	0xYY0c0000	0xYY0ffffc	0x10000 = 2^{16}	0xffffffff
Look-Up Table 1 Bits 0-15: Channel 0 LUT Bits 16-31: Channel 1 LUT	0xYY100000	0xYY13fffc	0x10000 = 2^{16}	0xffffffff
Look-Up Table 2 Bits 0-15: Channel 2 LUT Bits 16-31: Channel 3 LUT	0xYY140000	0xYY17fffc	0x10000 = 2^{16}	0xffffffff
Look-Up Table 3 Bits 0-15: Channel 4 LUT Bits 16-31: Channel 5 LUT	0xYY180000	0xYY1bfffc	0x10000 = 2^{16}	0xffffffff
Look-Up Table 4 Bits 0-15: Channel 6 LUT Bits 16-31: Channel 7 LUT	0xYY1c0000	0xYY1ffffc	0x10000 = 2^{16}	0xffffffff
NOTE: In some pieces of documentation and test code the Input Memories are referred to as Simulation Memories				
Input Memory 1 Bits 0-15: Channel 0 LUT Output Bits 16-31: Channel 1 LUT Output	0xYY200000	0xYY23fffc	0x10000 = 2^{16}	0xffffffff
Input Memory 2 Bits 0-15: Channel 2 LUT Output Bits 16-31: Channel 3 LUT Output	0xYY240000	0xYY27fffc	0x10000 = 2^{16}	0xffffffff
Input Memory 3 Bits 0-15: Channel 4 LUT Output Bits 16-31: Channel 5 LUT Output	0xYY280000	0xYY2bfffc	0x10000 = 2^{16}	0xffffffff
Input Memory 4 Bits 0-15: Channel 6 LUT Output Bits 16-31: Channel 7 LUT Output	0xYY2c0000	0xYY2ffffc	0x10000 = 2^{16}	0xffffffff
Output Memory	0xYY300000	0xYY33fffc	0x10000 = 2^{16}	0xffffffff
Engine Registers	0xYY340000	0xYY34007c	0x20 = 32 (max)	0xffff
Engine Configuration Memory	0xYY400000	0xYY5ffffc	0x80000 = 2^{19}	0x1
Registers (see below)	0xYY600000	0xYY600030	0xd = 13	See below
Block Transfer Registers	0xZZ000000	0xZZ000008	N/A	See below

Control and Status Registers (CSRs)

ID: Name	Address	Functionality	Access
1: Operation Control	0xYY600000	D0: Put DSM in Run (1) or Load (0) Mode D1: Enable Output FIFO	Read/Write
2: First/Last Specification	0xYY600004	D0: Set DSM to be first in the chain block transfer D1: Set DSM to be last in the chain block transfer	Read/Write
3: Input/Output Memory Configuration	0xYY600008	D0: Enable Input Memory D1: Enable Output Memory D2: Set Input Memory to play (1) or record (0) D3: Set Output Memory to play (1) or record (0)	Read/Write
4: Output FIFO	0xYY60000c	D0-D31: Engine FPGA output.	Read Only
5: FIFO Reset	0xYY600010	D0: Reset (i.e. clear) output FIFO	Write Only
6: Load FIFO Blanks	0xYY600014	D0: Load one blank into the output FIFO	Write only
7: Local Address Control	0xYY600018	D0: Copy the current value of the local address counter into CSR8 D1: Reset the local address counter to zero. D2: Increment the local address counter by one.	Write Only
8: Read Local Address	0xYY60001c	D0-D15: Current value of local address counter	Read Only
9: Board Connected Status	0xYY600020	D0: Channel 0 cable plugged in D1: Channel 1 cable plugged in D2: Channel 2 cable plugged in D3: Channel 3 cable plugged in D4: Channel 4 cable plugged in D5: Channel 5 cable plugged in D6: Channel 6 cable plugged in D7: Channel 7 cable plugged in	Read Only
10: FPGA and FIFO Status	0xYY600024	D0: Address Control FPGA configured D1: Engine FPGA configured D2: Output FIFO empty D3: Output FIFO full	Read Only
11: Begin FPGA Configuration	0xYY600028	D0: Instruct Address Control FPGA to configure the engine FPGA	Write Only
12: Software LEDs	0xYY60002c	D0: Switch LED 0 On/Off D1: Switch LED 1 On/Off D2: Switch LED 2 On/Off D3: Switch LED 3 On/Off	Read/Write
13: Strobe Reset	0xYY600030	D0: Reset the internal strobes on all FPGAs	Write Only

Block Transfer Registers

Name	Address	Functionality	Access
L1 Data Latch	0xZZ000000	D0-D15: Address of data in Input Buffers that is to be copied into the L1 Registers	Write Only
L1 Register	0xZZ000008	D0-D63: Data latched from input buffers. NOTE: These registers can only be accessed during a VME64 block read	Read Only