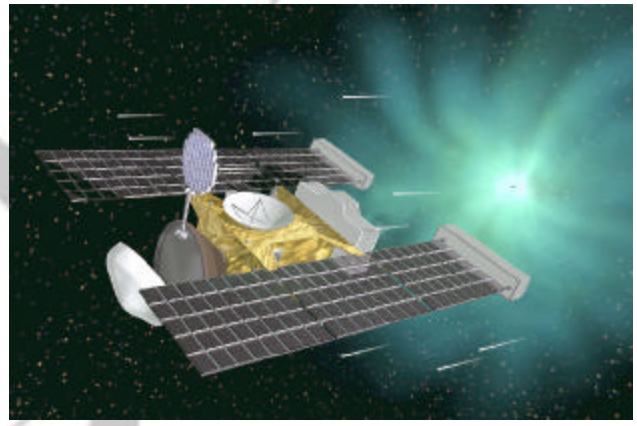

BAE SYSTEMS

Advanced Microprocessor Technologies and Challenges for Space Applications

Nadim F. Haddad

(nadim.haddad@baesystems.com)

2001 IEEE Microelectronics Reliability and Qualification Workshop

December 11-12

Pasadena, CA

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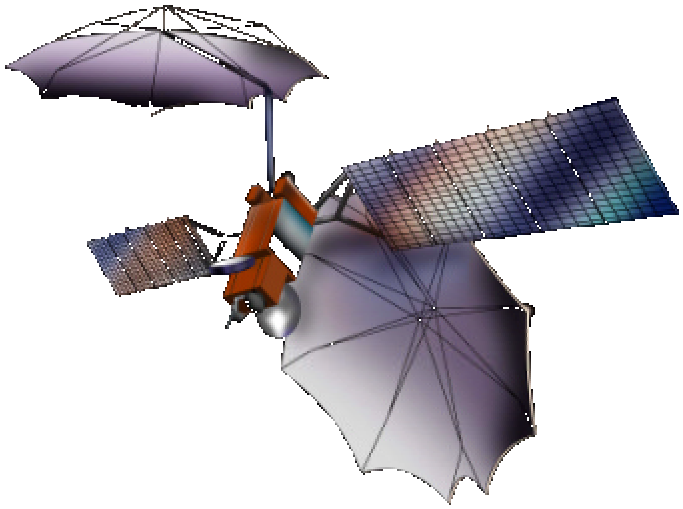
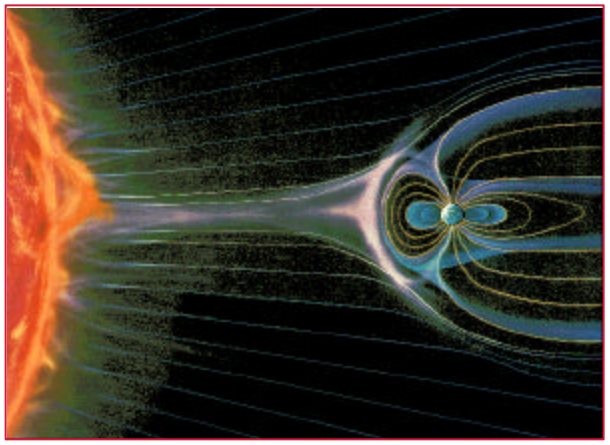


Agenda

- The Environment
- Effect of Technology Migration
- Mitigation Schemes and Penalties
- Radiation Hardened Processors for Space
- Space Processor Roadmap
- Conclusion



Nikkei Science, Inc. of Japan, by K. Endo

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Agenda

- **The Environment**
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- **Conclusion**

Variations in Radiation Flux Density

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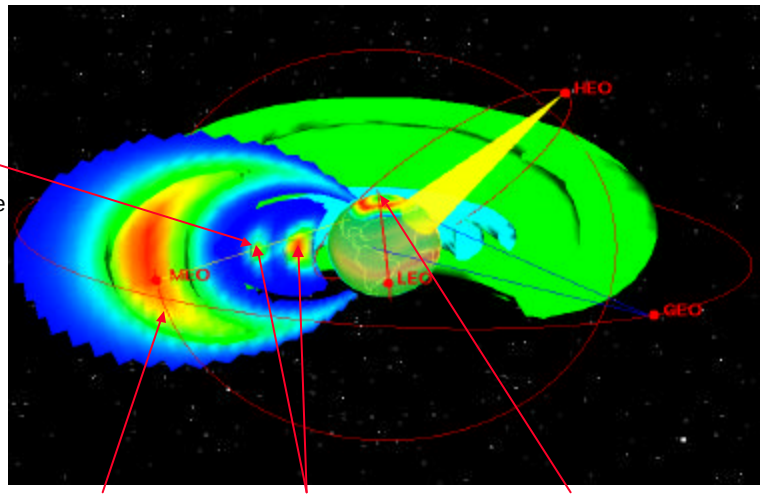
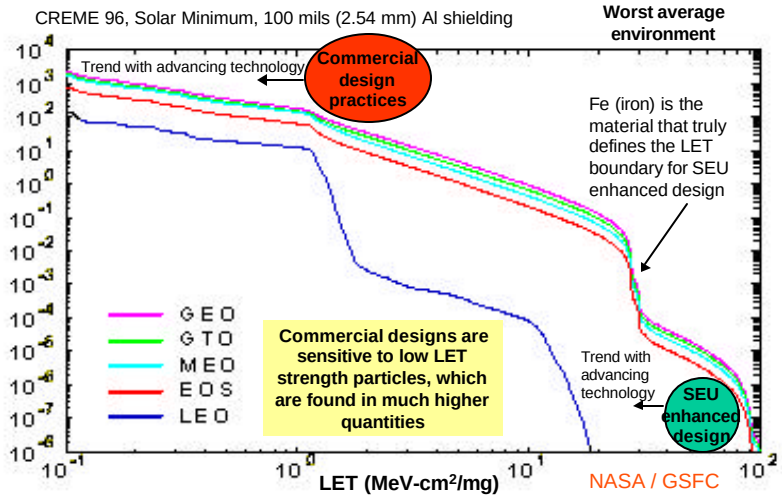


"Storm belt" - highly variable

Electron belt - in the path of the MEO orbits

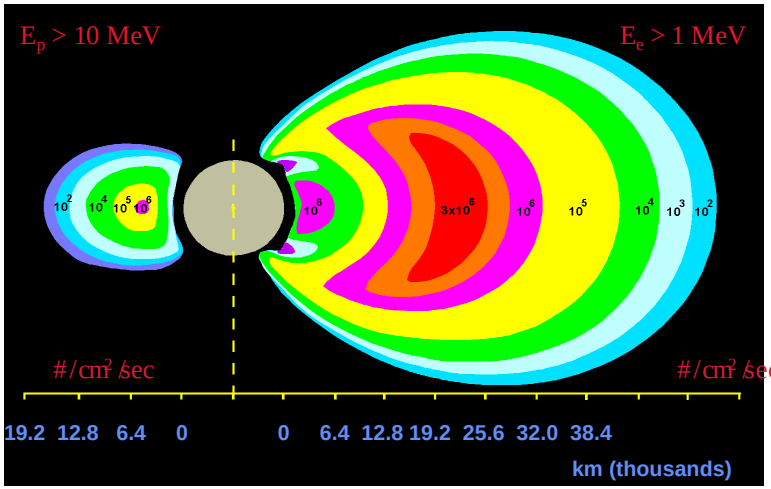
Proton / electron belts - in some of the LEO orbits

Funneling of magnetic fields at poles increases radiation in polar orbits

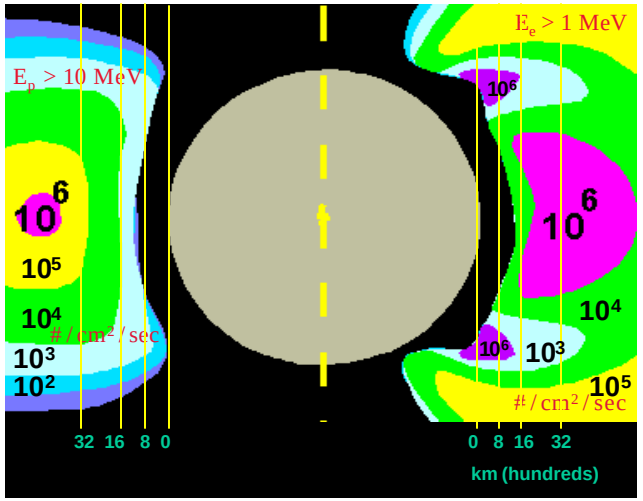


AP (proton) -8 Model

AE (electron) -8 Model



PROTONS (SEU and Total Dose)



ELECTRONS (Total Dose)

Proton & Electron Average Models

NASA / GSFC

NASA / GSFC

Variability of radiation environments affects the applicability of COTS in space

Extreme Conditions - Solar Flares

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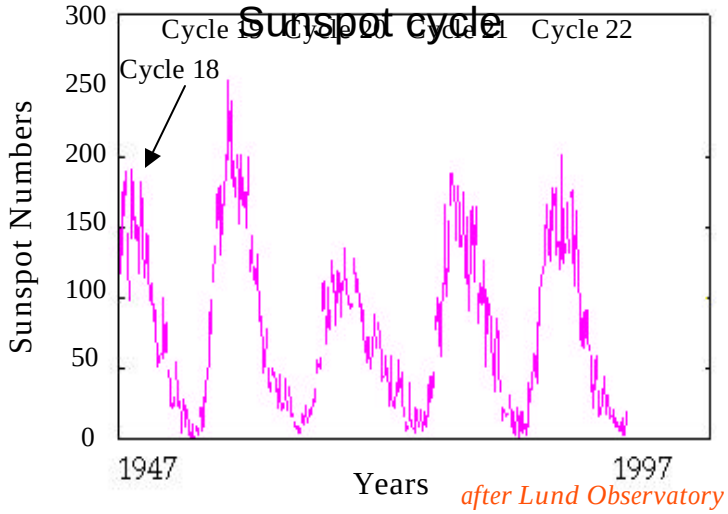
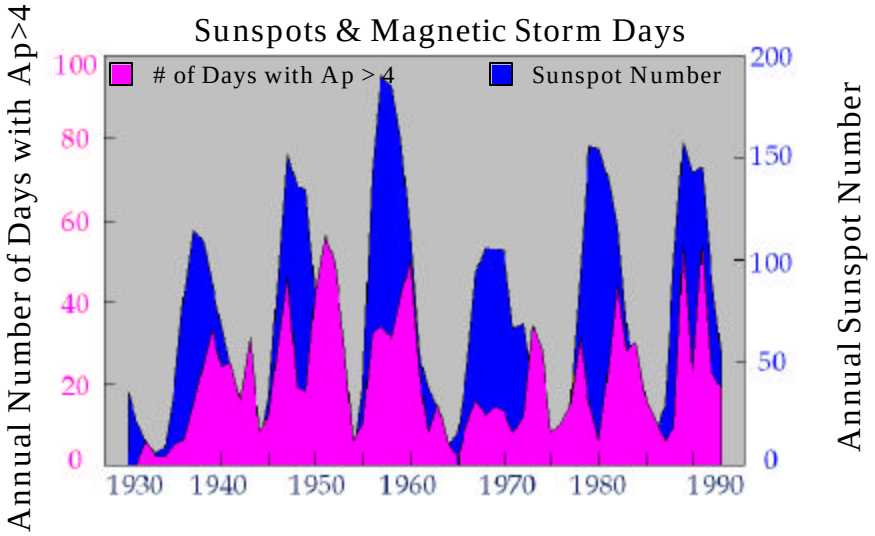
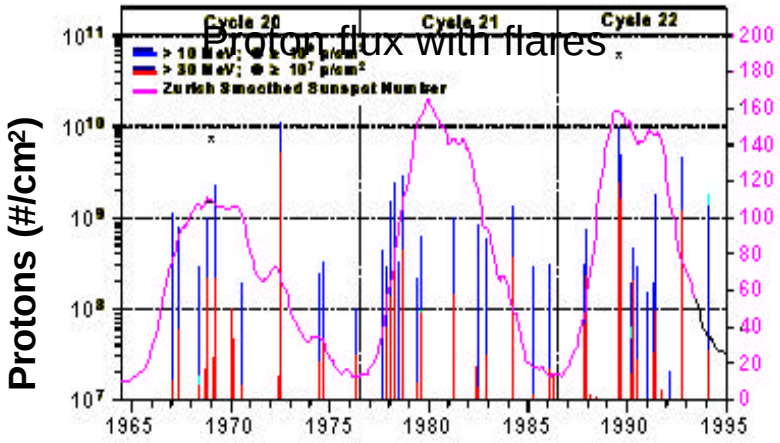
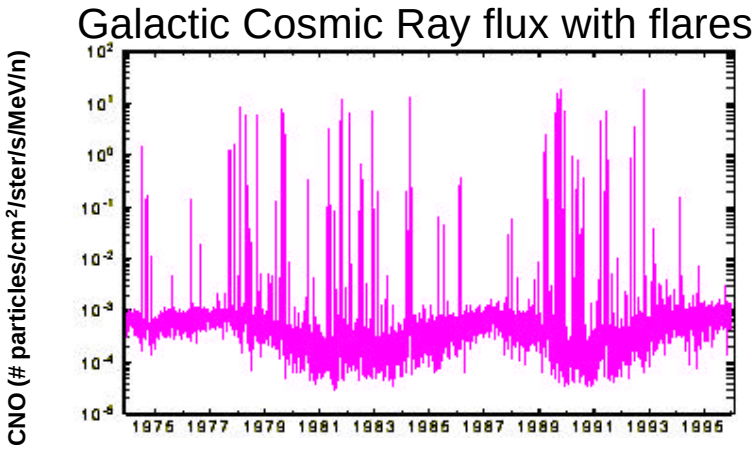








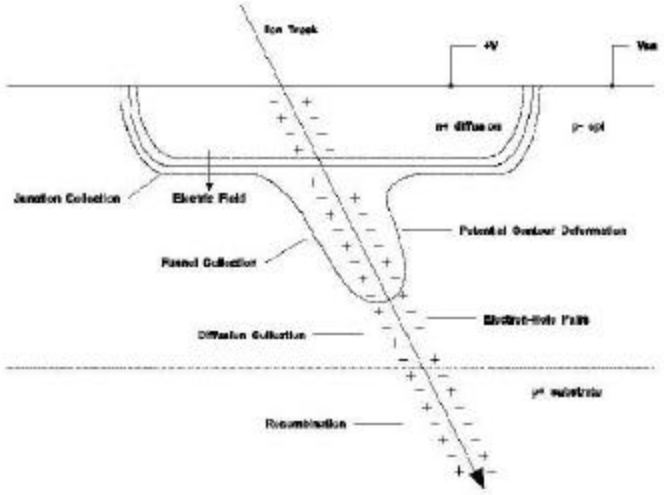
NASA / GSFC

Space environment is very variable - solar flares are unpredictable and create a severe environment

Issues Associated with Space

BAE SYSTEMS

- Radiation environment
  - **Total Ionizing Dose** (TID) - accumulation of radiation over time
  - **Prompt Dose** - ability to function during a massive burst of radiation
  - **Survivability** - ability to function after a massive burst of radiation
  - **Single Event Effects** (SEE) - soft or hard errors as the result of the penetration of a single charged particle
    - **Single Event Upset** (SEU) - state change of a storage node
    - **Single Event Transient** (SET) - pulse injection into combinational logic
    - **Single Event Gate Rupture** (SEGR) - destruction of the gate of a transistor
    - **Single Event Latchup** (SEL) - "lock-up" of a device; must remove power to reset
    - **Single Event Burnout** (SEB) - Burnout, especially in power devices
- Wide temperature range and stresses
- High reliability
- Mechanical stresses
- Severe mass and power constraints



Charge from single event impact

Spacecraft electronics are expected to overcome severe environmental conditions

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Trends in Commercial Technology

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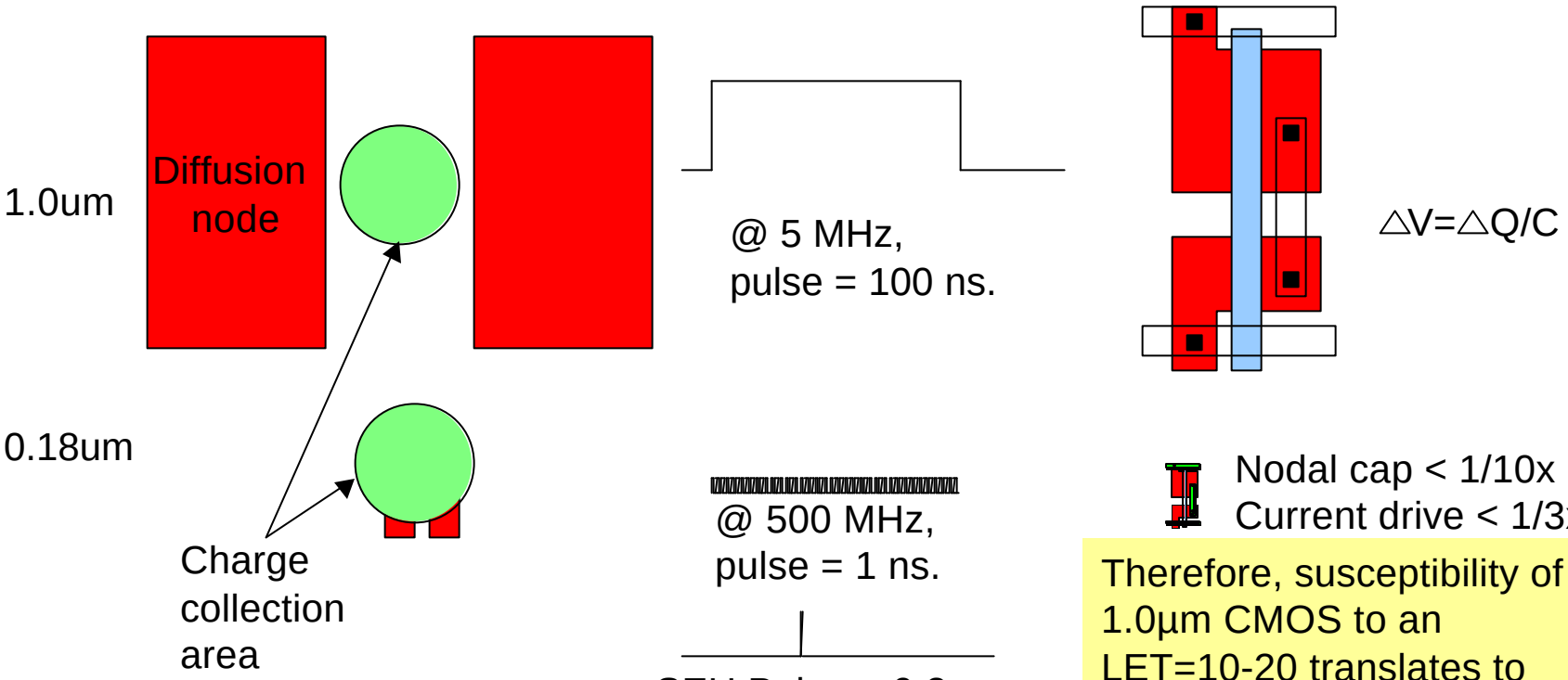
	Commercial CMOS Technology							Typical Rad Hard
Environment	0.8 μm	0.5 μm	0.35 μm	0.25 μm	0.18 μm	0.13 μm	0.18 μm SOI	
Total Dose (Krad(Si))	10 - 20	20 - 40	20 – 50	40 - 100	40 - 150	40 – 150	30 – 50	200 – 1,000
SEU (u/b-d) (90% W.C. Geo)	1E-7	1E-6	2E-6	5E-6	1E-5	>1E-5	1E-6 to 1E-7	< 1E-10
Prompt Dose Upset (rad/s)	1E7	1E7-1E8	1E7-1E8	1E7-1E8	1E7	<1E7	1E8	> 1E9
Latch up	Generally prone	Some prone	Some prone	Generally immune	Generally immune	?	Possibly self-latch	Immune
Neutron (u/cm^2)	1E14 (limited by TID)	1E14 (limited by TID)	1E14	1E13-1E14	?	?	?	1E14

Trends in commercial technologies have not always been favorable for spaceborne application, given the various failure mechanisms

Effect of Scaling on Single Event Upset

BAE SYSTEMS

SIZE ***DURATION*** ***STRENGTH***

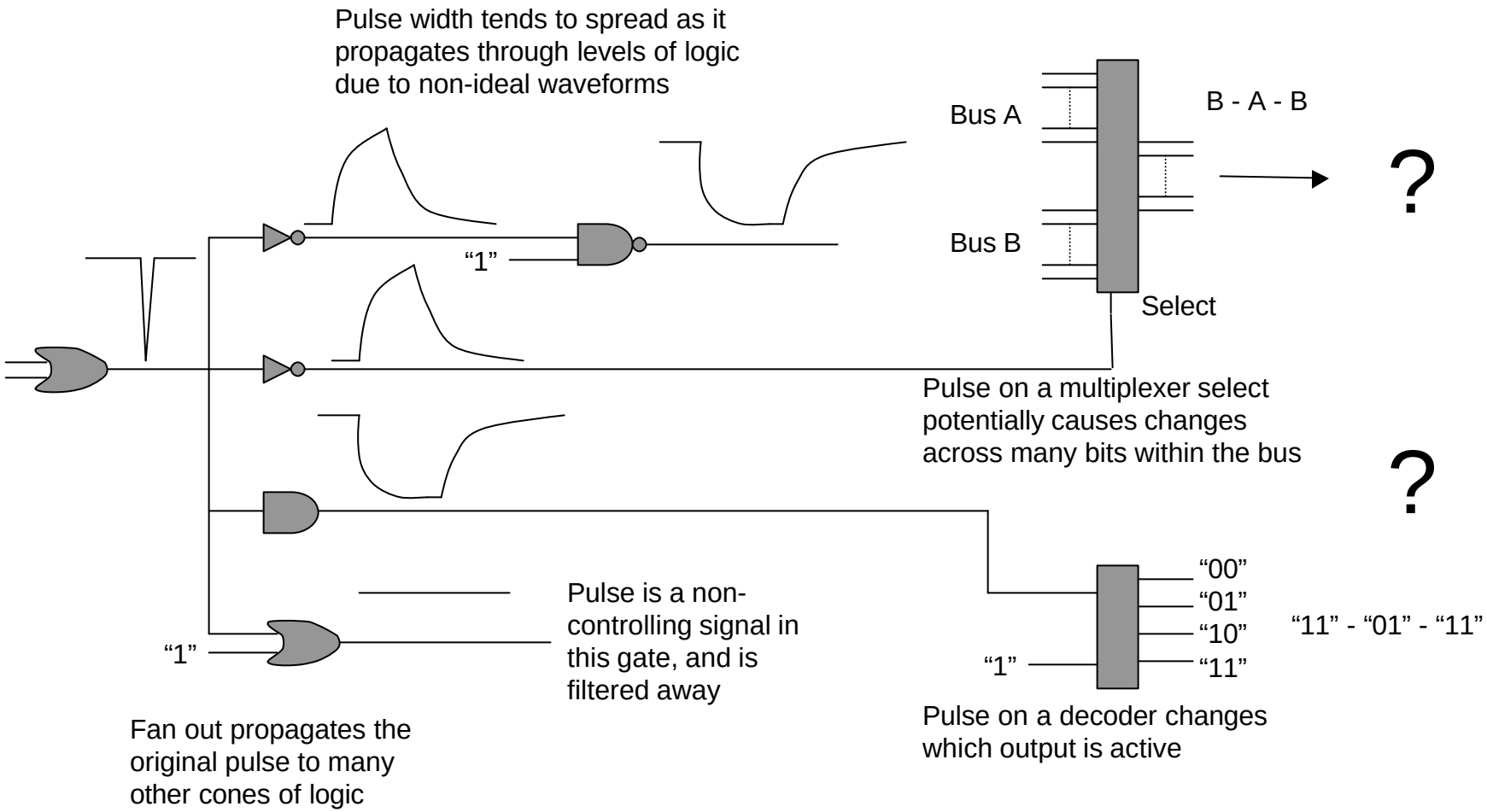


Therefore, susceptibility of 1.0µm CMOS to an LET=10-20 translates to susceptibility of 0.18 µm CMOS to an LET = 0.3-0.7

Technology scaling is driving a multi- exponential increase in sensitivity to SEU / SET

Single Event Transient (SET)

BAE SYSTEMS

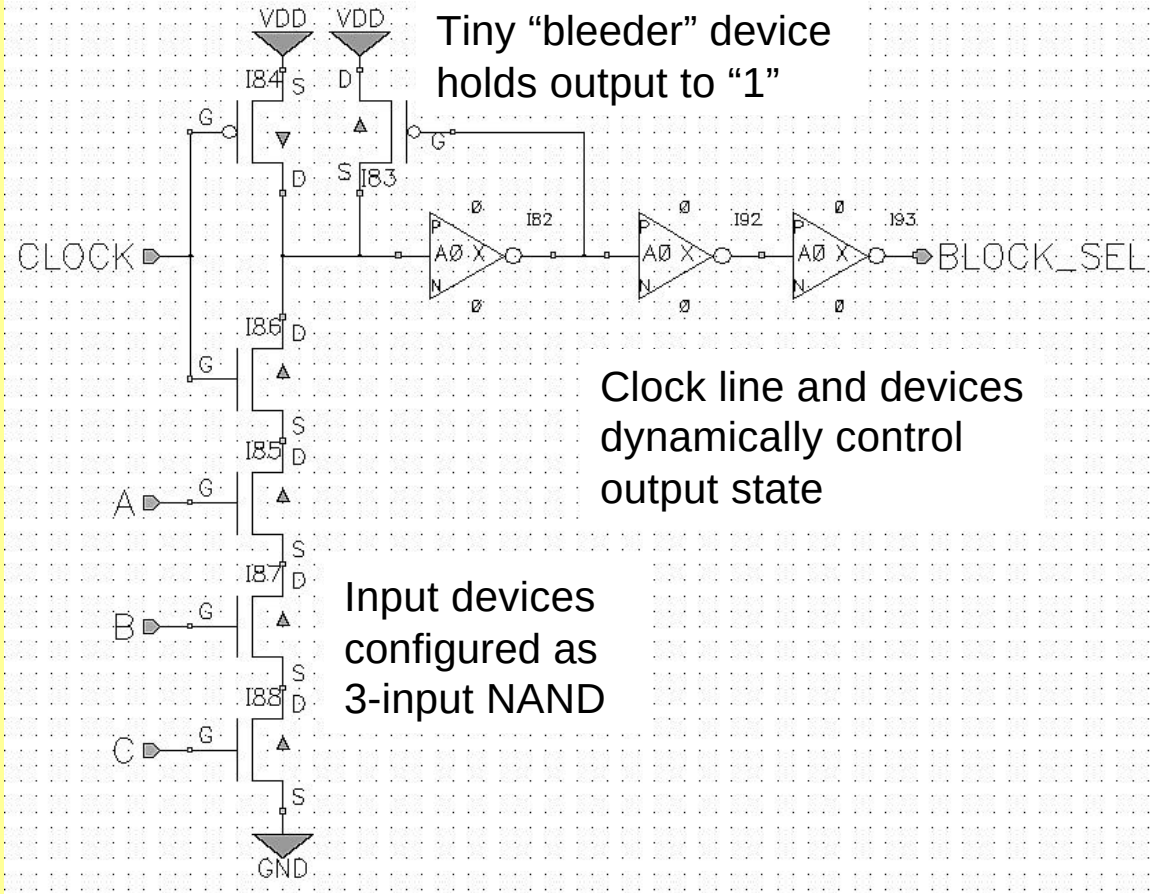


An injected pulse can propagate far beyond it's point of inception, based on logic design paths

SEU Susceptibility in Dynamic Circuitry

BAE SYSTEMS

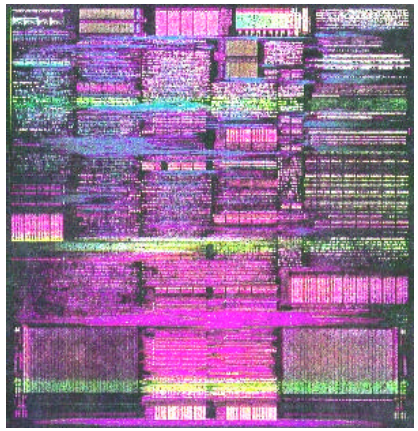
- Global block select decoder
- Classic pre-charged dynamic circuit used in: decode, buffers, datapaths, logic, and clocks
- Operation:
  - CLOCK = “0” results in output pre-charge to “1”
  - CLOCK = “1” results in valid signal output, based on input conditions
- Very soft, due to:
  - Small bleeder device holding “1” state
  - Switching due to SET pulse on clock line
- Upset will select wrong block of data (1 block = 32K bits)



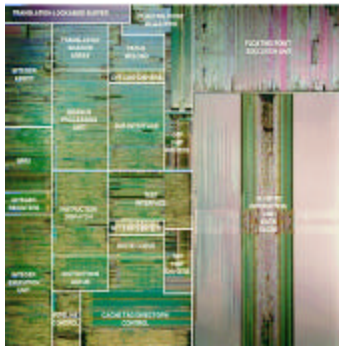
Exotic circuit design techniques (common in recent COTS products) increase density and performance, but are more susceptible to SEU/SET

Estimated SEU Rates by Commercial Processor Generation

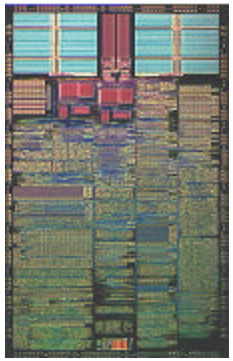
BAE SYSTEMS



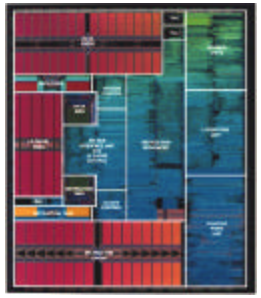
RSC - “G0(?)”



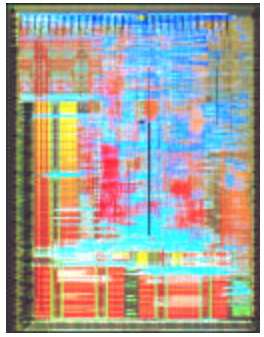
601 - “G1”



603 / 603e - “G2”



750 - “G3”



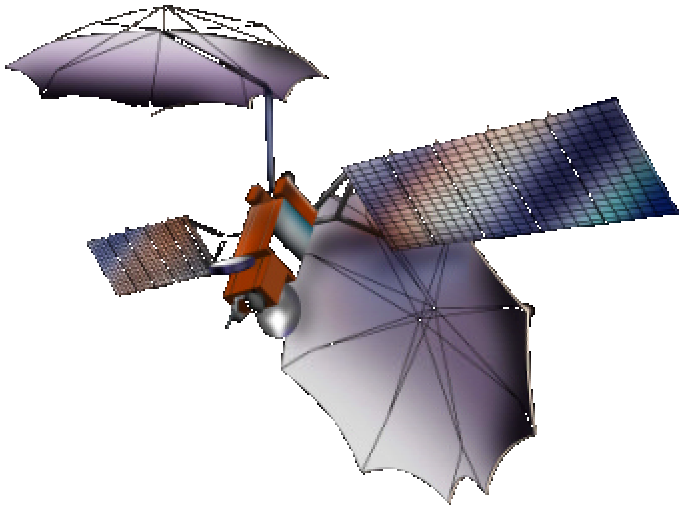
7400 - “G4”

	RSC - “G0(?)”	601 - “G1”	603 / 603e - “G2”	750 - “G3”	7400 - “G4”
Technology:	0.8 µm	0.6 µm	0.5 / 0.35 µm	0.25 µm	0.18 µm
Transistors:	1.0 M	2.8 M	1.6 / 2.6 M	6.4 M	10.5 M
Supply:	3.6 V	3.6 V	3.3 V / 2.5 V	2.5 V	1.8 V
Speed:	33 MHz	50 MHz	80 MHz / 200 MHz	266 MHz	450 MHz
Released:	1992	1993	1994 / 1995	1997	1999
Estimated SEU Rate					
90% GEO:	**1 / 60 days**	**1 / 8 days**	**1 / 5 days / 1 / day**	**1 / hour**	**3 / hour**
During Flares:	**0.02 - 2 / min**	**0.1 - 9 / min**	**0.2 - 14 /min / 1 - 100 / min**	**0.3 - 27 / sec**	**1 - 100 / sec**

* SET upsets begin to increase at 0.35 micron and then accelerate, due to small devices, low supply, and high clock rates

Across Generations, the Increase in SEU/SET Susceptibility is Dramatic

BAE SYSTEMS



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Total Dose Mitigation

BAE SYSTEMS

Total Dose Environment for Various Orbits
(10 Year Mission Assumed)

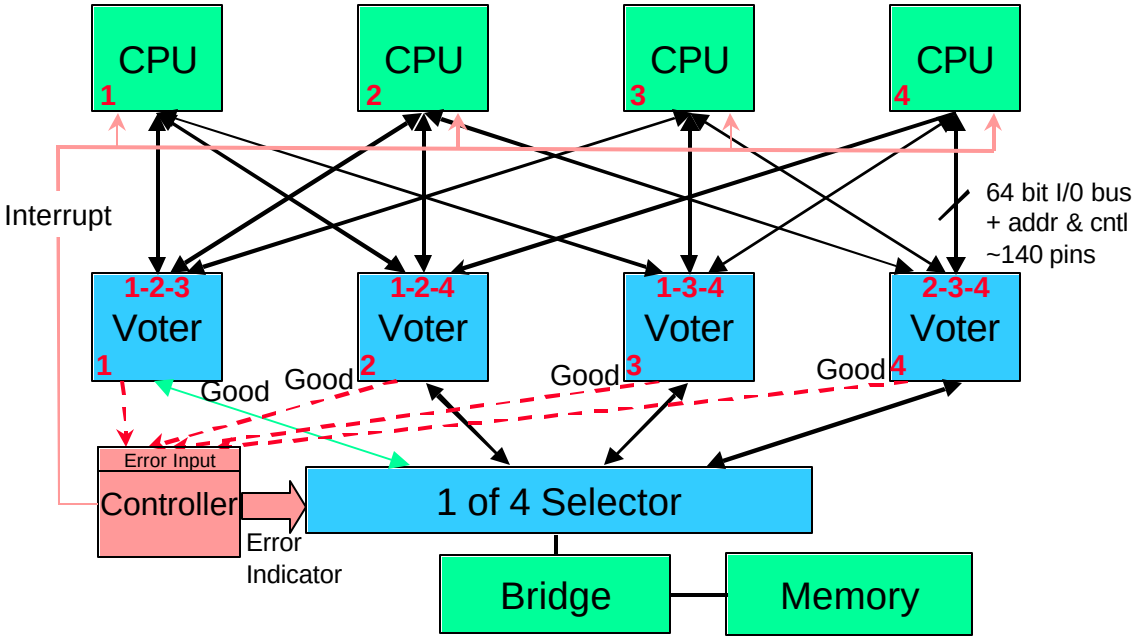
Orbit		Total Dose (krad(Si))	
Altitude(Km)	Inclination(Degree)	100 mil Al	250 mil Al
850	28	22	12
1,350	90	56	38
1,400	53	130	50
1,500	30	240	100
Geo	00	400	20
1/2Geo	60	3,000	100

Shielding is an effective way to reduce total dose, but it comes at a cost… It is also ineffective in mitigating single event effects

SEU Mitigation - Redundant System Example

BAE SYSTEMS

- **Hardware redundancy functions**
  - Multiple voting functions check the CPU outputs, confirming correct results or identifying the “bad” CPU
  - If a fail is detected:
    - The controller uses that information to shut down (hard reset) the failing CPU
    - Begins recovery routine
  - The selector sends good output to the I/O and/or memory
  - Approximately two cycles of latency are added to I/O and memory operations



- **Software redundancy functions**
  - Regular “sweep” issued to cause output for checking
  - Either clears key embedded memories (caches, branching) during each regular sweep, or during a recovery operation
  - Match up the processors at a “work task” boundary, and start simultaneous processing again

Redundant systems operate by detecting errors in processing functions after they occur and removing them through voting

Applicability of Redundant COTS Electronics in Space

BAE SYSTEMS

Orbital variations

- Low LEO is the most benign (below 800 km)
- Polar - more severe than near equatorial

- Upper LEO is more severe for both Total Dose and SEU
- The South Atlantic Anomaly is the worst case in LEO orbits

- MEO is worst for Total Dose
- GEO is worst for Cosmic Rays

- Long term missions encounter extreme conditions at some point (solar flares and coronal mass ejections); these conditions REQUIRE SEU immune design - ***redundancy is not applicable***

Application variations

- Short term applications *(example: shuttle)* may be timed around extremes
  - Some unpredictability exists
  - Some years are better than others

- Applications that can accept outages (1-4 days in length) can simply shut down during solar flares *(example: geology, telescope)*

- New ASIC designs can address some of the problem in design
  - TMR at each latch
  - Error correct embedded memories
  - Addressing SET errors is more difficult

- Real time / critical applications have a problem; they CAN'T shut down *(example: cell phone, internet, video, weather, global positioning, military)*

The Ability to Consider TMR is a Function of Both Orbit and Application

Redundant Modern Commercial Processors in Space

BAE SYSTEMS

Size, weight, and power (SWAP)

- **Size**
  - TMR requires **significant board space**
    - 3-4 CPUs
    - Voting Chip
  - **Will not fit** on a 3U format
- **Weight**
  - About **2X weight** of Single Processor Solution
- **Power**
  - Increased **Component Count**
  - **Increased processing** for upset checking / recovery
  - About **3X Power**

Software effort and overhead

- **Effort**
  - **"Upset checking" routine**
  - **Split application code** for regular checking
  - **Recovery** routine
- **Overhead**
  - Interrupted processing
  - Increased check pointing
- **50% Performance loss Typical**

  (through HW & SW)

SEU / SET susceptibility

- **Upset mechanisms**
  - **Dynamic logic**
  - **Storage nodes**
  - Transient **(SET)** propagation
- **Flux rate**
  - **GCR** Cause **1-2** upsets / hr
  - **Protons** at LEO cause **0.3-0.7** upsets / hr
  - **Solar flares** cause **0.1 - 20 upsets / sec**
- **Recovery**
  - **TMR recovery** will typically **require several minutes**
  - Upsets **may not be detected** in time to respond
  - Expect **trouble during flares**

Product cost

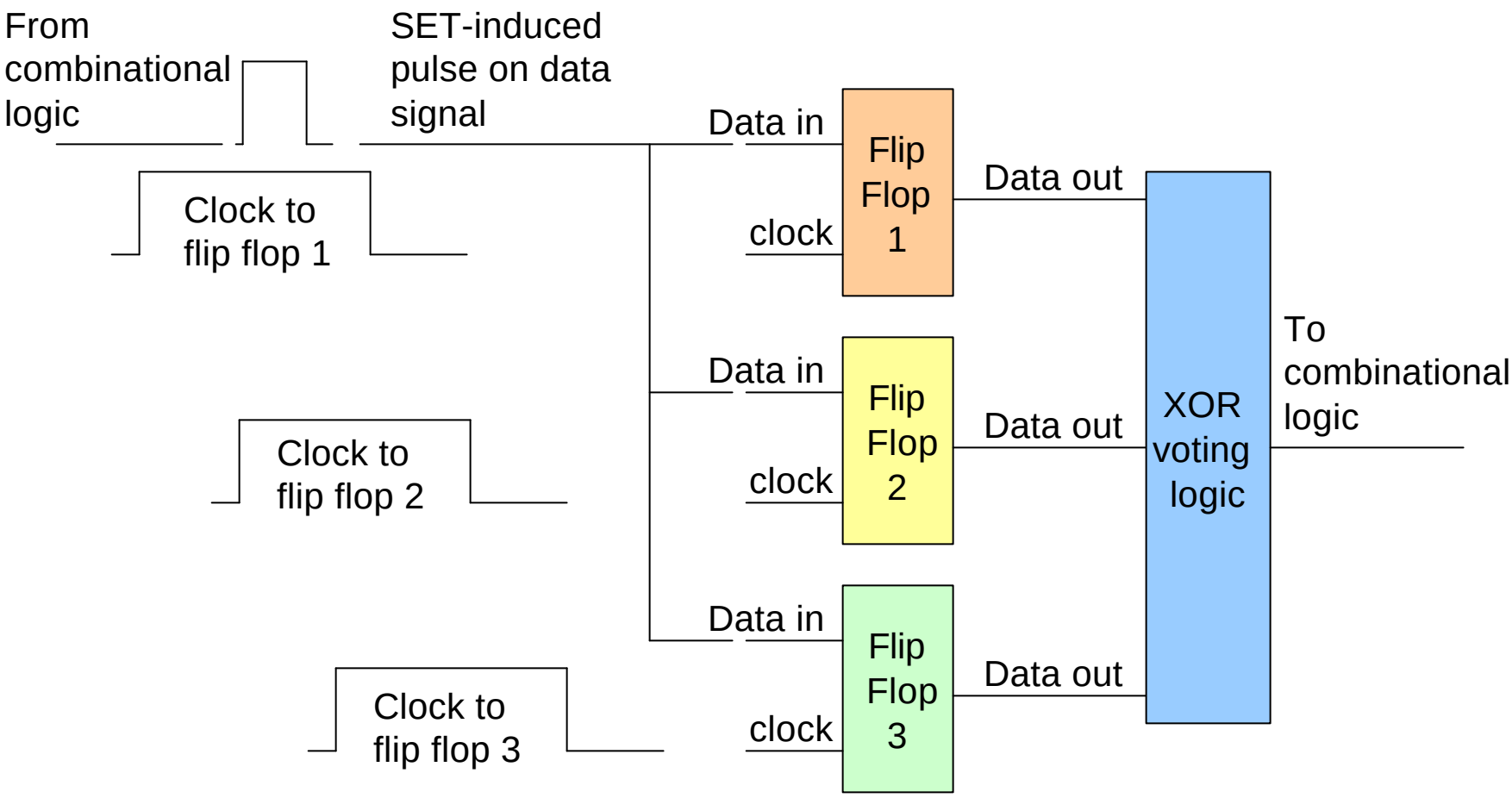
- **Component costs**
  - **Rad-hard voting chip** has high recurring cost in addition to NRE
  - Commercial CPUs have cost advantage
- **Software costs**
  - **NRE for development** of checking and recovery routines
  - **Board costs**

    More complex board design with lead time vs. a standard rad-hard product

Commercial Processors, Even with Redundancy, Have Issues and Exposures that Far Outweigh their Benefits Compared to Enhanced Processor Solutions

SEU Mitigation - Redundant Circuitry Example

BAE SYSTEMS

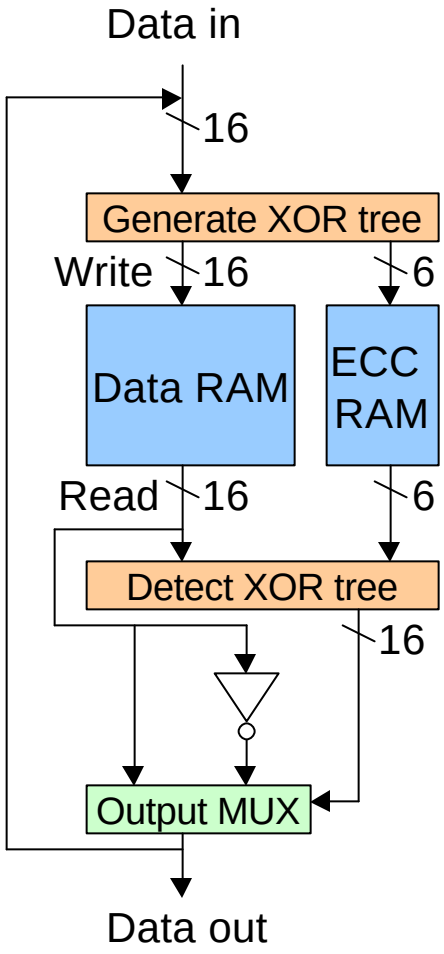


Redundant storage cells with time shifted clocks fight SET upsets by attempting to filter out the pulse prior to capturing it

SEU Mitigation - In-line Error Correction

BAE SYSTEMS

- Typical uses
  - Memory subsystems
  - Communication links
- Sequence for Single Error Correct Double Error Detect (SECDED):
  - Generate error bits via XOR based on masking
  - Detect error via XOR with masking
    - No mismatch indicates good data
    - Valid value identifies bit in error
    - Invalid value defines uncorrectable errors
  - Multiplex data or inversion bit-by-bit to correct
- Radiation mitigation:
  - Employ variable rate “scrubbing” (read, test, correct and write back if needed) sequence at varying rates, based on rate of errors induced
  - Useful until error rate exceeds ability to fix or ability to perform both function and correction
  - Combination with hardened Cache reduces functional access demand



Error correction removes errors that occur within stored memory by generating codes that uniquely identify the validity of each bit of data

SEU Mitigation - Hardened Circuitry Example

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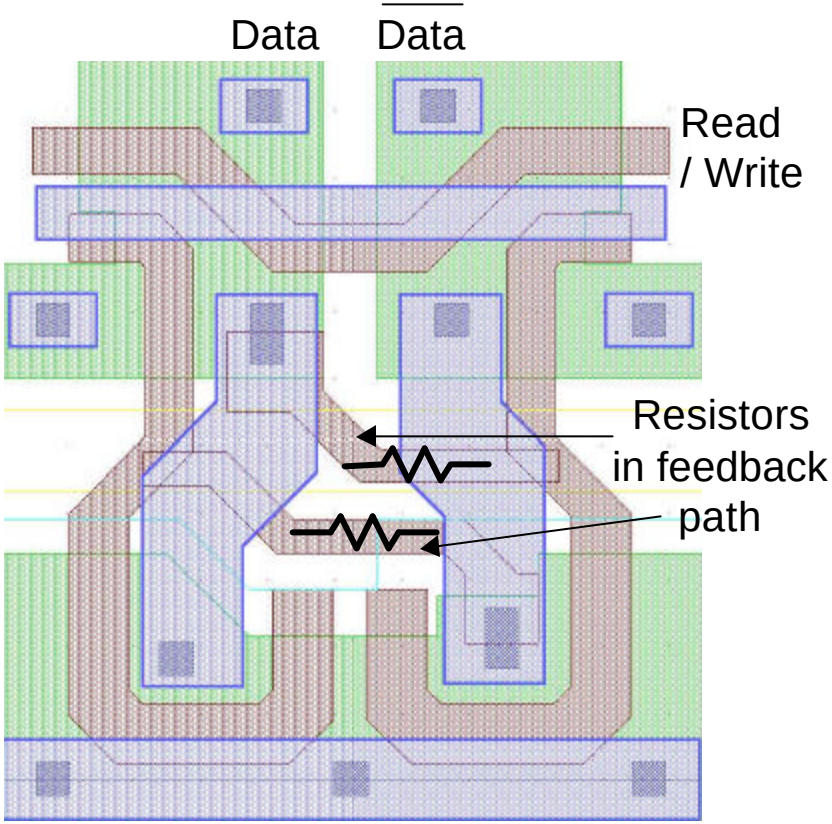
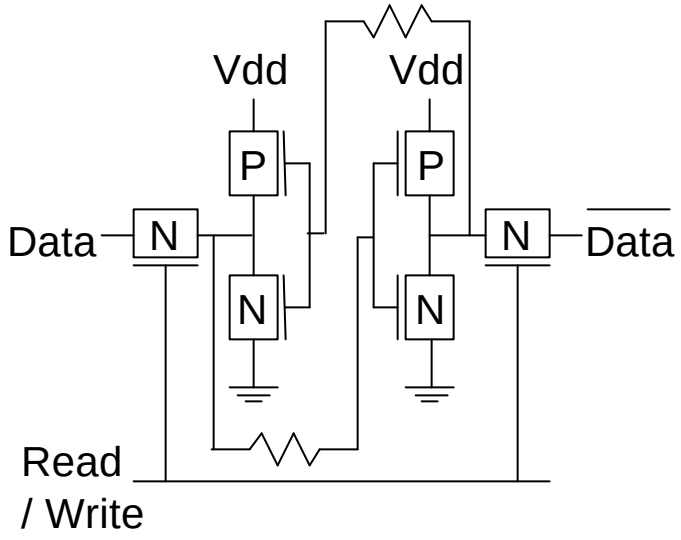
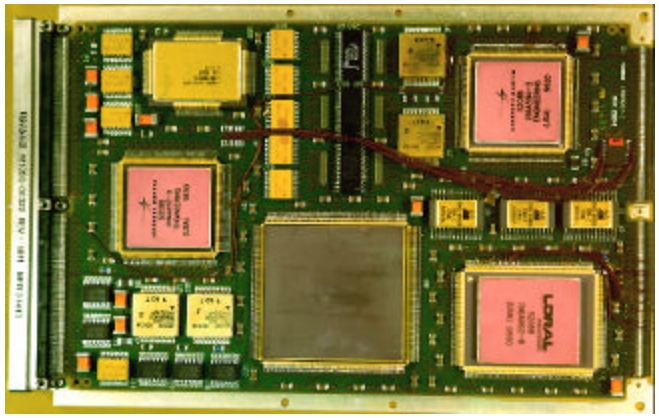




- Large resistance in the feedback path fights state change in the cell via RC time constant
- Typically employs unique manufacturing process steps
- Adverse effects on Write time and circuit density

Radiation hardened circuits prevent upsets through design techniques that fight against the charge deposit from the impact



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90 satellites currently on orbit with 286 single board computers*

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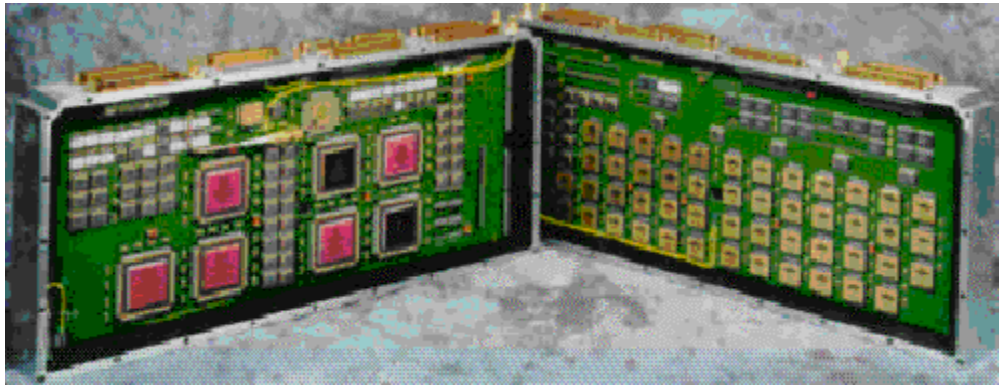
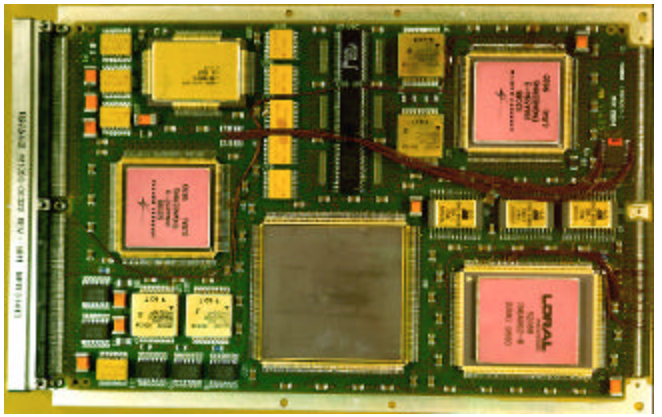
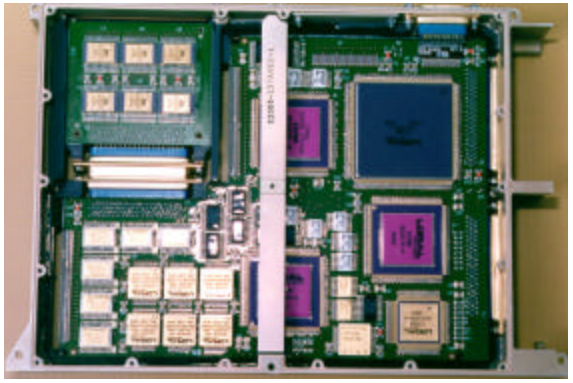
* As of November 30, 2001



Cassini GVSC processor

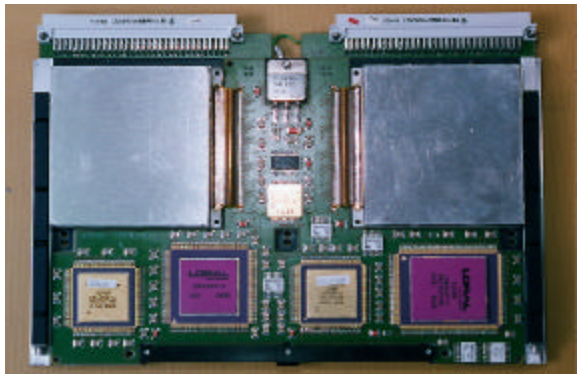


SBIRS Low/Orbview RAD6000™



CCP drop in tray (GVSC)

Over 500 flight boards delivered or ordered for new launches through 2006



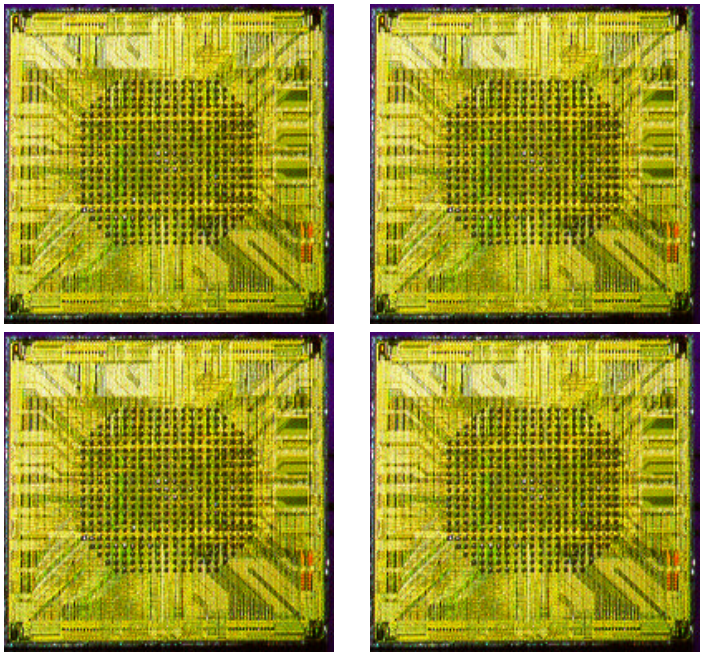
VME 6U RAD6000™ board *

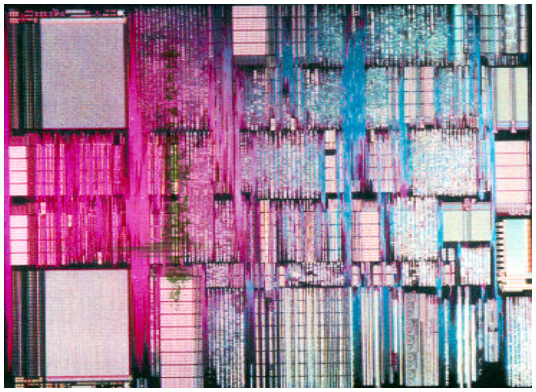
* as used on FHLP

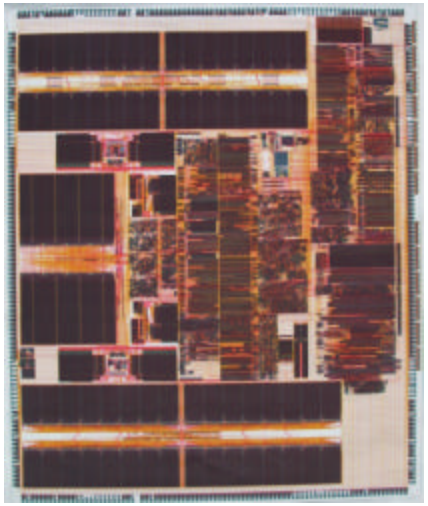
Our processors have been the standard in space for many years, with millions of hours of flawless operation in a variety of applications

Three generations of radiation hardened microprocessors

BAE SYSTEMS







1991
GVSC 1750
1.0 µm Radiation Hardened CMOS
- **MIL-STD-1750A architecture**
- **4 by 88 sq mm**
- **0.3 M transistors**
- **20 MHz**
- **3 MIPS**

1996
RAD6000™
0.5 µm Radiation Hardened CMOS
- **RS/6000 "Power" architecture**
- **145 sq mm**
- **1.1 M transistors**
- **33 MHz**
- **35 MIPS**

2001
RAD750™
0.25 µm Radiation Hardened CMOS
- **PowerPC architecture family**
- **130 sq mm**
- **10.4 M transistors**
- **133 - 166 MHz** ***(up to 200 as available)***
- **240 - 300 MIPS** ***(up to 366 as available)***

The RAD750 represents our third generation product, with architectural and technological enhancements that improve power/performance

RAD750™ - Power PCI
RAD6000™ architecture compatibility

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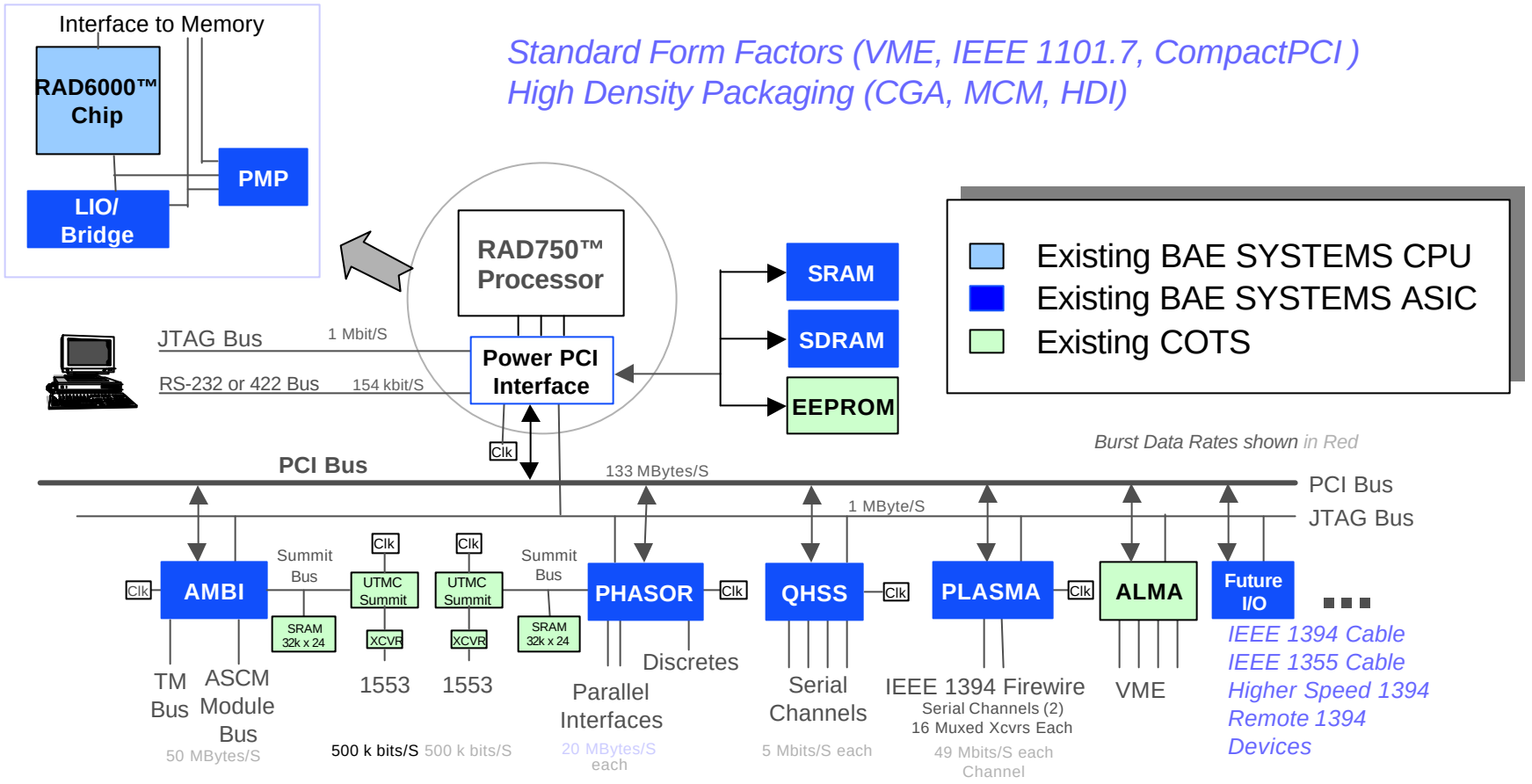

The RAD750™ and Power PCI easily replace the current RAD6000™ and LIO in our processor board architecture

RAD750™ specifications

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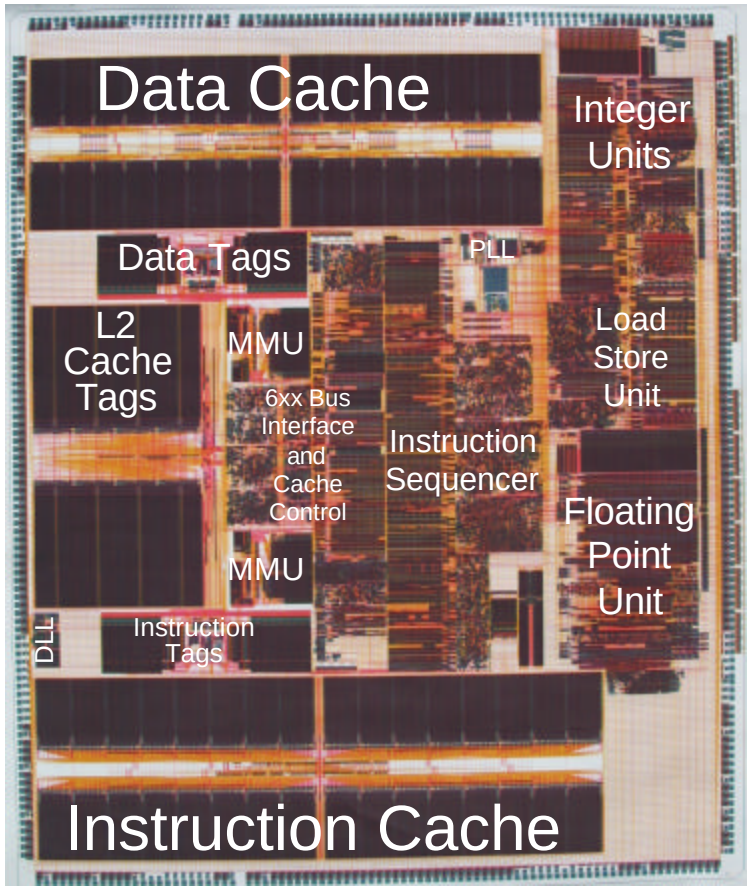
Specifications	
Processor Speed	110 to 133 MHz
Process Technology	0.25 um (0.18 um Leff) CMOS, 6 levels of metal
Die Size	10.4 mm. by 12.5 mm.
RAD750™ Performance ***without L2 (est)*** ***with 1MB L2 (est)***	6.5 SPECint95 3.9 SPECfp95 @ 150 MHz. 7.0 SPECint95 4.7 SPECfp95 @ 150 MHz.
Signal I/O	256 (including L2 port)
Power Supply	2.5 V + / - 5% core 2.5 or 3.3 V + / - 10% I/O
Power Dissipation	5.0 watts at 133 MHz, 2.5V
Temperature Range	-55ºC to +125ºC
Packaging	25.0 mm. by 25.0 mm. by 6.22 mm. 360 pin Column Grid Array (CGA)
Mass	9.0 grams
Radiation Hardness	Total Ionizing Dose: 200 Krad (Si) SEU: 1E-10 upsets / bit-day (W.C. 90% GEO) Latchup: Immune
Mean Time Between Failures (MTBF)	> 4.3M hours



The final design has completed characterization and qualification

RAD750™ Testing Status

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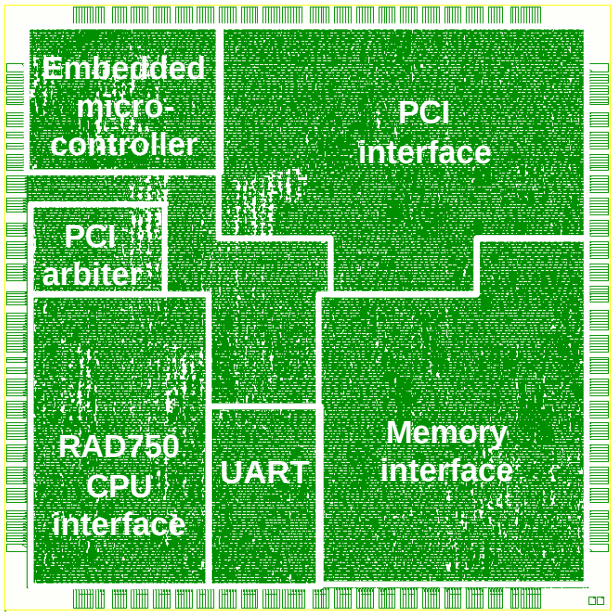
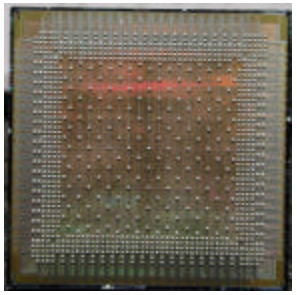
- RAD750™ Testing was completed October 31 (functional equivalency to PowerPC™ 750 verified)
- Environmental testing proved successful across the full military temperature and voltage ranges
- Performance specification will be 110 MHz - 133 MHz based upon screening levels
- Radiation testing results support flight requirements
  - No latchup nor gate rupture
  - TID >200Krad(Si)
  - SEU <1E-10 error/bit.day
    - Threshold LET(@10% of Saturation) = 45 MeV/mg/cm^2
- RAD750™ Specification Updated to reflect testing

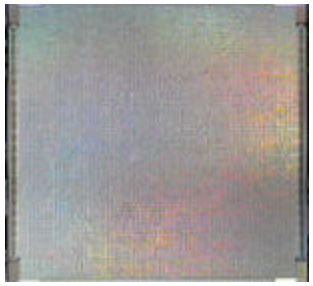
Power PCI ASIC specifications

BAE SYSTEMS

Specifications	
Clock Speed	33 MHz
Process Technology	0.50 um Leff CMOS, 5 levels of metal
Die Size	12.7 mm. by 12.7 mm.
Cells / Gates / Latches	926K / 700K / 26K
PCI Peak Bandwidth	130 MB/s write 90 MB/s read
Signal I/O	456 *(+ test)*
Power Supply	3.3 V + / - 10% core and I/O
Power Dissipation	1.5 W
Temperature Range	-55ºC to +125ºC
Packaging	32.5 mm. By 32.5 mm. By 6.22 mm. 624 pin Column Grid Array (CGA) with flip-chip C4 mount
Radiation Hardness	Total Ionizing Dose: >1Mrad (Si) SEU: < 1E-10 upsets / bit-day (W.C. 90% GEO) Latchup: Immune
Mass	14.5 grams





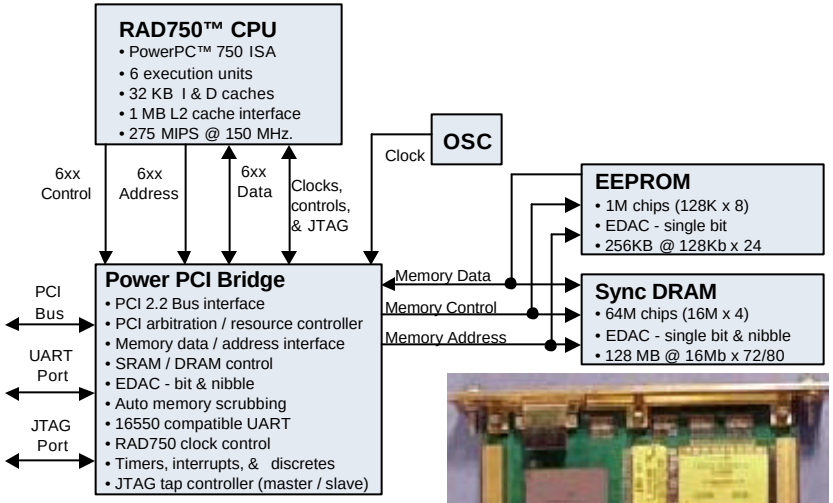


The Power PCI has been integrated on a 3U CompactPCI single board computer

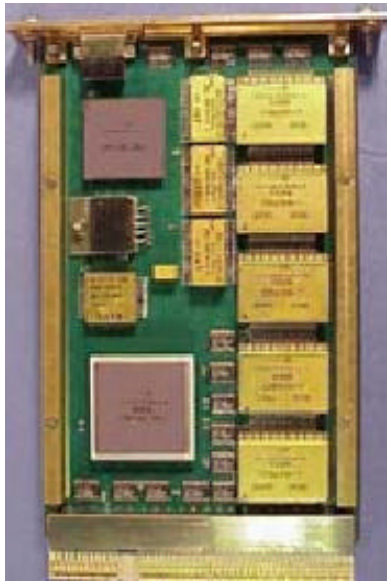
Conduction Cooled CompactPCI®
3U Format RAD750™ Processor Board

BAE SYSTEMS

Specifications	
Form Factor	*CompactPCI 3U (100 mm x 160 mm.)* *Weight: 549 grams*
Processor	*RAD750™ 240 Dhrystone 2.1 MIPS @ 133 MHz.*
Radiation Hardness	Total Ionizing Dose: > 100 Krad (Si) SEU: < 1E-5 upsets/day (W.C. 90% GEO) Latchup: Immune
Performance (estimated)	*5.8 SPECint95 3.5 SPECfp95 @ 133 MHz.*
PCI Backplane Bus	*32 bit, 33 MHz., PCI version 2.2* *Peak Bandwidth: 130 MB/s write 90 MB/s read* *Can be keyed for System or Agent Slot*
Power Supply	*3.3 V + / - 10%* *(2.5 V generated via on-board regulator)*
Power Dissipation (typ)	*10 W*
Temperature Range	*-55°C to +125°C*
Mean Time Between Failures (MTBF)	*Greater than 390K hours*



Flight boards have completed qualification for NASA JPL!



Currently available in flight, engineering and low cost commercial versions

The RAD750™ product line introduces a completely new era of both on-board processing capability and space standard products

RAD750™ Software Development Environment

BAE SYSTEMS

Software Development System

- Pentium personal computer
- Windows NT Operating System
- Ethernet connection to RAD750
- Corellis JTAG interface
- RAD750 or COTS PowerPC Board

Green Hill Multi and GNU Tools

- Optimized C, C++, Ada compilers
- Source level debugger
- Mixed language integration
- Version control system
- Program builder
- Editor

WindRiver VxWorks OS

- High performance multi-tasking kernal
- Networking capability
- Device independent I/O
- Dynamic load of user programs
- Highly configurable execution environment
- **"Tornado"** Software development and debug tools

BAE SYSTEMS Supplied Software

Board Support Package (BSP)
- VxWorks compatible

I/O device drivers

Start-Up ROM (SUROM)
- System "Reset handler"
- On-board diagnostics
  - CPU and Power PCI self-test
  - Memory test
- Bootstrap image load into RAM
- Test and initialize board hardware
- Fault recovery during restart

A complete environment, based on our RAD6000™ experience, eases RAD750™ software development

Hardened Processor Flight Heritage

BAE SYSTEMS

1995 - November, 2001 (Launched)

SATELLITE	SATs	SBCs
Agila / APSTAR-2R	2	4
Cassini	1	7
EchoStar 5	1	2
Garuda 1 (ACeS)	1	2
Globalstar (16 bit)	52	104
GOES L, M	2	4
Intelsat 901	1	4
NSTAR A,B	2	4
SS/L DBS-2	1	2
PAS 6 - 8	3	6
Sirius 3 - CD Radio	3	6
Sky 1A (MCI)	1	2
Telstar 5-7 (Skynet)	3	6
TEMPO 2	1	2
16 Bit Computers	74	155
Deep Space 1	1	1
FAISat	1	1
Fuse	1	1
Globalstar (32 bit)	52	104
Mars Odyssey	1	2
MightySat 1	1	1
Orbiter/Lander -X	3	7
Mars Pathfinder	1	1
LMA (STEX, Stardust)	2	4
TSX-5	1	1
RAD6000 Computers	64	123

2001 - 2003 (Under Contract)

SATELLITE	SATs	SBCs
ChinaSat 8	1	2
Globalstar (16 bit)	4	8
Intelsat 902	1	4
SS/L DBS-3	2	4
Sky 2A (MCI)	1	2
Telstar 8-9 (Skynet)	3	6
16 Bit Computers	12	26
ETS-8	1	4
Globalstar (32 bit)	4	8
Gravity Probe B	1	9
HESSI	1	1
HIRDLs	1	2
MightySat 2	1	1
C/NOFS	1	1
RAD6000 Computers	10	26

2004 - 2006 (Under Contract / Plan)

SATELLITE	SATs	SBCs
Intelsat 903-905	3	12
KaStar 1,2	2	4
Messenger	2	10
Storage Unit	2	4
Astrolink 1- 4	4	8
Coriolis	1	1
AEHF (Bus)	5	10
GENESIS	1	2
MIRO	1	2
MSL	1	2
Muses-C	1	2
SIRTF	1	4
Solstice/VCL	2	3
SWIFT	1	4
Solar X-Ray	1	2
TES	1	2
TRIANA	1	3
DRP	1	4
X-2000	5	20
AEHF (Payload)	5	30
Athena	1	1
Classified	12	16
CloudSat	1	2
Deep Impact	1	2
Discovery	4	5
Mars 03 Micro Miss	1	2
Secchi	1	4
SBIRS Low	24	100

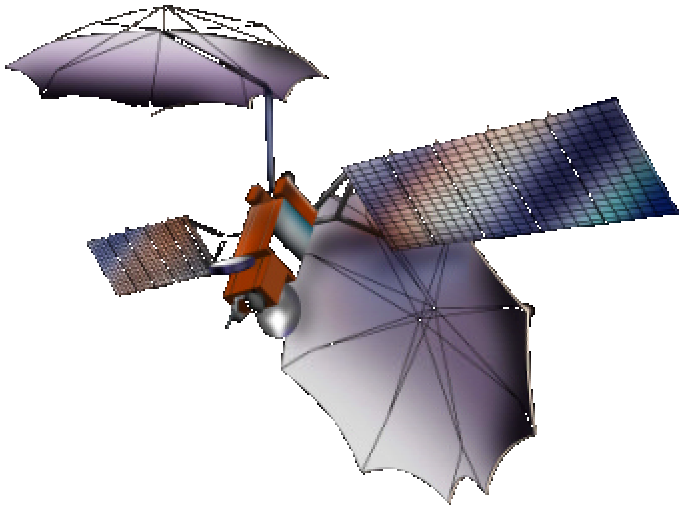
In Space Today: 86 Satellites 278 Computers

Hours on Orbit: 16 Bit - 3.7 Million RAD6000 - 2.4 Million

10/24/01

16 Bit RAD6000 RAD750

BAE SYSTEMS

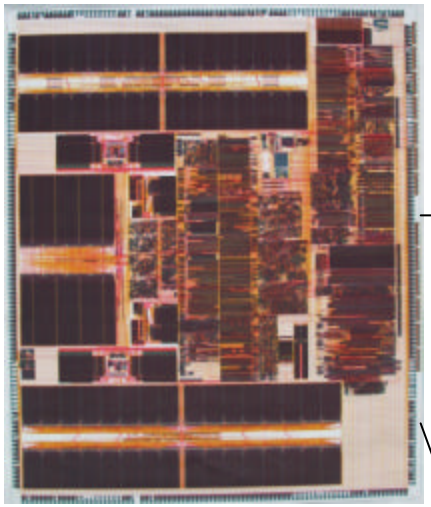


Agenda

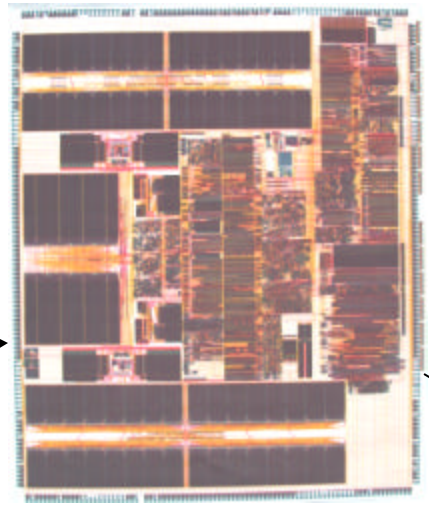
- The Environment
- Effect of Technology Migration
- Mitigation Schemes and Penalties
- Radiation Hardened Processors for Space
- Space Processor Roadmap
- Conclusion

RAD750 Forward Plan Options (2002-2006)

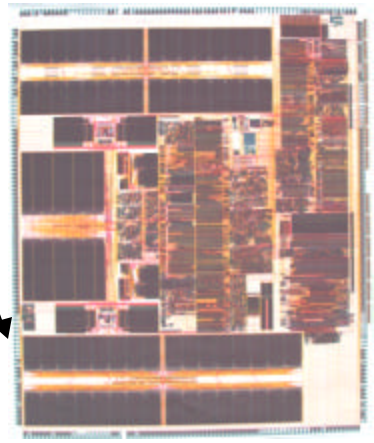
BAE SYSTEMS



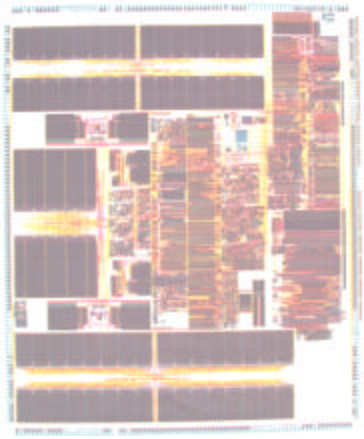
2002
RAD750™ *(pass 2)*
0.25 µm Bulk CMOS (Comm'l Foundry)
(Budgeted in '02)
- **130 sq mm**
- **10.4 M transistors**
- **166 MHz**
- **300 MIPS**
- **200 Krad (Si) Total Dose**
- **1E-11 error/ bit-day SEU**



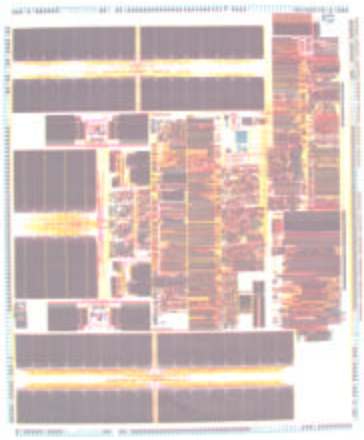
2004
"Megarad" RAD750™
0.25 µm Bulk CMOS (Accelerated RH Foundry Program w/ addl product support)
- **130 sq mm**
- **10.4 M transistors**
- **166 MHz**
- **300 MIPS**
- **1 Mrad (Si) Total Dose**
- **1E-11 error/ bit-day SEU**



2003
RAD750™
0.18 µm Bulk CMOS (Comm'l Foundry-w/ add'l product support)
- **est. 90 sq mm**
- **10.4 M transistors**
- **est .200 MHz**
- **366 MIPS**
- **200 Krad (Si) Total Dose**
- **1E-11 error/ bit-day SEU**



2005
"Megarad" RAD750™
0.18 µm Bulk CMOS (Accelerated RH Foundry Program w/ prod spt)
- **est. 90 sq mm**
- **10.4 M transistors**
- **est. 200 MHz**
- **366 MIPS**
- **1 Mrad (Si) Total Dose**
- **1E-11 error/ bit-day SEU**



2006
"Megarad" RAD750™
0.18 µm Fully Depleted SOI/ SOS CMOS (Accelerated RH Foundry Program w/ process & product support)
- **est. 90 sq mm**
- **10.4 M transistors**
- **est. 250 MHz**
- **457 MIPS**
- **1 Mrad (Si) Total Dose**
- **1E-11 error/ bit-day SEU**

Space Processor Roadmap 2001-2005

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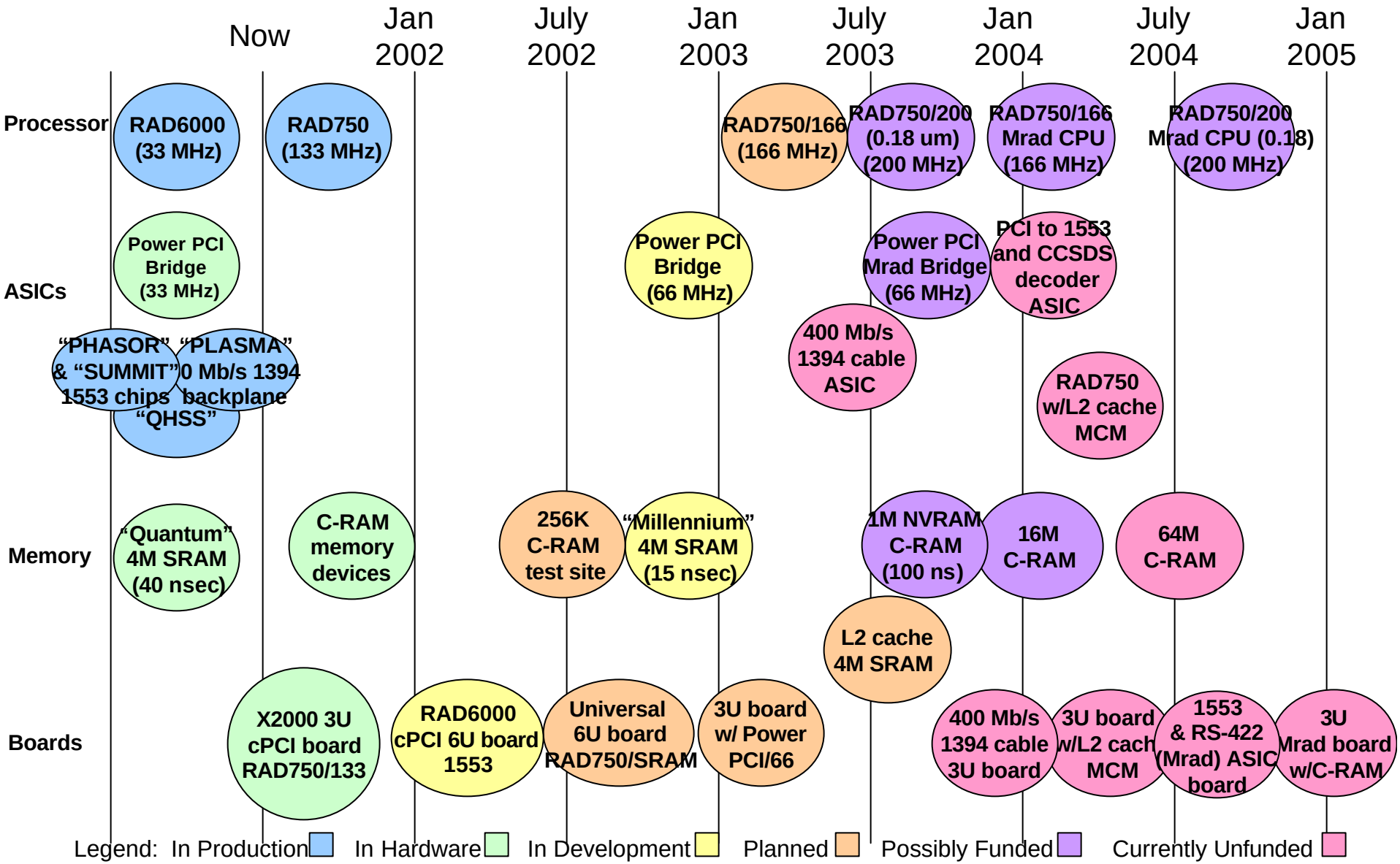
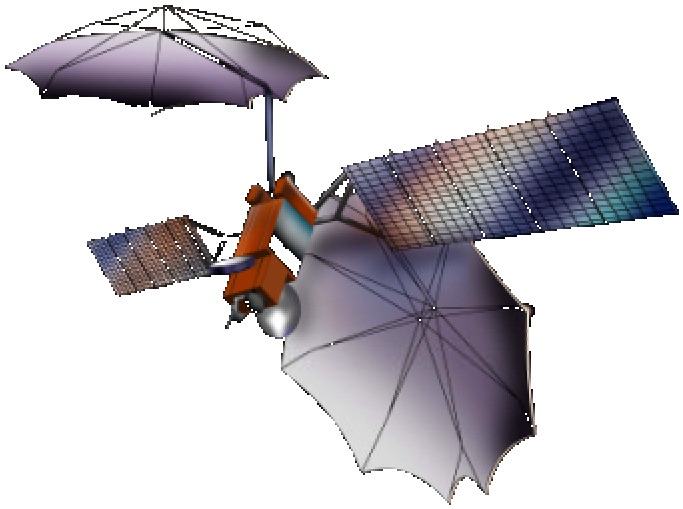


BAE SYSTEMS



Agenda

- The Environment
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What it all Means

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- Space microelectronics have to operate in a severe environment
- Users are driven to high performance electronics to address new and expanded applications:
  - Available COTS are very sensitive to space radiation
  - Variation in the radiation environment with orbit and over time is a major consideration in processor selection
  - Mitigation techniques have significant impact on weight, power and performance.
  - Technology scaling results in dramatically increased exposure to Single Event Effects in more modern semiconductor components
- Radiation Hardened Processors offer the best solution
  - Capitalize on massive commercial investment in hardware and software
  - Enhanced for the various environmental issues
  - Offer the best power/performance/mass/volume alternative

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